MOTOROLA

TELECOMMUNICATIONS DEVICE DATA

Motorola is a major supplier of Semiconductors to Telecommunications equipment manufacturers worldwide, and our data manuals for such standard products as dedicated MOS and Bipolar Telecom ICs, CMOS Special Circuits, High-Speed CMOS, ECL, TTL, Linear, Power Transistors, Microprocessors, and Memories, are on the reference shelves of designers throughout the industry.

This data book pulls together Motorola's Semiconductor Products which are dedicated to applications in Telecommunications. It reflects both the growing portfolio of Motorola devices for Telecommunications and the need for designers to have product information at hand in a convenient form.

Many of the products presented here are new, for new applications in an industry which is presently one of the most dynamic and fastest growing—Telecommunications. It was possible only to include a limited amount of application material. Hence these products are supported by applications and product specialists within the Motorola Semiconductor organizations. Should you require further details or assistance in designing with any of these devices, your Motorola Semiconductor Sales Office can put you in touch with the relevant expertise within our organization.

Motorola reserves the right to make changes to any product herein to improve reliability, function or design. Motorola does not assume any liability arising out of the application or use of any product described herein; neither does it convey any license under its patent rights nor the rights of others.

Motorola, Inc. general policy does not recommend the use of its components in life support applications, where in a failure or malfunction of the component may directly threaten life or injury. Per Motorola Terms and Conditions of Sale, the user of Motorola components in life support applications assumes all risk of such use and indemnifies Motorola against all damages.

ISBN 1 870760 03 4

First Edition 1985—DLE136/D
Second Edition 1988—DLE136R1/D
Printed in Great Britain by Grosvenor Press (Portsmouth) Ltd, 8,000, 4/88

Alphanumeric Index 1

1

ALPHANUMERIC INDEX

1

Selector Guide and Cross-Reference

2

INDEX BY FUNCTION

Competition Cross-Reference

Device Title	Supplier	Description	Nearest Motorola Equivalent
AMS3201	APTEK	DTMF Receiver	MC145436
AMS3210	APTEK	DTMF Receiver	MC145436
AMS3870	APTEK	DTMF Receiver (MITEL)	MC145436
AM79C30	AMD	ISDN S/T Interface	MC145474 + MC145500
AM79C31	AMD	ISDN S Interface Transc.	MC145474
AM79C32	AMD	ISDN S Interface Transc.	MC145474
AM79C33	AMD	ISDN U Interface Transc.	MC145472
AM79C36	AMD	ISDN Term. Power Contr.	MC34129
AM7901	AMD	COMBO (SLAC)	MC145500/01/02/03/05
AM7905	AMD	COMBO (SLAC)	MC145500/01/02/03/05
AM7910	AMD	V21/V23 Modem	MC145442 (V21)
AM7911	AMD	V21/V23 Modem	MC145442 (V21)
AM7950	AMD	SLIC	MC3419 - 1L
AM7953	AMD	SLIC	MC3419 - 1L
AY-5-9151	Gen. Instr	Pulse Dialer	MC145409
BA6571	Rohm	Handsfree Speakerphone	MC34018 or MC34118
CD22100	RCA	Crosspoint Switch	MC142100*
CD22101	RCA	Crosspoint Switch	MC142101*
CD22103	RCA	Transcoder	MC142103*
CD22204	RCA	DTMF Receiver	MC145436
CD22419	RCA	SLIC	MC3419 - 1L
C5262	Cherry	Handsfree Speakerphone	MC34018 or MC34118
CS34017	Cherry	Tone Ringer	MC34017*
DF320/320A/322A	Siliconix	Pulse Dialer	MC145409
DF320/321/322/323	ITT	Pulse Dialer (Siliconix)	MC145409
DF820	Siliconix	Pulse Dialer	MC145409
EFB7310	Thomson	Crosspoint Switch (RCA)	MC142100*
EFB7446	Thomson	Transcoder	MC142103
EF7332 + 7333	Thomson	Transcoder	MC142103
EF7910	Thomson	V21/V23 Modem (AMD)	MC145442
ETC5040	Thomson	PCM Filter (NSC TP3040)	MC4413/14
ETC5051/54/56/57	Thomson	COMBO (NSC TP3051 . . .)	MC145500/01/02/03/05
ETC5064/67	Thomson	COMBO (NSC TP3064)	MC145500/01/02/03/05
GA6112	Rohm	Handsfree Speakerphone	MC34018 or MC34118
G8870	GTE	DTMF Receiver (MITEL)	MC145436
HC5501/02/04/08	Harris	SLIC	MC3419 - 1L
HC5521	Harris	SLIC	MC3419 - 1L
HC5541	Harris	Pulse/DTMF Dialer	MC145410
HC5552/53/54/57	Harris	COMBO (NSC TP3052 . . .)	MC145500/01/02/03/05
HC5560	Harris	Transcoder	MC145439*
HC5570	Harris	V21 Modem	MC145442
HD44210/11/12	Hitachi	COMBO	MC145500/01/02/03/05
HD44230/31/32/33/34	Hitachi	COMBO	MC145500/01/02/03/05
HD44235/36/37/38	Hitachi	COMBO	MC145500/01/02/03/05
HD44247/48	Hitachi	COMBO	MC145500/01/02/03/05
HD44270A	Hitachi	SLIC	MC3419 - 1L
ITT90 + 91 + 92	ITT	Handsfree Speakerphone	MC34018 or MC34118
LB1020 + 1021	ATT (SGS)	Handsfree Speakerphone	MC34018 or MC34118
LM386	NSC	Teleph. Loudsp. Amp.	MC34119
LR3N3	Sharp	Tone Ringer	MC34017
LR3N31	Sharp	Telephone Speech Circuit	MC34014
LR3N33	Sharp	Handsfree Speakerphone	MC34018 or MC34118
LR40981/982	Sharp	Pulse Dialers (MOSTEK)	MC145409
LR40991/992	Sharp	Pulse Dialers (MOSTEK)	MC145409
LR40993/994	Sharp	Pulse Dialers	MC145409*
LR4803	Sharp	Pulse/DTMF Rep. Dialer	MC145412/13
LS1240	SGS	Tone Ringer	MC34017
LS1241	SGS	Tone Ringer	MC34017

Device Type	Supplier	Description	Nearest Motorola Equivalent
LS156	SGS	Telephone Speech Circuit	MC34014
LS285/288	SGS	Telephone Speech Circuit	MC34014
LS356/388/588/656	SGS	Telephone Speech Circuit	MC34014
L3000 + 3010	SGS	SLIC (Hi Volt + Low Volt)	MC3419 - 1L
L3240	SGS	Tone Ringer	MC34017
MB87003/004	Fujitsu	Pulse/DTMF Dialer	MC145410
MH88500	Mitel	SLIC	MC3419 - 1L
MJ1471	Plessey	Transcoder	MC142103*
MK50981/82/91/92	Thomson Mostek	Pulse Dialer	MC145409
MK5102	Thomson Mostek	DTMF Decoder	MC145436
MK5370N/71N/72N	Thomson Mostek	Pulse/DTMF Dialer	MC145410
MK5375N/76N	Thomson Mostek	Pulse/DTMF Rep. Dialer	MC145412/13
ML8204/05	Mitel (SGS)	Tone Ringer	MC34017
MSM6926RS	OKI	V21 Modem	MC145442
MT3506/07	Mitel	COMBO	MC145500/01/02/03/05
MT4320/22/23	Mitel	Pulse Dialer (Siliconix)	MC145409
MT4325/26/27	Mitel	Pulse Dialer	MC145409
MT5501	Mitel	Pulse/DTMF Dialer	MC145410
MT8860/62/63	Mitel	DTMF Decoder	MC145436
MT8870	Mitel	DTMF Receiver	MC145436
MT8912	Mitel	PCM Filter (Intel)	MC14413/14
MT8930	Mitel	ISDN S Interface Transc.	MC145474
MT8952	Mitel	HDLC Controller	MC145488
MT8960/61/62	Mitel	COMBO	MC145500/01/02/03/05
MT8963/64/65	Mitel	COMBO	MC145500/01/02/03/05
MT8972	Mitel	ISDN U Interface Transc.	MC145472
M22100	SGS	Crosspoint Switch (RCA)	MC142100*
M22101	SGS	Crosspoint Switch (RCA)	MC142101*
M2560A	SGS	Pulse Dialer (AMI)	MC145409
M3326/27	SGS	Pulse Dialer	MC145409
M5912	SGS	PCM Filter (Intel)	MC14413/14
M5913/14/16/17	SGS	COMBO (Intel)	MC145500/01/02/03/05
M947/956/957/977	Teltone	DTMF Receiver	MC145436
PBL3725/26	Rifa	Telephone Speech Circuit	MC34014
PBL3781	Rifa	Telephone Speech Circuit	MC34014
PBL3785	Rifa	Tone Ringer	MC34017
PBM3910	Rifa	Handsfree Speakerphone	MC34018 or MC34118
PCD3310	Philips	Pulse/DTMF Dialer	MC145410
PCD3315	Philips	Pulse/DTMF Rep. Dialer	MC145516
PCD3320/21/22/23/25	Philips	Pulse Dialer	MC145409
PCD3360	Philips	Tone Ringer	MC34017
PCD4410	Philips	Pulse/DTMF Dialer	MC145410
PEB2060	Siemens	COMBO (Sicofi)	MC145500/01/02/03/05
PEB2070	Siemens	LAP D Controller	MC145488
PEB2080	Siemens	ISDN S Interface Transc.	MC145474
PEB2090	Siemens	ISDN U Interface Transc.	MC145472
PEB2095	Siemens	Burst Controller	MC145421/25 (UDLT2)
SC11203/204	Sierra Sc.	DTMF Receiver (SSI)	MC145436*
SS1203/204	Silicon System	DTMF Receiver	MC145436*
S2550	AMI	Speech Circt. + Tone Ringer	MC34014 + MC34017
S2551	AMI	Speech Circt. + Tone Ringer	MC34014 + MC34017
S2552	AMI	Speech Circt. + Pulse dial	MC34014 + MC145409
S2553	AMI	Speech Circt. + DTMF Dial.	MC34014 + MC14410
S2560	AMI	Pulse Dialer	MC145409
S2560A	AMI	Pulse Dialer	MC145409
S2561A	AMI	Tone Ringer	MC34017

Device Type	Supplier	Description	Nearest Motorola Equivalent
S2563A	AMI	Pulse/DTMF Rep. Dialer	MC145412/13
S2570/71/73	AMI	Pulse/DTMF Dialer	MC145410
S2575	AMI	Pulse/DTMF Rep. Dialer	MC145516
S3506/07	AMI	COMBO (Mitel)	MC145500/01/02/03/05
S3530	AMI	V21 Modem	MC145442
S44231/32/33/34	AMI	COMBO (Hitachi)	MC145500/01/02/03/05
S7230	Seiko	Pulse/DTMF Dialer	MC145410
S7283	Seiko	Pulse/DTMF Rep. Dialer	MC145516
TA31008	Toshiba	Telephone Speech Circuit	MC34014
TA31023	Toshiba	Telephone Speech Circuit	MC34014
TA7331	Toshiba	Telephone Loudsp. Ampli.	MC34119
TBA820	SGS	Telephone Loudsp. Ampli	MC34119
TBA915G	Philips	Telephone Loudsp. Ampli.	MC34119
TCM1501A/06A/09A/12A	Texas	Tone Ringer	MC34017
TCM1705/06	Texas	Telephone Speech Circuit	MC34014
TCM2222	Texas	Transcoder	MC142103
TCM2912	Texas	PCM Filter (Intel)	MC14413/14
TCM2913/14/16/17	Texas	COMBO (Intel)	MC145500/01/02/03/05
TCM4201 + 4202	Texas	SLIC	MC3419 - 1L
TDA7050	Philips	Telephone Loudsp. Ampli.	MC34119
TDB3111 + 3311	Thomson	SLIC (Hi Volt + Low volt)	MC3419 - 1L
TEA1042	Philips	Handsfree Speakerphone	MC34018 or MC34118
TEA1046	Philips	Speech Circt. + DTMF Dial.	MC34014 + MC14410
TEA1060/61/67/68	Philips	Telephone Speech Circuit	MC34014
TEA3046/47	Thomson	Speech + DTMF Circt. (GMY)	MC34014 + MC14410
TEA7030/36/37	Thomson	Speech + DTMF Circt. (FRA)	TCA3381 + 82 + 83
TEA7531	Thomson	Telephone Loudsp. Ampli.	MC34119
TMS99534A	Texas	V21 Modem	MC145442
TP3040	National Sc.	PCM Filter	MC14413/14
TP3051/52/53/54	National Sc.	COMBO	MC145500/01/02/03/05
TP3056/57	National Sc.	COMBO	MC145500/01/02/03/05
TP3064/67	National Sc.	COMBO	MC145500/01/02/03/05
TP3200/01	National Sc.	SLIC	MC3419 - 1L
TP50981/82/85	National Sc.	Pulse Dialer (Mostek)	MC145409
TP53190	National Sc.	Pulse Dialer	MC145409
TP5700	National Sc.	Telephone Speech Circuit	MC34014
UAB1023	ITT	COMBO	MC145500/01/02/03/05
UA3054/57	Fairchild	COMBO (NSC TP3054/57)	MC145500/01/02/03/05
UA5800	Fairchild	SLIC	MC3419 - 1L
ULN2283	Sprague	Telephone Loudsp. Ampli.	MC34119
UPC1218	NEC	Telephone Loudsp. Ampli.	MC34119
UPD22100	NEC	Crosspoint Switch (RCA)	MC142100*
XR-T6420 + T6421	Exar	Handsfree Speakerphone	MC34018 or MC34118
29C48	Intel (Harris)	ISDN COMBO	MC145500/01/02/03/05
29C51	Intel	COMBO	MC145500/01/02/03/05
29C53	Intel (Harris)	ISDN S Interface Transc.	MC145474
2912	Intel	PCM Filter	MC14413/14
2913/14/16/17	Intel	COMBO	MC145500/01/02/03/05
4913/14/16/17	Intel	COMBO	MC145500/01/02/03/05

(*) Means Devices are True Second Sources

MOTOROLA

2

NEW ISDN DEVICES

In addition to the devices included in this data book, Motorola wishes to announce the following devices presently under development, and for which insufficient data was available at the time of going to press. Please contact your local Motorola sales office if you need more details.

MC145470/71: UDLT2 with IDL* Interface

MC145472: ISDN "U" Interface transceiver
* transmits/receives 160K bits/s of data on 2 wires
* uses IDL* for data transfer
* uses 2B1Q block code for data transmission on the line as defined by the T1D1 committee.

MC145474: ISDN "S/T" Interface transceiver (see Product Preview)

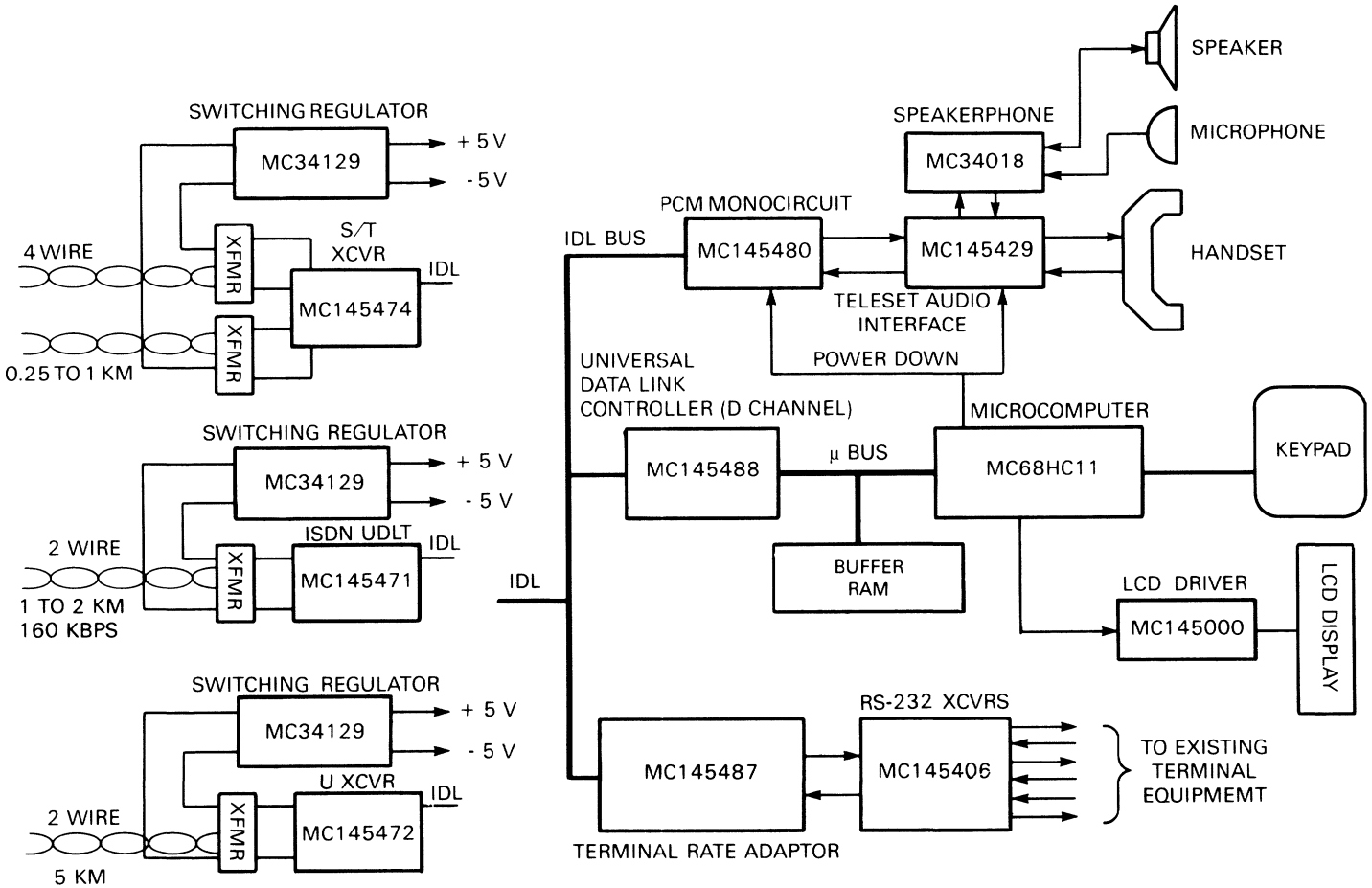
MC145480: Enhanced codec/filter with IDL interface

MC145487: ISDN Terminal rate adapter, with IDL interface

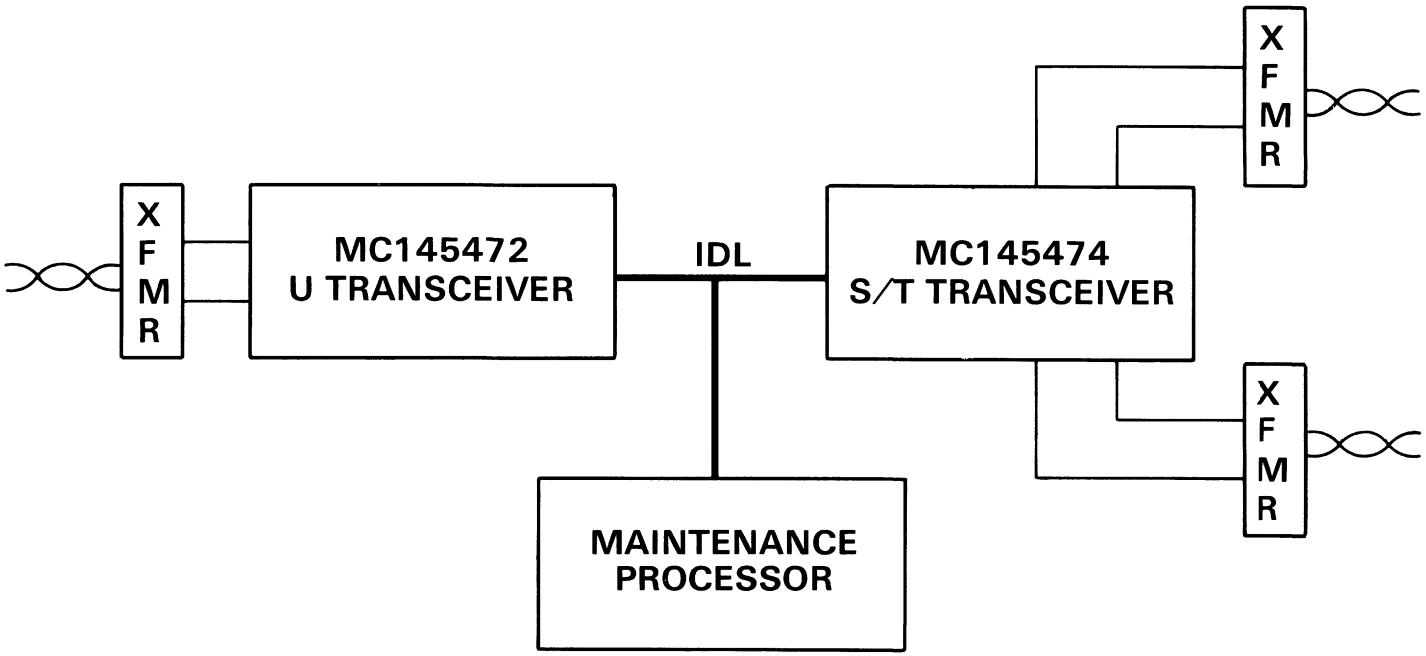
MC145488: Dual data link controller (see Product Preview).

*IDL = Interchip digital link. Standard Motorola bus used for the interchange of data between ISDN devices.

ISDN BASIC TERMINALS



ISDN
NETWORK TERMINATION 1



Data Sheets 3

MOTOROLA

Technical Summary

56-Bit General Purpose Digital Signal Processor

This document provides a technical summary of the architecture and instruction set for the DSP56001, a fourth generation, low power, HCMOS, user-programmable digital signal processor. The DSP56001 is a member of Motorola's family of general purpose Digital Signal Processors. The DSP56001 features 512 words of full speed on-chip program RAM memory, two preprogrammed data ROMs, and special on-chip bootstrap hardware to permit convenient loading of user programs into the program RAM.

The core of the processor consists of three execution units operating in parallel — the data ALU, the address ALU, and the program controller. The DSP56001 has MCU-style on-chip peripherals, program and data memory, as well as a memory expansion port. The MPU-style programming model and instruction set make the generation of efficient, compact code straightforward. The DSP56001 instruction set is identical to the DSP56000 instruction set.

Core Features

- 10.25 Million Instructions Per Second (MIPS)
- Single Cycle Data ALU
  - 24 x 24 ♦ 56-Bit Parallel Multiply/Accumulate
  - Two 56-Bit Accumulators
  - Ten Data Registers
  - Two Data Bus Shifter/Limiters
- DSP Oriented Address ALU
  - 24 Address Registers
  - Dual Modulo Arithmetic Units
  - Linear, Modulo, and Bit Reversed Address Generation
- Advanced Program Controller
  - 15 Level Hardware Stack
  - Nested Hardware DO Loops
  - No Overhead Auto-Return (Fast) Interrupts
- Highly Orthogonal Instruction Set
  - 62 MPU-Style Instruction Types
  - Makes Pipeline Invisible
  - Suitable for High Level Language (HLL) Compilers
- Multiple Buses
  - Four Data Buses
  - Three Address Buses

On-Chip MCU-Style Peripherals

- 24 Programmable I/O Port Pins or a Combination of I/O Port Pins and
  - 8-Bit Parallel Host MPU/DMA Interface
  - Serial Communication Interface with Baud Rate Generator
  - Synchronous Serial (Codec) Interface with Clock Generator

On-Chip Memory

- Two Independent 256 x 24-Bit Data RAMs
- Two 256 x 24-Bit Preprogrammed Data ROMs
- 512 x 24-Bit Program RAM

Off-Chip Memory Expansion

- 128K x 24-Bit Data Memory
- 64K x 24-Bit Program Memory
- Programmable Off-Chip Access Times (Wait States)

BRE505/D

PROGRAM RAM (PRAM)

The DSP56001 program memory contains 512 words of high speed, on-chip Program RAM (PRAM). The DSP56001 PRAM can be loaded with the user's program after power-up reset. The bootstrap mode, described in Appendix I, provides a convenient, low cost method to load the DSP56001 PRAM.

The PRAM DSP56001 offers many advantages:

- The DSP56001 is an off-the-shelf product because it contains user programmable PRAM instead of factory programmable ROM.
- PRAM allows quick program development.
- On-chip PRAM operates at the full DSP56001 speed with no bus contention with external Data Memory space accesses.
- Programs can be changed dynamically, allowing efficient overlaying of DSP software algorithms.
- The user can write to PRAM from an application program using the MOVEM instruction.
- The bootstrap mode allows the designer to easily initialize the PRAM. Bootstrap mode can:
  - — load PRAM from a single, inexpensive EPROM
  - — load PRAM through the Host Interface from a microprocessor.

SIGNAL DESCRIPTION

The DSP56001 is an 88-pin integrated circuit available in surface mount or pin-grid array packaging. Its input and output signals are organized into seven functional groups which are listed below and shown in Figure 1.

Address and Data Buses
Bus Control
Interrupt and Mode Control
Power and Clock
Host Interface or PI/O
SCI Interface or PI/O
SSI Interface or PI/O

Descriptions of the signals in each group are given in the following paragraphs.

3

ADDRESS AND DATA BUS

The following paragraphs describe the address and data bus signals.

Address Bus (A0-A15)

These three-state output pins specify the address for external program and data memory accesses. A0-A15 do not change state when external memory spaces are not being accessed in order to minimize power dissipation.

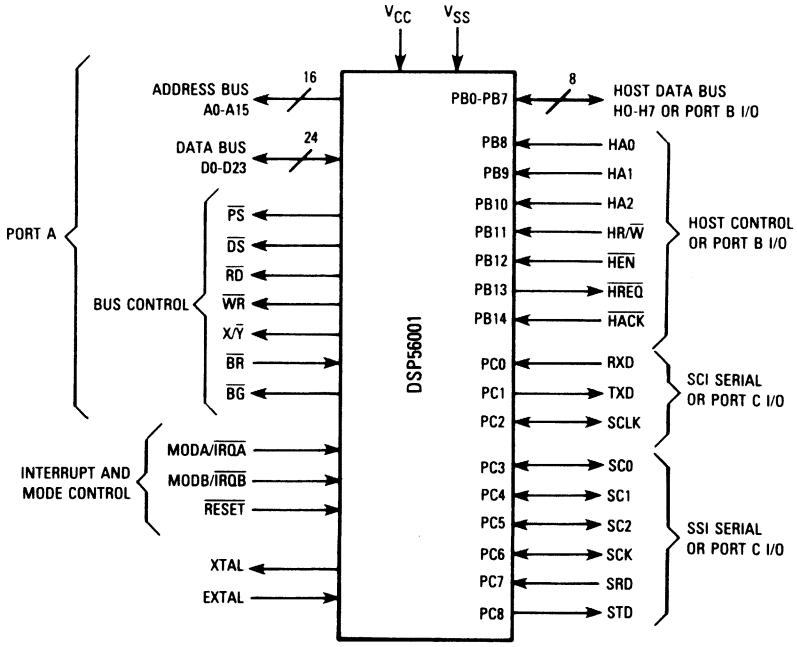


Figure 1. Functional Signal Groups

Data Bus (D0-D23)

These pins provide the bidirectional data bus for external program and data memory accesses. D0-D23 are in the high-impedance state when the bus grant signal is asserted in order to minimize power dissipation.

BUS CONTROL

The following paragraphs describe the bus control signals.

Program Memory Select ($\overline{PS}$)

This three-state output is asserted only when external program memory is referenced.

Data Memory Select ($\overline{DS}$)

This three-state output is asserted only when external data memory is referenced.

X/$\overline{Y}$ Select (X/$\overline{Y}$)

This three-state output selects which external data memory space (X or Y) is referenced by data memory select $\overline{DS}$.

Read Enable ($\overline{RD}$)

This three-state output is asserted to read external memory on the data bus D0-D23.

Write Enable ($\overline{WR}$)

This three-state output is asserted to write external memory on the data bus D0-D23.

Bus Request ($\overline{BR}$)

The bus request input $\overline{BR}$ allows another device such as a processor or DMA controller to become the master of the external data bus D0-D23 and external address bus A0-A15. When $\overline{BR}$ is asserted, the DSP56001 will release control of the external data bus D0-D23, address bus A0-A15 and bus control pins $\overline{PS}$, $\overline{DS}$, X/$\overline{Y}$, $\overline{RD}$, and $\overline{WR}$. These pins will be placed in the high-impedance state and the bus grant, $\overline{BG}$, output will be asserted.

Bus Grant ($\overline{BG}$)

This three-state output is asserted to acknowledge an external bus request.

INTERRUPT AND MODE CONTROL

The following paragraphs describe the interrupt and mode control signals.

Mode Select A, B (MODA, MODB) or External Interrupt Request A, B ($\overline{IRQA}$, $\overline{IRQB}$)

These two inputs have two functions — 1) to select the initial chip operating mode and, 2) to receive an interrupt request from an external source. MODA and MODB are read and internally latched in the DSP when the processor exits the RESET state. Several clock cycles after leaving the RESET state, the MODA and MODB pins automatically change to external interrupt requests $\overline{IRQA}$ and $\overline{IRQB}$. After leaving the RESET state the chip operating mode can be changed by software. $\overline{IRQA}$ and $\overline{IRQB}$ may be programmed to be level sensitive or negative edge triggered.

Reset ($\overline{RESET}$)

This input pin is used to reset the DSP56001. When $\overline{RESET}$ is asserted, the DSP56001 is initialized and placed in the RESET state. When the $\overline{RESET}$ signal is removed, the initial chip operating mode is latched from the MODA and MODB pins.

POWER AND CLOCK

The following paragraphs describe the power and clock signals.

V_{CC} and V_{SS}

V_{CC} is the power input and V_{SS} is ground.

External Clock/Crystal Input (EXTAL)

EXTAL may be used to interface the internal crystal oscillator input to an external crystal or an external clock. The maximum clock rate is 20.5 MHz.

Crystal Output (XTAL)

This output connects the internal crystal oscillator output to an external crystal. If an external clock is used, XTAL should not be connected.

HOST INTERFACE

The following paragraphs describe the Host Interface.

Host Data Bus (H0-H7)

This bidirectional data bus is used to transfer data between the host processor and the DSP56001. This bus is an input unless enabled by a host processor read. H0-H7 may be programmed as general purpose parallel I/O pins called PB0-PB7 when the Host Interface is not being used.

Host Address (HA0, HA1, HA2)

These inputs provide the address selection for each Host Interface register. HA0-HA2 may be programmed as general purpose parallel I/O pins called PB8-PB10 when the Host Interface is not being used.

Host Read/Write (HR/$\overline{W}$)

This input selects the direction of data transfer for each host processor access. HR/$\overline{W}$ may be programmed as a general purpose I/O pin called PB11 when the Host Interface is not being used.

Host Enable ($\overline{HEN}$)

This input enables a data transfer on the host data bus. When $\overline{HEN}$ is asserted and HR/$\overline{W}$ is high, H0-H7 become outputs and DSP56001 data may be read by the host processor. When $\overline{HEN}$ is asserted and HR/$\overline{W}$ is low, H0-H7 become inputs and host data is latched inside the DSP when $\overline{HEN}$ is negated. Normally a chip select signal derived from host address decoding and an enable clock, is used to generate $\overline{HEN}$. $\overline{HEN}$ may be programmed as a

general purpose I/O pin called PB12 when the Host Interface is not being used.

Host Request ($\overline{\text{HREQ}}$)

This open-drain output signal is used by the DSP56001 Host Interface to request service from the host processor, DMA controller or simple external controller. $\overline{\text{HREQ}}$ may be programmed as a general purpose I/O pin (not open-drain) called PB13 when the Host Interface is not being used.

Host Acknowledge ($\overline{\text{HACK}}$)

This input has two functions — 1) to provide a Host Acknowledge handshake signal for DMA transfers and, 2) to provide a Host Interrupt Acknowledge compatible with MC68000 Family processors. $\overline{\text{HACK}}$ may be programmed as a general purpose I/O pin called PB14 when the Host Interface is not being used.

SERIAL COMMUNICATIONS INTERFACE (SCI)

The following paragraphs describe the serial communications interface.

Receive Data (RXD)

This input receives byte-oriented serial data and transfers the data to the SCI Receive Shift Register. Input data is sampled on the positive edge of the Receive Clock. RXD may be programmed as a general purpose I/O pin called PC0 when the SCI RXD function is not being used.

Transmit Data (TXD)

This output transmits serial data from the SCI Transmit Shift Register. Data changes on the negative edge of the transmit clock. This output is stable on the positive edge of the transmit clock. TXD may be programmed as a general purpose I/O pin called PC1 when the SCI TXD function is not being used.

SCI Serial Clock (SCLK)

This bidirectional pin provides an input or output clock from which the transmit and/or receive baud rate is derived. SCLK may be programmed as a general purpose I/O pin called PC2 when the SCI SCLK function is not being used.

SYNCHRONOUS SERIAL INTERFACE (SSI)

The following paragraphs describe the synchronous serial interface.

Serial Control Zero (SC0)

This bidirectional pin is used for control by the SSI serial interface. SC0 may be programmed as a general purpose I/O pin called PC3 when the SSI SC0 function is not being used.

Serial Control One (SC1)

This bidirectional pin is used for control by the SSI serial interface. SC1 may be programmed as a general purpose I/O pin called PC4 when the SSI SC1 function is not being used.

Serial Control Two (SC2)

This bidirectional pin is used for control by the SSI serial interface. SC2 may be programmed as a general purpose I/O pin called PC5 when the SSI SC2 function is not being used.

SSI Serial Clock (SCK)

This bidirectional pin provides the serial bit rate clock for the SSI interface. SCK may be programmed as a general purpose I/O pin called PC6 when the SSI interface is not being used.

SSI Receive Data (SRD)

This input pin receives serial data and transfers the data to the SSI Receive Shift Register. SRD may be programmed as a general purpose I/O pin called PC7 when the SSI SRD function is not being used.

SSI Transmit Data (STD)

This output pin transmits serial data from the SSI Transmit Shift Register. STD may be programmed as a general purpose I/O pin called PC8 when the SSI STD function is not being used.

BLOCK DIAGRAM DESCRIPTION

DSP56001 architecture has been designed to maximize throughput in data intensive Digital Signal Processing (DSP) applications. This objective has resulted in a dual natured, expandable architecture with sophisticated on-chip peripherals and general purpose I/O. It is dual natured in that there are two independent expandable data memory spaces, two address arithmetic units, and a data ALU which has two accumulators and two shifter/limiters. The duality of the architecture makes it easier to write software for DSP applications. For example, data is naturally partitioned into X and Y spaces for graphics and image processing applications, into coefficient and data spaces for convolution sums, and into real and imaginary spaces for performing complex arithmetic.

The major components of the DSP56001 are:

- Data Buses
- Address Buses
- Data ALU
- Address ALU
- X Data Memory
- Y Data Memory
- Program Controller
- Program Memory
- Bootstrap ROM
- Input/Output
  - Expansion Port
  - General Purpose I/O
  - Host Interface
  - SCI Interface
  - SSI Interface

These components are depicted in Figure 2 and described in the following paragraphs.

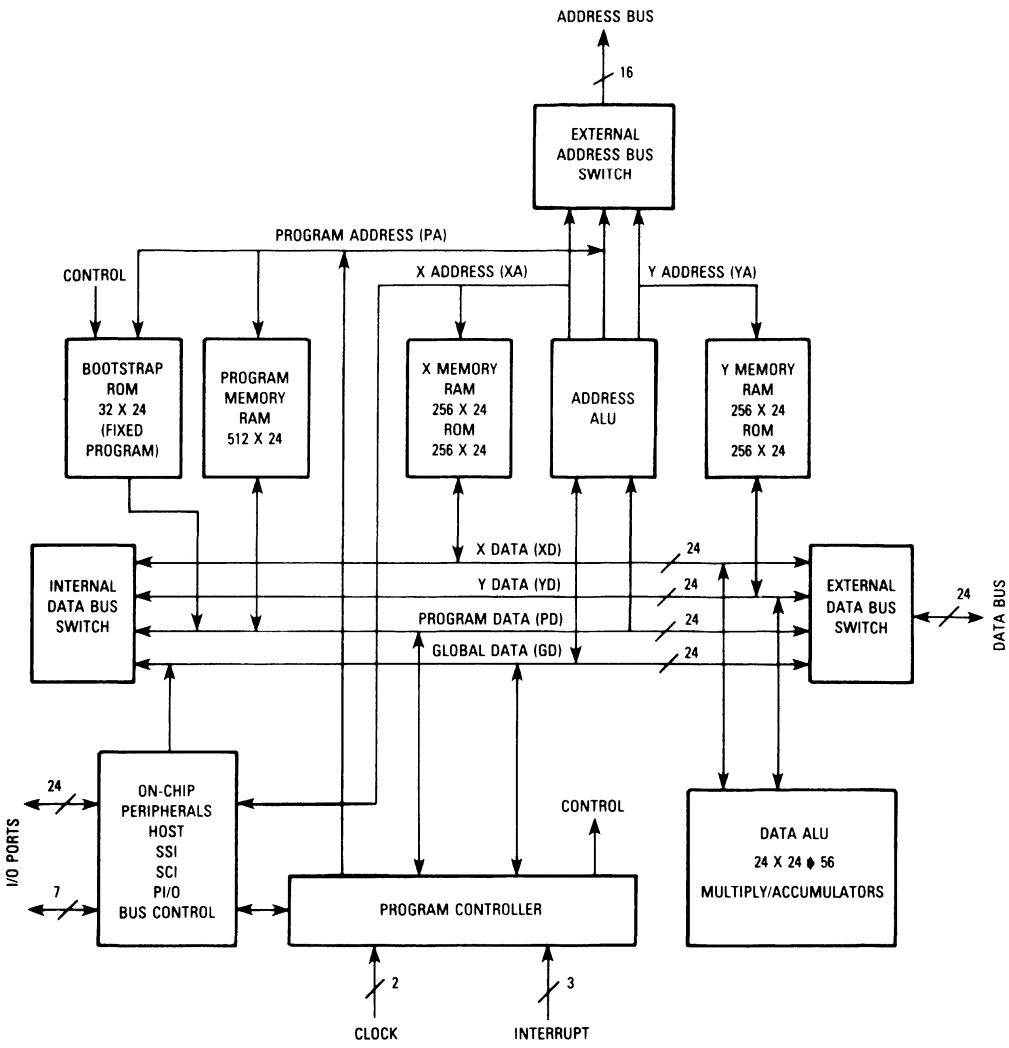


Figure 2. DSP56001 Block Diagram

DATA BUSES

Data movement on the chip occurs over four bidirectional 24-bit buses — the X data bus (XD), the Y data bus (YD), the program data bus (PD), and the global data bus (GD). The X and Y data buses may also be treated by certain instructions as one 48-bit data bus by concatenation of XD and YD. Data transfers between the data ALU and the X data memory and Y data memory occur over XD and YD. XD and YD are kept local on the chip to maximize speed and minimize power dissipation. All other data transfers such as I/O transfers to peripherals occur over GD. Instruction word pre-fetches take place in parallel over PD. Transfers between buses are accomplished in the internal bus switch.

ADDRESS BUSES

Addresses are specified for internal X data memory and Y data memory on two unidirectional 16-bit buses — X address bus (XA) and Y address bus (YA). Program memory addresses are specified on the program address bus (PA). External memory spaces are addressed via a single 16-bit unidirectional address bus driven by a three input

multiplexer that can select either the X address bus (XA), the Y address bus (YA), or the program address bus (PA). There is no speed penalty if only one external memory space is accessed in an instruction. If two or three external memory spaces are accessed in a single instruction there will be a one or two instruction cycle, respectively, execution delay. A bus arbitrator controls external access.

DATA ALU

The data ALU has been designed to be fast and yet provide the capability to process signals having a wide dynamic range. Special circuitry has been provided to facilitate handling data overflows and roundoff errors.

The data ALU performs all of the arithmetic and logical operations on data operands. The data ALU consists of four 24-bit input registers, two 48-bit accumulator registers, two 8-bit accumulator extension registers, an accumulator shifter, two data bus shifter/limiters, and a parallel single cycle non-pipelined multiply-accumulator (MAC) unit. Data ALU operations use fractional 2's complement arithmetic. Data ALU registers may be read or written over XD and YD as 24- or 48-bit operands. The data ALU is capable of performing any of the following operations in a single instruction cycle — multiplication, multiply-accumulate with positive or negative accumulation, convergent rounding, multiply-accumulation with positive or negative accumulation and convergent rounding, addition, subtraction, a divide iteration, a normalization iteration, shifting, and logical operations. Data ALU source operands may be 24-, 48-, or in some cases 56-bits and originate from data ALU registers. The data ALU destination is always one of the two 56-bit accumulators.

The 24-bit data words provide 144 dB of dynamic range. This is sufficient for all real world applications since the majority of A/Ds and D/As are 16 bits or less, and certainly not greater than 24 bits. The 56-bit accumulation internal to the data ALU provides 336 dB of internal dynamic range so that there will be no loss of precision due to intermediate processing.

The data shifter/limiters provide special post processing on data read from the ALU accumulator registers A and B out to the XD or YD data buses. Two independent shifter/limiter operations are used — one for XD and one for YD.

The data shifters are capable of shifting data one bit to the left or one bit to the right as well as passing the data unshifted. Each data shifter has a 24-bit output with overflow indication. The data shifters are controlled by the scaling mode bits in the status register. These shifters permit dynamic scaling of fixed point data without modifying the program code. This permits block floating-point algorithms to be implemented in a regular fashion. FFT routines for example, can use this feature to selectively scale each butterfly pass.

Saturation arithmetic is provided to minimize errors due to overflow. Overflow is said to occur when a source operand requires more bits for accurate representation than there are available in the destination.

For example, if the source operand were 01.100 (+ 1.5 decimal) and the destination register were only four bits, the destination register would contain 1.100 (− 1.5 decimal) after the transfer assuming signed fractional arithmetic. This is clearly in error. Overflow has occurred. To minimize the error due to overflow it is preferrable to write the maximum (or 'limited') value the destination can assume in the destination. In the example, the 'limited' value would be 0.111 (+ 0.875 decimal). This is clearly closer to + 1.5 than − 1.5 and therefore introduces less error.

In the DSP56001 the data ALU accumulators A and B have extension bits. Therefore, when the extension bits are in use and either A or B is the source being read over XD or YD, limiting will occur. In the DSP56001 the limiters place a 'limited' value on XD or YD. Limiting is performed on the content of A or B after the content has been shifted in the shifter. There are two limiters. This allows two word operands to be limited independently in the same instruction cycle. The two data limiters can also be combined to form one 48-bit data limiter for long word operands. If the contents of the selected source accumulator can be represented in the destination operand size without overflow (that is, the accumulator extension register is not in use) the data limiter is disabled and the operand is not modified. If the content of the selected source accumulator cannot be represented without overflow in the destination operand size, the data limiter will substitute a 'limited' data value having maximum magnitude and the same sign as the source accumulator: 7FFFFF for 24-bit or 7FFFFF FFFFFF for 48-bit positive numbers, 800000 for 24-bit or 800000 000000 for 48-bit negative numbers. The shifted value in the accumulator register itself is not changed and can be reused within the Data ALU. When limiting does occur a flag is set and latched.

ADDRESS ALU

The address ALU performs all of the address storage and effective address calculations necessary to address data operands in memory. It implements three types of arithmetic — linear, modulo, and reverse carry. This ALU operates in parallel with other chip resources to minimize address generation overhead. The address ALU contains eight address registers (R0-R7), eight offset registers (N0-N7), and eight modifier registers (M0-M7). The Rn are 16-bit registers which may contain an address or data. Each Rn register may be accessed for output to the XA, YA, and PA address buses. The Nn and Mn registers are 16-bit registers which are normally used to control updating of the Rn registers.

Address ALU registers may be read or written via the global data bus as 16-bit operands. The Address ALU has two module arithmetic units which can generate two 16-bit addresses every instruction cycle — one for any two of the XA, YA, or PA buses. The address ALU can directly address 65,536 locations on the XA bus, 65,536 locations on the YA bus, and 65,536 locations on the PA bus — a total capability of 196,608 24-bit data words.

MEMORIES

Three independent memory spaces of the DSP56001, X Data, Y Data, and Program, are shown in Figure 3. The

memory spaces are configured by control bits in the Operating Mode Register (Figure 8). MA and MB control the Program Memory map and select the reset vector address. DE controls the X and Y Data Memory maps, enabling the internal X and Y data ROMs.

X Data Memory

On-chip X data RAM is a 24-bit wide internal memory which occupies the lowest 256 locations in X memory space. The on-chip X data ROM occupies locations 256 through 511 in X data memory space when enabled by setting DE = 1 in the Operating Mode Register. The X data ROM is factory programmed with positive Mu-law and A-law expansion tables (see **Appendix II**) useful in telecommunication applications. The on-chip peripherals occupy the top 64 locations. Addresses are received from the XA bus and data transfers to the data ALU occur on the XD bus. X memory may be expanded off chip.

Y Data Memory

On-chip Y data RAM is a 24-bit wide internal memory which occupies the lowest 256 locations in Y memory space. The on-chip Y data ROM occupies locations 256 through 511 in Y data memory space when enabled by setting DE = 1. The Y data ROM is factory programmed with a full sine wave table (see **Appendix III**) useful for FFTs, DFTs, and waveform generation. The off-chip peripherals are optimally mapped into the top 64 locations. Addresses are received from the YA bus and data transfers to the data ALU occur on the YD bus. Y memory may be expanded off chip.

Program Memory

On-chip program memory consists of a 512 location by 24-bit RAM which is enabled by the MA and MB bits in the Operating Mode register. Addresses are received from the program control logic (usually the program counter).

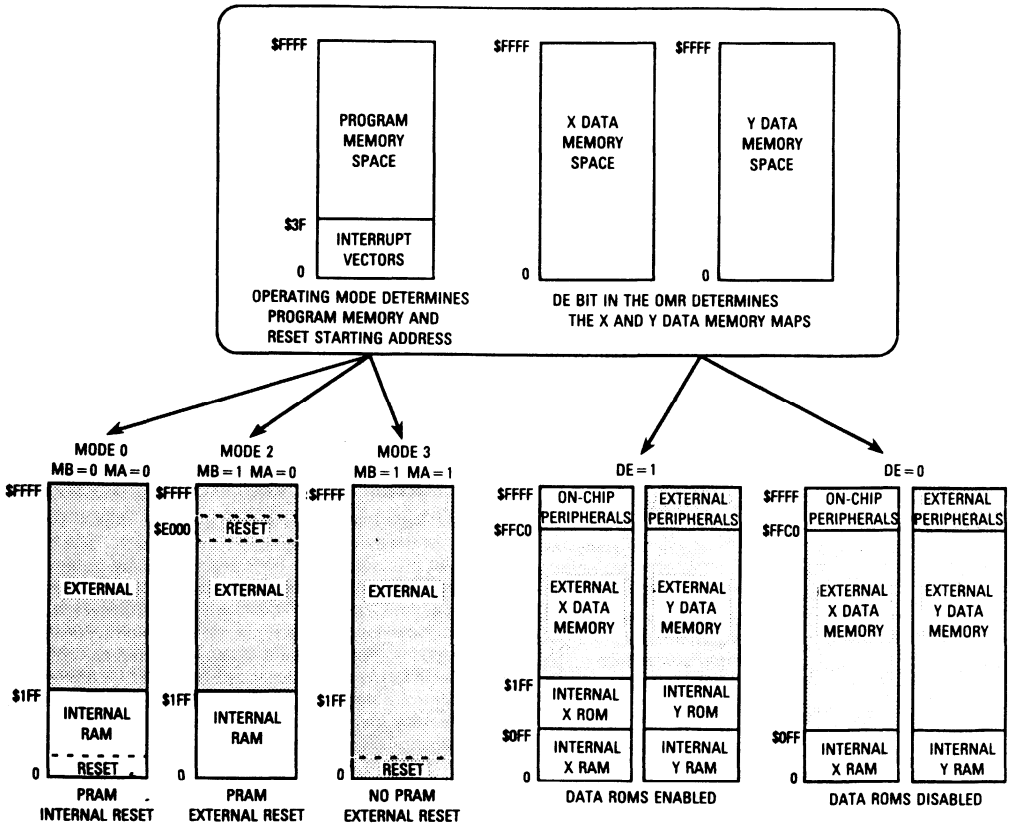


Figure 3. DSP56001 Memory Map

Program memory may be written using MOVEM instructions. The interrupt vectors for the on-chip resources are located in the bottom 64 locations of program memory. Program memory may be expanded off-chip.

Bootstrap ROM

Bootstrap ROM is a 32 location by 24-bit factory programmed ROM which is used only in the bootstrap mode, Operating Mode 1. The Bootstrap ROM is not accessible by the user and is disabled in normal operating modes. See **Appendix I** for a full description of the bootstrap feature of the DSP56001.

PROGRAM CONTROLLER

The program controller performs instruction prefetch, instruction decoding, hardware DO loop control, and exception processing. It contains six directly addressable registers — the program counter (PC), loop address (LA), loop count (LC), status register (SR), operating mode register (OMR), and stack pointer (SP) — and a 15 level by 32-bit system stack memory. The 16-bit PC can address 65,536 locations in program memory space.

INPUT/OUTPUT

The I/O capability of the DSP56001 is extensive and advanced. This I/O structure facilitates interfacing into a variety of system configurations including multiple DSP56001 systems with or without a host processor, global bus systems with bus arbitration, and many serial configurations, all with minimal glue logic (see Figure 4). Each I/O interface has its own control, status, and data registers, and is treated as memory-mapped I/O by the DSP56001. Each interface has several dedicated interrupt vector addresses and control bits to enable/disable interrupts. This minimizes the overhead associated with servicing the device since each interrupt source can have its own service routine. The interrupt vectors can be programmed to one of three maskable priority levels.

Specifically, the I/O structure consists of an extremely flexible expansion port, Port A, and 24 additional I/O pins. These pins may be used as general purpose I/O pins called Port B and Port C, or allocated to an on-chip peripheral under software control. Three on-chip peripherals are provided on the DSP56001 — an 8-bit parallel host MPU/DMA interface, a serial communications interface (SCI), and a synchronous serial interface (SSI). Port B is a 15-bit I/O interface which may be used as general purpose I/O pins or as host MPU/DMA interface pins. Port C is a 9-bit I/O interface which may be used as general purpose I/O pins or as SCI and SSI serial interface pins. These interfaces are described in the following paragraphs.

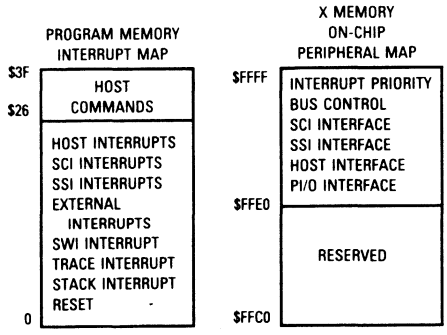


Figure 4. Interrupt and Peripheral Register Memory Maps

Expansion Port (Port A)

DSP56001 expansion port is designed to synchronously interface over a common 24-bit data bus with a wide variety of memory and peripheral devices. They include high speed static RAMs, slower memory devices, as well as other DSPs and MPUs in master/slave configurations. This is possible because the expansion bus timing is programmable. The expansion bus timing is controlled by a bus control register (BCR). The BCR controls the timing of the bus interface signals $\overline{RD}$ and $\overline{WR}$, and the data output lines. Each of the four memory spaces — X data, Y data, program data, and I/O, has its own 4-bit BCR which can be programmed for up to 15 WAIT states (one WAIT state is equal to a clock period or equivalently one-half of an instruction cycle). In this way external bus timing can be tailored to match the speed requirements of the different memory spaces.

General Purpose I/O (Port B, Port C)

Each Port B and C pin may be programmed as a general purpose I/O pin or as a dedicated on-chip peripheral pin under software control. A 9-bit port control register, PCC, is associated with port C which allows each port pin to be programmed for one of these two functions. The port control register associated with port B, PBC, contains only one bit which programs all 15 pins. Also associated with each general purpose port is a data direction register which programs the direction of each pin, and a data register for data I/O. Note that all these registers are read/write making the use of bit manipulation instructions extremely effective.

HOST INTERFACE

The Host Interface is a byte-wide full duplex parallel port which may be connected directly to the data bus of a host processor. The host processor may be any of a number of industry standard microcomputers or microprocessors, another DSP, or DMA hardware. The DSP56001 Host Interface has an 8-bit bidirectional data bus H0-H7 (PB0-PB7) and seven dedicated control lines HA0, HA1, HA2, HR/$\overline{W}$, $\overline{HEN}$, $\overline{HREQ}$, and $\overline{HACK}$ (PB9-PB15) to control data transfers. The Host Interface appears as a memory mapped peripheral occupying eight bytes in the *host processor* address space. Separate transmit and receive data registers are double-buffered to allow the DSP56001 and host processor to transfer data efficiently at high speed. Host processor communication with the Host Interface is accomplished using standard host processor data move instructions and addressing modes. Handshake flags are provided for polled or interrupt driven

data transfers with the host processor. DMA hardware may be used with the handshake flags to transfer data without host processor intervention.

One of the most innovative features of the Host Interface is the Host Command feature. With this feature the host processor can issue vectored exception requests to the DSP56001. The host may select any one of 32 DSP56001 exception routines to be executed by writing a Vector Address Register in the Host Interface. This flexibility allows the host programmer to execute up to 32 preprogrammed functions inside the DSP56001. For example, host exceptions can allow the host processor to read or write DSP56001 registers, X, Y, or program memory locations, force exception handlers for SSI, SCI, $\overline{IRQA}$, and $\overline{IRQB}$ exception routines, and perform control and debugging operations if the appropriate exception routines are implemented in the DSP56001 to do these tasks.

SERIAL COMMUNICATION INTERFACE

The Serial Communications Interface (SCI) provides a full-duplex port for serial communication to other DSPs, microprocessors, or peripherals such as modems. The communication can be either direct or via RS232C-type lines. This interface uses three dedicated pins — transmit data (TXD), receive data (RXD), and SCI serial clock (SCLK). It supports industry standard asynchronous bit rates and protocols as well as high speed (up to 2.5 Mbits/sec) synchronous data transmission. The asynchronous protocols include a multidrop mode for master/slave operation. The Serial Communication Interface consists of separate transmit and receive sections whose operations can be asynchronous with respect to each other. A programmable baud rate generator is included to generate the transmit and receive clocks. An enable and interrupt vector have been included so that the baud rate generator can function as a general purpose timer when it is not being used by the SCI peripheral.

SYNCHRONOUS SERIAL INTERFACE (SSI)

The Synchronous Serial Interface (SSI) is an extremely flexible full-duplex serial interface which allows the DSP56001 to communicate with a variety of serial devices. These include one or more industry standard codecs, other DSPs, microprocessors, and peripherals. The following characteristics of the SSI interface can be independently defined by the user — the number of bits per word, the protocol or mode, the clock, and the transmit/receive synchronization. There are three modes which can be selected. They are the Normal, On-Demand, and Network modes. The Normal mode is typically used to interface with devices on a regular or periodic basis. In this mode the SSI interface functions with one data word of I/O per frame. The On-Demand mode is a data driven mode. There are no timeslots defined. This mode is intended to be used to interface to devices on a non-periodic basis. The Network mode provides time slots in addition to a bit clock and frame synchronization pulse. The SSI functions with from 2 to 32 words of I/O per frame in the Network mode. This mode is typically used in star or ring Time Division Multiplex (TDM) networks with other DSP56000s and/or codecs. The clock can be programmed to be continuous or gated. Since the transmitter and receiver sections of the SSI interface are independent they may be programmed to be synchronous (use a common clock) or asynchronous with respect to each other. The SSI interface supports a subset of the Motorola SPI interface. The SSI requires three to six pins depending on the operating mode selected. A matrix of SSI operating modes and typical applications is provided in Table 1.

Table 1. SSI Operating Modes

Mode (Protocol)	Serial Clock	Relative Tx-Rx Timing	Typical Applications
Normal	Continuous	Asynchronous	Asynchronous Codec
Normal	Continuous	Synchronous	Synchronous Codecs
Normal	Gated	Asynchronous	DSP-to-DSP
Normal	Gated	Synchronous	DSP-to-A/D and D/A
On-Demand	Continuous	Asynchronous	DSP-to-MCU
On-Demand	Continuous	Synchronous	P-to-S and S-to-P Conversion
On-Demand	Gated	Asynchronous	DSP-to-DSP
On-Demand	Gated	Synchronous	DSP-to-SPI Peripherals
Network	Continuous	Asynchronous	TDM Codec Networks
Network	Continuous	Synchronous	TDM DSP Networks
Network	Gated	Asynchronous	—
Network	Gated	Synchronous	—

PROGRAMMING MODEL DESCRIPTION

The programmer can view the DSP56001 architecture as three execution units operating in parallel. The three execution units are the Data ALU, Address ALU, and Program Controller. It was possible to make the programming model like that of conventional MPUs and eliminate the need to refer to the detailed chip architecture when programming the DSP56001 because the parallel execution units make the pipeline virtually invisible. The programming model is shown in Figure 5 and is described in the following paragraphs.

DATA ALU

The data ALU features 24-bit input/output data registers which can be concatinated to handle 48-bit data, two 56-bit accumulators, programmable scaling, and saturation arithmetic.

DATA ALU INPUT REGISTERS (X1, X0, Y1, Y0)

X1, X0, Y1, and Y0 are four 24-bit general purpose data registers. They may be treated as four independent 24-bit registers or as two 48-bit registers called X and Y developed by the concatenation of X1:X0 and Y1:Y0 respectively. The register with the highest number is the most significant word. The registers serve as input pipeline registers between the XD and YD data buses and the multiply-accumulator unit (MAC). They are used as data ALU source operands and allow new operands to be loaded for the next instruction while the register contents are used by the current instruction. They may also be read back out to the appropriate data bus to implement memory delay operations and save/restore operations for interrupt service routines.

DATA ALU ACCUMULATOR REGISTERS (A2, A1, A0, B2, B1, B0)

The six data ALU registers A2, A1, A0, B2, B1, and B0 form two general purpose 56-bit accumulators, A and B, developed by the concatenation of A2:A1:A0 and B2:B1:B0 respectively. These registers are used for arithmetic calculations and data manipulation. The four registers A1, A0, B1, and B0 are 24 bits wide and the two registers A2 and B2 are 8 bits wide. All of these registers are treated as word operands. The register with the highest number is the most-significant word in the accumulator; the register with the lowest number is the least-significant word.

These accumulators are 48 bits long with 8-bit extensions to accommodate word growth in vector arithmetic. The registers A2 and B2 are called accumulator extension registers. Automatic sign extension is provided when writing to the 56-bit accumulators A or B with a 48- or 24-bit operand. The low-order portion will be automatically zeroed when a 24-bit operand is written to form a valid 56-bit operand. The registers may also be written without sign extension or zero fill by specifying the individual register name.

When the accumulator registers A or B are read, they may be optionally scaled one bit left or one bit right for block floating-point arithmetic. Reading the A or B accumulators over XD and YD is protected against overflow by substituting a limiting constant for the data that is being transferred. The content of A or B is not affected should limiting occur; only the value transfered over XD and YD is limited. This overflow protection is performed after the content of the accumulator has been shifted according to the scaling mode. Note that only when A or B as opposed to A0, A1, A2, B0, B1, or B2, is specified as the source for a parallel data move over XD, YD will shifting and limiting be performed. The accumulator registers serve as pipeline registers between the MAC unit and the XD and YD data buses. They are used as both data ALU source and destination operands.

ADDRESS ALU

The programmer's model for the address ALU consists of three banks of register files — address register files, offset register files, and modifier register files. They provide all the registers necessary to generate address register indirect effective addresses.

Address Register Files (R0-R3 and R4-R7)

The eight address registers, R0-R7, are 16 bits wide and may contain addresses or general purpose data. The 16-bit address in a selected address register is used in the calculation of the effective address of an operand. When supporting parallel X and Y data memory moves the address registers must be thought of as separate two files, R0-R3 and R4-R7. The content of an Rn may point to data directly or may be pre- or post-updated according to the addressing mode selected. Modifier registers, Mn, are always used if an Rn is updated. Offset registers, Nn, are used for the update by offset addressing modes. The address register modification is performed by one of the two modulo arithmetic units.

Offset Register Files (N0-N3 and N4-N7)

The eight offset registers, N0-N7, are 16 bits wide and may contain offset values used to increment and decrement address registers in address register update calculations or they may be used for 16-bit general purpose storage. For example, the contents of an offset register may be used to step through a table at some rate (e.g., five locations per step for waveform generation), or may specify the offset into a table or the base of the table for indexed addressing. Each address register, Rn, has its own offset register, Nn, associated with it.

Modifier Register Files [M0-M3 and M4-M7]

The eight modifier registers, M0-M7, are 16 bits wide. The content of Mn defines the type of address arithmetic to be performed for addressing mode calculations. The address ALU supports linear, modulo, and reverse carry arithmetic types for all address register indirect addressing modes. For the case of modulo arithmetic, the content of Mn also specifies the modulus. Each address register, Rn, has its own modifier register, Mn, associated with it. Each modifier register is set to $FFFF on processor reset which specifies linear arithmetic as the default type for address register update calculations.

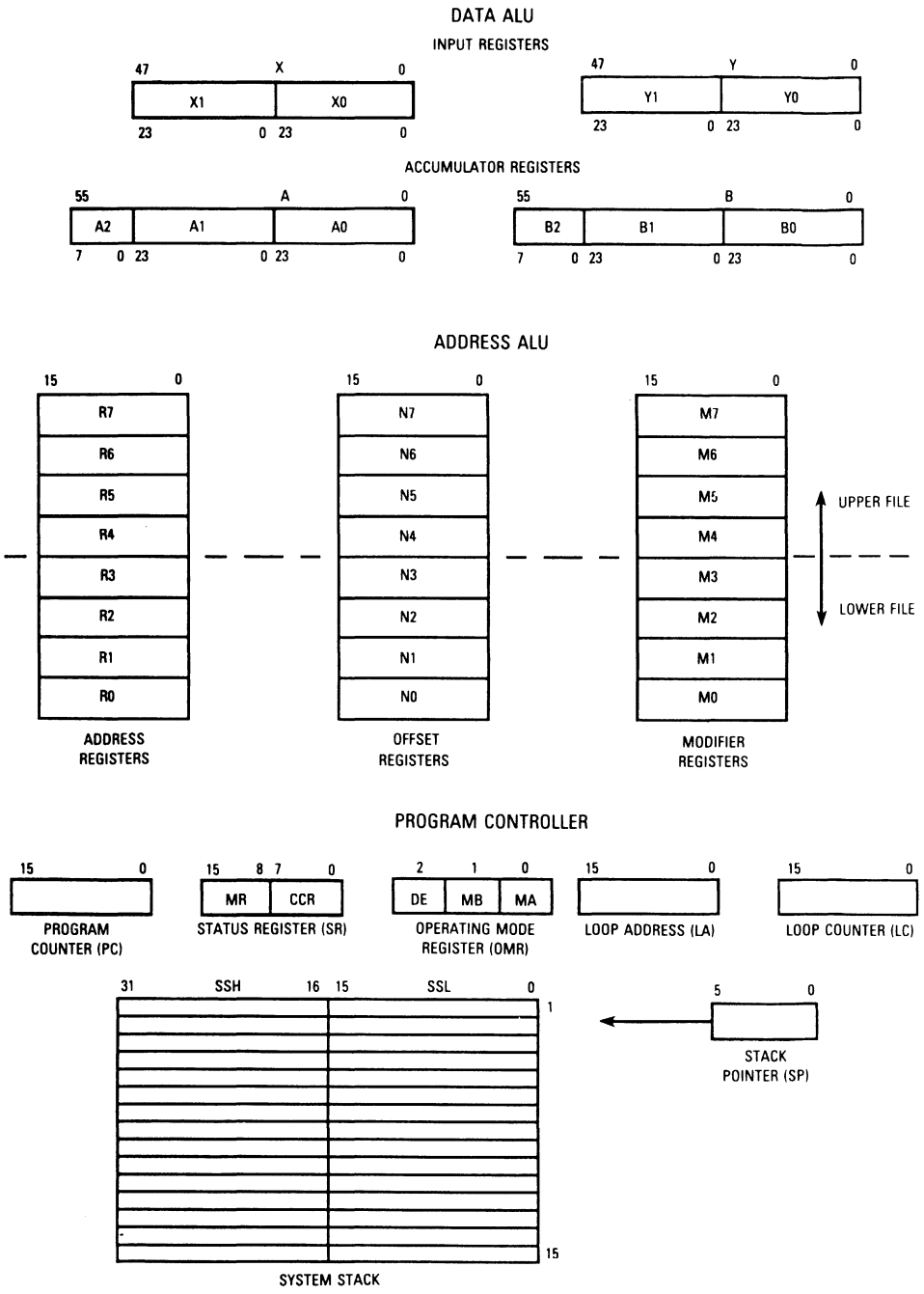


Figure 5. DSP56001 Programming Model

PROGRAM CONTROLLER

The program controller features registers (LA and LC) dedicated to supporting the hardware DO loop instruction in addition to the standard program flow control resources such as a program counter, complete status register, and system stack. All registers are read/write to facilitate system debug.

Program Counter (PC)

This 16-bit register contains the address of the next location to be fetched from program memory space. This special purpose address register is stacked when program looping is initiated, or when a jump to subroutine (JSR) is performed, and when interrupts occur, except for fast, 'no overhead', interrupts.

Status Register (SR)

The status register is a 16-bit register consisting of an 8-bit mode register (MR) and an 8-bit condition code register (CCR). SR is stacked when program looping is initialized, or when a jump to subroutine (JSR) is performed, and when interrupts occur, except for fast, no overhead, interrupts. The status register format is shown in Figure 6.

MR is a special purpose control register which defines the current system state of the processor. The MR bits are affected by processor reset, exception processing, the DO, ENDDO, RTI, and SWI instructions, and by instructions which directly reference the MR register — ORI and ANDI.

CCR is a special purpose control register which defines the current user state of the processor at any given time. The CCR bits are affected by data ALU operations and by instructions which directly reference the CCR register — ORI and ANDI. The CCR bits are not affected by parallel move operations unless data limiting occurs when reading the A or B accumulators.

Loop Counter (LC)

The loop counter is a special 16-bit counter used to specify the number of times to repeat a hardware program loop. This register is stacked by a DO instruction and unstacked by end of loop processing or by execution of an ENDDO instruction. The loop counter may be read under program control. This allows the number of times a loop has been executed to be monitored during execution.

Loop Address Register (LA)

The content of the loop address register indicates the location of the last instruction word in a program loop. This register is stacked by a DO instruction and unstacked by end of loop processing or by execution of an ENDDO instruction.

System Stack (SS)

The system stack is a separate internal memory which stores the PC and SR for subroutine calls and long interrupts. The stack will also store the LC and LA registers in addition to the PC and SR registers for program looping. The SS is in stack memory space and its address is always inherent and implied by the current instruction. The system stack memory is 32 bits wide and 15 locations 'deep'.

When a subroutine call or long interrupt occurs, the content of the PC and SR are stored (pushed) on the 'top' location in the system stack. When a return from subroutine occurs, the content of the 'top' location in the

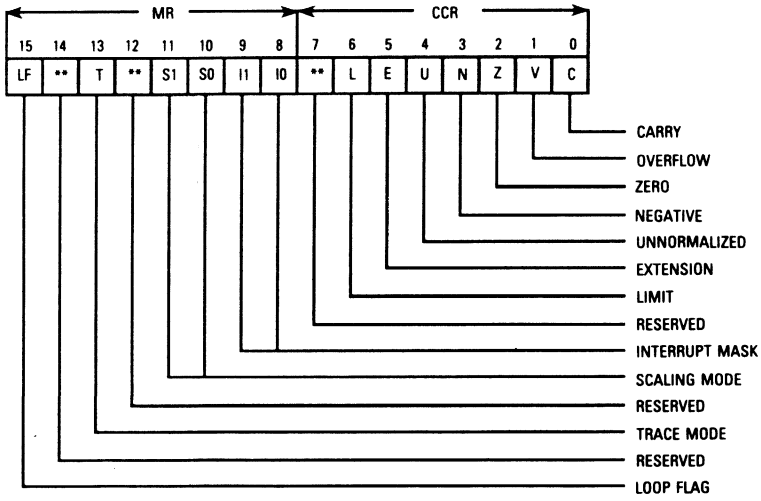


Figure 6. Status Register Format

system stack are transferred (pulled) to the PC only. When a return from interrupt occurs, the content of the 'top' location in the system stack are transferred (pulled) to both the PC and SR.

The interrupt subsystem of the DSP56001 is vector based and prioritized. Interrupt vectors point to two consecutive locations in program memory. If one of the two words fetched by the interrupt controller is a jump to subroutine instruction, a long interrupt routine is formed, and a context switch is performed using the stack. If neither interrupt instruction word causes a change of control flow, then the two interrupt instruction words fetched constitute a fast interrupt routine. The fast interrupt routine provides exception processing with no overhead. This mechanism is commonly used to move data between memory and an I/O device.

The system stack is also used to implement no-overhead nested hardware DO loops. Each stack location can be addressed as two separate 16-bit registers, system stack high (SSH) and system stack low (SSL). This facilitates creating software stacks for unlimited nesting.

Stack Pointer (SP)

The stack pointer register (SP) is a 6-bit register that indicates the location of the top of the system stack and the status of the stack (underflow, empty, full, and overflow conditions). The stack pointer is referenced implicitly by some instructions (DO, REP, JSR, RTI, etc.) or directly by the MOVEC instruction. The stack pointer register format is shown in Figure 7.

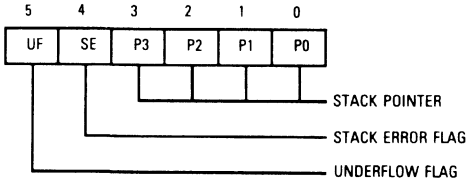


Figure 7. Stack Pointer Format

Operating Mode Register (OMR)

The operating mode register (OMR) is a 3-bit register which defines the current operating mode of the processor, i.e., the memory maps for program and data memories as well as the startup procedure. The OMR bits are only affected by processor reset and by instructions which directly reference the OMR. During processor reset the chip operating mode bits, MB and MA, will be loaded from the external mode select A, B, pins. The Data ROM Enable bit (DE) will be cleared, disabling the X and Y on-chip lookup table ROMs. Figure 3 shows the effect of the OMR on the DSP56001 memory maps. The operating mode register format is shown in Figure 8. Table 2 summarizes the DSP56001 operating modes. Tables 3 and 4 show the program and data memory spaces.

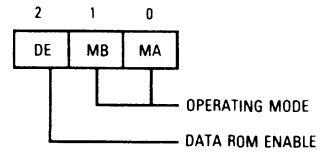


Figure 8. Operating Mode Register Format

Table 2. Operating Mode Summary

Operating Mode	M B	M A	Description
0	0	0	PRAM enabled, Reset at $0000 (internal).
1	0	1	Special Bootstrap mode, after PRAM loading mode 2 is automatically selected.
2	1	0	PRAM enabled, Reset at $E000 (external).
3	1	1	PRAM disabled, Reset at $0000 (external).

Table 3. Program Memory Space

Operating Mode	M B	M A	Program Memory Space Map
0 & 2	X	0	internal RAM: $0000-$01FF external: $0200-$FFFF
3	X	1	external: $0000-$FFFF

Table 4. Data Memory Space

DROM Enable DE	Y Data Memory Space Map	X Data Memory Space Map
0	internal RAM: $0000-$00FF external: $0100-$FFFF	internal RAM: $0000-$00FF external: $0100-$FFBF on-chip peripherals: $FFC0-$FFFF
1	internal RAM: $0000-$00FF internal ROM: $0100-$01FF external: $0200-$FFFF	internal RAM: $0000-$00FF internal ROM: $0100-$01FF external: $0200-$FFBF on-chip peripherals: $FFC0-$FFFF

INSTRUCTION SET SUMMARY

The DSP56001 instruction set has been designed to be as orthogonal as possible to allow flexible, independent, concurrent control of the data ALU, address ALU, and program control execution units during each instruction cycle. This maximizes throughput and minimizes program storage requirements.

The rich instruction set features DSP oriented instructions such as CMPM, NORM, RND, MACR, SUBL, SUBR, ADDL, ADDR, DO, and REP, which are summarized below.

The instruction set is divided into the following groups:

- Arithmetic
- Logical
- Bit Manipulation
- Loop
- Move
- Program Control

ARITHMETIC INSTRUCTIONS

The arithmetic instructions perform all of the arithmetic operations within the data ALU. They may affect all of the condition code register bits. Arithmetic instructions are register-based so that the data ALU operation indicated by the instruction does not use the X data bus, the Y data bus, or the global data bus. This allows for parallel data movement over the X and Y data buses or over the global data bus during a Data ALU operation. This permits new data to be pre-fetched for use in following instructions, and results calculated by previous instructions to be stored. These instructions execute in one instruction cycle. The destination is either of the 56-bit accumulators. The following are the arithmetic instructions.

ABS	Absolute Value
ADC	Add Long with Carry
ADD	Add
ADDL	Shift Left then Add Accumulators
ADDR	Shift Right then Add Accumulators
ASL	Arithmetic Shift Accumulator Left
ASR	Arithmetic Shift Accumulator Right
CLR	Clear Accumulator
CMP	Compare
CMPM	Compare Magnitude
DIV	Divide Iteration*
MAC	Signed Multiply-Accumulate
MACR	Signed Multiply-Accumulate and Round
MPY	Signed Multiply
MPYR	Signed Multiply and Round
NEG	Negate Accumulator
NORM	Normalize Accumulator Iteration*
RND	Round Accumulator
SBC	Subtract Long with Carry
SUB	Subtract
SUBL	Shift Left then Subtract Accumulators
SUBR	Shift Right then Subtract Accumulators
Tcc	Transfer Conditionally*
TFR	Transfer Data ALU Register
TST	Test Accumulator

*These instructions do not allow parallel data moves.

The CMPM affects the condition code bits according to the results of the subtraction of the absolute values of two operands. This instruction, together with TCC, is useful in determining maxima and minima in blocks of data.

The NORM instruction normalizes the content of an accumulator register and updates the content of the specified address register according to the normalization. This is particularly useful in implementing floating-point routines.

The RND instruction performs convergent rounding on the content of an accumulator register in a manner consistent with the scaling mode operation.

The MACR instruction is one of the most powerful instructions in the instruction set. It performs a signed multiply-accumulate with convergent rounding and allows two parallel data moves in one instruction. These rounding instructions facilitate minimizing the effects of roundoff errors.

The ADDL, ADDR, SUBL, and SUBR, instructions multiply or divide the content of the accumulator register by two before the addition or subtraction operation is performed. They are particularly useful for implementing Radix-2 Decimation In Time (DIT) Fast Fourier Transforms (FFT).

LOGICAL INSTRUCTIONS

The logical instructions perform all of the logical operations within the data ALU. They affect all of the condition code register bits. Logical instructions are register-based. Optional data transfers may be specified with most logical instructions. This allows for parallel data movement over XD, YD, or GD during a Data ALU logical operation. This allows new data to be pre-fetched for use in following instructions, and results calculated in previous instructions to be stored. These instructions execute in one instruction cycle. The destination is either A1 or B1, except for ANDI or ORI. The following are the logical instructions.

AND	Logical AND
ANDI	AND Immediate with Control Register*
EOR	Logical Exclusive OR
LSL	Logical Shift Accumulator Left
LSR	Logical Shift Accumulator Right
NOT	Logical Complement on Accumulator
OR	Logical Inclusive OR
ORI	OR Immediate with Control Register*
ROL	Rotate Accumulator Left
ROR	Rotate Accumulator Right

*These instructions do not allow parallel data moves.

BIT MANIPULATION INSTRUCTIONS

There are two basic groups of bit manipulation instructions. One group tests the state of any single bit in a memory location and then optionally sets, clears, or inverts the bit. The other group tests the state of any single bit in a memory location and jumps (or jumps to subroutine) if the bit is set or clear. The carry bit of the condition code register will contain the result of the bit test for the first group. The following are the bit manipulation instructions. Note that parallel data moves are not allowed with any of these instructions.

BCLR	Bit Test and Clear
BSET	Bit Test and Set

BCHG	Bit Test and Change
BTST	Bit Test on Memory
JCLR	Jump if Bit Clear
JSET	Jump if Bit Set
JSCLR	Jump to Subroutine if Bit Clear
JSSET	Jump to Subroutine if Bit Set

LOOP INSTRUCTIONS

The DO and ENDDO instructions make writing straight line code practically unnecessary. The DO instruction sets up a hardware loop by initiating a program loop, setting up looping parameters and then 'cleans up' the system stack when terminating a loop. Initialization includes saving registers LA and LC used by a program loop on the system stack so that program loops can be nested. The address of the first instruction in a program loop is also saved to allow no-overhead looping. Single instruction DO loops can be implemented. The ENDDO instruction is used to terminate a DO loop prematurely. It is used to 'clean up' the stack. These instructions do not allow parallel data moves. The following are the loop instruction definitions.

DO	Start Hardware Loop
ENDDO	Exit from Hardware Loop

MOVE INSTRUCTIONS

The move instructions perform data movement over XD, YD, and GD data buses as well as the program data bus, PD. Move instructions do not affect the condition code register except the limit bit, L, if limiting is performed when reading Data ALU accumulator registers A or B. The MOVE instruction provides all of the parallel data move operations and can be considered to be a data ALU no-op with parallel moves. The following are the move instructions.

LUA	Load Updated Address
MOVE	Move Data
MOVEC	Move Control Register
MOVEM	Move Program Memory
MOVEP	Move Peripheral Data

PROGRAM CONTROL INSTRUCTIONS

The program control instructions include jumps, conditional jumps, and other instructions which affect the PC and system stack. Program control instructions may affect the condition code register bits as specified in the instruction. Optional parallel data transfers over XD, YD, and GD are not allowed in the program control instructions. The REP instruction repeats the next instruction without refetching the instruction to maximize throughput without resorting to using straight line code. Because the REP instruction is not refetched it is not interruptable. An interruptable repeat instruction can be implemented using a single instruction DO loop. All processor activity is suspended and the oscillator is gated off after a STOP instruction has been executed. When the WAIT instruction is executed internal processing is halted and the processor waits for an interrupt. The STOP and WAIT states are low power states. The following are the program control instructions.

Jcc	Jump Conditionally
JMP	Jump
JScc	Jump to Subroutine Conditionally
JSR	Jump to Subroutine
NOP	No Operation
REP	Repeat Next Instruction
RESET	Reset On-Chip Peripheral Devices
RTI	Return from Interrupt
RTS	Return from Subroutine
STOP	Stop Processing (Low Power Standby)
SWI	Software Interrupt
WAIT	Wait for Interrupt (Low Power Standby)

INSTRUCTION FORMATS

Instructions are one or two words in length. The instruction and its length are specified by the first word of the instruction. The second word may contain information about an operand for the instruction. The assembly language source code for a typical one word instruction is shown below. The source code is organized into four columns.

Opcode	Operands	X Bus Data	Y Bus Data
MAC	X0,Y0,A	X:(R0)+,X0	Y:(R4)+,Y0

The Opcode column typically indicates the Data ALU operation to be performed; it may also specify an Address ALU or Program Control operation. The operands column specifies the operands to be used by the opcode. The X bus data column specifies an optional data transfer over the X bus and the addressing mode to be used. The Y bus data column specifies an optional data transfer over the Y bus and the addressing mode to be used. The memory space qualifiers X:, Y:, P: and L: (long memory space) indicate which memory space is being referenced. The opcode column must always be included in the source code.

The DSP56001 allows parallel processing by the data ALU, address ALU, and program controller. For example, in the instruction word above the DSP56001 will perform the designated ALU operation (data ALU), the data transfers specified with address register updates (address ALU), and will also decode the next instruction and fetch an instruction word from program memory (program controller), all in one instruction cycle. In addition, the program controller may be processing an active hardware DO loop. When an instruction is more than one word in length, an additional instruction execution cycle may be required. Most operations involving the data ALU are register-based (that is, all operands are in data ALU registers) and therefore do not utilize the data buses. This allows the programmer to keep each execution unit busy by specifying memory accesses in parallel over the XD, YD, or GD buses. An instruction which is memory-oriented (such as a bit manipulation instruction) or an instruction that causes a control flow change (such as a jump) does not allow parallel data moves during its execution.

ADDRESSING MODES

The addressing modes are grouped into three categories — register direct, address register indirect, and special. These addressing modes are summarized in Table 5. All address calculations are performed in the address ALU to minimize execution time and loop overhead. Addressing modes specify whether the operand(s) is (are) in a register, memory, or encoded in the instruction (as immediate data) and provide the specific addresses of the operand.

The register direct addressing mode can be subclassified according to the specific register addressed. The data registers include X1, X0, Y1, Y0, X, Y, A2, A1, A0, B2, B1, B0, A, and B. The control registers include SR, OMR, SP, SSH, SSL, LA, LC, CCR, and MR.

Address register indirect modes use an address register, Rn, to point to locations in memory. The content of Rn is the effective address (ea) except in the indexed by offset mode where the ea is Rn + Nn. Address register indirect modes use a modifier register, Mn, to specify the type of arithmetic to be used to update Rn. If a mode using an offset is specified an offset register, Nn, is also used for the update. The Nn and Mn registers are assigned to the Rn with the same n. Thus the assigned register sets are R0;N0;M0, R1;N1;M1, R2;N2;M2, R3;N3;M3, R4;N4;M4, R5;N5;M5, R6;N6;M6, and R7;N7;M7. This structure is unique and extremely powerful in general, and particularly powerful in setting up DSP oriented data structures. All address register indirect modes use at least one set of address registers, and the XY memory reference uses two sets of address registers, one set for X memory space and one set for Y memory space.

The special addressing modes include immediate and absolute modes as well as implied references to the PC, system stack, and program memory.

ADDRESS MODIFIERS [Mn]

The address modifiers allow the DSP Address ALU to support linear, reverse-carry, and modulo address arithmetic for all address register indirect modes. These special address arithmetic types allow the creation of data structures in memory for FIFOs (queues), delay lines, circular buffers, stacks and bit-reversed FFT buffers. Data is manipulated by updating address registers rather than moving large blocks of data. The content of the address modifier register, Mn, defines the type of address arithmetic to be performed for addressing mode calculations.

Table 5. Addressing Modes Summary

Addressing Mode	Modifier MMMM	Operand Reference								
		S	C	D	A	P	X	Y	L	XY
Register Direct										
Data or Control Register	No	x	x	x						
Address Register	No				x					
Address Modifier Register	No				x					
Address Offset Register	No				x					
Address Register Indirect										
No Update	Yes					x	x	x	x	x
Postincrement by 1	Yes					x	x	x	x	x
Postdecrement by 1	Yes					x	x	x	x	x
Postincrement by Offset Nn	Yes					x	x	x	x	x
Postdecrement by Offset Nn	Yes					x	x	x	x	
Indexed by Offset Nn	Yes					x	x	x	x	
Predecrement by 1	Yes					x	x	x	x	
Special										
Immediate Data	No					x				
Absolute Address	No					x	x	x	x	
Immediate Short Data	No					x				
Short Jump Address	No					x				
Absolute Short Address	No					x	x	x	x	
I/O Short Address	No						x	x		
Implicit	No	x	x			x				

Where:
MMMM = Address Modifier
S = Stack Reference
C = Program Controller Register Reference
D = Data ALU Register Reference
A = Address ALU Register Reference
P = Program Memory Reference
X = X Memory Reference
Y = Y Memory Reference
L = L Memory Reference
XY = XY Memory Reference

For the case of modulo arithmetic, the content of Mn also specifies the modulus. The three types of arithmetic are discussed below.

Linear Arithmetic [Mn = $FFFF]

The address modification is performed using normal 16-bit (modulo 65,536) linear arithmetic (2's complement). A 16-bit offset, Nn, may be used in the address calculations. The range of values may be considered as signed (Nn from −32,768 to +32,767) or unsigned (Nn from 0 to +65,535).

Reverse-Carry Arithmetic [Mn = $0000]

The address modification is performed by propagating the carry in the reverse direction, that is, from the most-significant bit (MSB) to the least-significant bit (LSB). This is equivalent to bit-reversing (i.e., redefining the MSB as the LSB and the next MSB as bit 1, etc.) the content of Rn and the offset value Nn, adding normally and then bit-reversing the result. If the (Rn) + Nn addressing mode is used with this address modifier type, and Nn contains the value two to the power of k-1 (2^{k-1}), then post-incrementing by +Nn is equivalent to incrementing Rn by 1 and bit-reversing the k LSBs of Rn. This address arithmetic is useful for performing 2^k point Fast Fourier Transforms (FFTs). The range of values for Nn is 0 to +65,535. This allows bit-reversed addressing for FFTs having up to 65,536 points.

As an example, consider a 1,024 point FFT (k = 10) with real data stored in X memory and imaginary data stored in Y memory. Then Nn would contain the value 512 and postincrementing by +Nn would generate the address sequence 0, 512, 256, 768, 128, 640, ... This is the scrambled FFT data order for sequential frequency points from 0 to 2pi. The base address must have at least k zeros so that the reverse-carry modifier also works when the base address of the FFT data buffer is a multiple of 2_k, such as 2048, 3072, in our example. The use of addressing modes other than postincrement by +Nn is possible but may not provide a useful result.

Modulo Arithmetic [Mn = modulus − 1]

The address modification is performed modulo M, where M ranges from 2 to +32,768. Modulo M arithmetic causes the address register value to remain within an address range of size M defined by a lower and upper address boundary. The value m = M-1 is stored in the modifier register Mn. The lower boundary (base address) value must have zeroes in the k LSBs, where $2^k \geq M$, and therefore must be a multiple of 2^k. The upper boundary is the lower boundary plus the modulo size minus one (base address plus M-1). For example, to create a circular buffer of 21 stages, M is 21 and the lower address boundary must have its five least-significant bits equal to zero ($2^k \geq 21$, thus $k \geq 5$). The Mn register is loaded with the value 20. The lower boundary may be chosen as 0, 32, 64, 96, 128, 160, etc. The upper boundary of the buffer is then the lower boundary plus 20. The address pointer is not required to start at the lower address boundary or end on the upper address boundary; it may initially point anywhere within the defined modulo address range. Note that neither the lower nor the upper boundary of the modulo region is stored; only the size of the modulo region is stored in Mn. Assuming the (Rn) + indirect addressing mode, if the address register pointer increments past the upper boundary of the buffer (base address plus M-1) it will wrap around to the base address (lower boundary). Alternatively, assuming the (Rn) − indirect addressing mode, if the address decrements past the lower boundary (base address) it will wrap around to the base address plus M-1 (upper boundary).

If an offset, Nn, is used in the address calculations, the 16-bit value |Nn| must be less than or equal to M. The range of values for Nn is −32,768 to +32,767. The modulo arithmetic unit will automatically wrap the address pointer around by the required amount. This type of address modification is useful in creating circular buffers for FIFOs (queues), delay lines, and sample buffers up to 32,768 words long. It is also useful for decimation, interpolation, and waveform generation.

APPENDIX I
BOOTSTRAP MODE — OPERATING MODE 1

The bootstrap feature of the DSP56001 consists of four special on-chip modules: the 512 words of PRAM, a 32-word bootstrap ROM, the bootstrap control logic and the bootstrap firmware program.

BOOTSTRAP ROM

This 32-word on-chip ROM has been factory programmed to perform the actual bootstrap operation from the memory expansion port (Port A) or from the Host Interface. Users have no access to the bootstrap ROM other than through the bootstrap process. Control logic will disable the bootstrap ROM during normal operations.

BOOTSTRAP CONTROL LOGIC

The bootstrap mode control logic is activated when the DSP56001 is in Operating Mode 1. The control logic maps the bootstrap ROM into program memory space as long as the DSP56001 remains in Operating Mode 1. The bootstrap firmware changes operating modes when the bootstrap load is completed.

When the DSP56001 exits the reset state in Mode 1, the following actions occur.

1. The control logic maps the bootstrap ROM into the internal DSP program memory space starting at location $0000.

2. The control logic forces the user PRAM to be write-only memory during the bootstrap loading process.

3. Program execution begins at location $0000 in the bootstrap ROM.

   The bootstrap ROM program is able to perform the load of PRAM through either the memory expansion port from a byte-wide external memory, or through the Host Interface.

4. The bootstrap ROM program executes the following sequence to end the bootstrap operation and begin user program execution.

   A. Enter Operating Mode 2 by writing to the OMR. This action will be timed to remove the bootstrap ROM from the program memory map, and re-enable read/write access to the PRAM.

   B. The change to Mode 2 is timed exactly to allow the boot program to execute a NOP then a JMP #00 and begin execution of the user's program at location $0000.

The user may also select the bootstrap mode by writing into the OMR. This will cause the bootstrap ROM to be mapped into the program address space after a delay to allow execution of a NOP then a JMP #00. This technique allows the DSP56001 user to reboot the system (with a different program if desired). Steps 1 and 2 below detail this technique.

1. From any operating mode, program the OMR to Operating Mode 1. This begins a timed operation to map the bootstrap ROM into the program address space.

2. This delay is exactly timed to allow the DSP program to execute a NOP then a JMP #00 and begin the bootstrap process as described above in steps 1-4.

BOOTSTRAP FIRMWARE PROGRAM

Bootstrap ROM contains the bootstrap firmware program that performs initial loading of the DSP56001 PRAM.

The program is written in DSP56000/DSP56001 assembly language. It contains two separate methods of initailizing the PRAM: loading from a byte-wide memory starting at location $C000 or loading through the Host Interface. The particular method used is selected by the level of program memory location $C000, bit 23.

If location P:$C000, bit 23 is read as a one, the external bus version of the bootstrap program will be selected. Typically, a byte wide EPROM will be connected to the DSP56001 Address and Data Bus as shown in Figure A-2. The data contents of the EPROM must be organized as shown below.

Address of External Byte Wide P Memory	Contents Loaded to Internal PRAM at:	
P:$C000	P:0000	low byte
P:$C001	P:0000	mid byte
P:$C002	P:0000	high byte
.	.	
.	.	
.	.	
P:$C5FD	P:01FF	low byte
P:$C5FE	P:01FF	mid byte
P:$C5FF	P:01FF	high byte

If location P:$C000, bit 23 is read as a zero, the Host Interface version of the bootstrap program will be selected. Typically a host microprocessor will be connected to the DSP56001 Host Interface. The host microprocessor must write the host interface registers TXH, TXM, and then TXL with the desired contents of PRAM from location P:$0000 up to P:$01FF. If less than 512 words are to be loaded, the host programmer can exit the bootstrap program and force the DSP56001 to begin executing at location P:0000 by setting HF0 = 1 in the host interface. In most systems, the DSP56001 response is so fast that handshaking between the DSP56001 and the host is not necessary.

The bootstrap program is shown in flowchart form in Figure A-1 and in assembler listing format below.

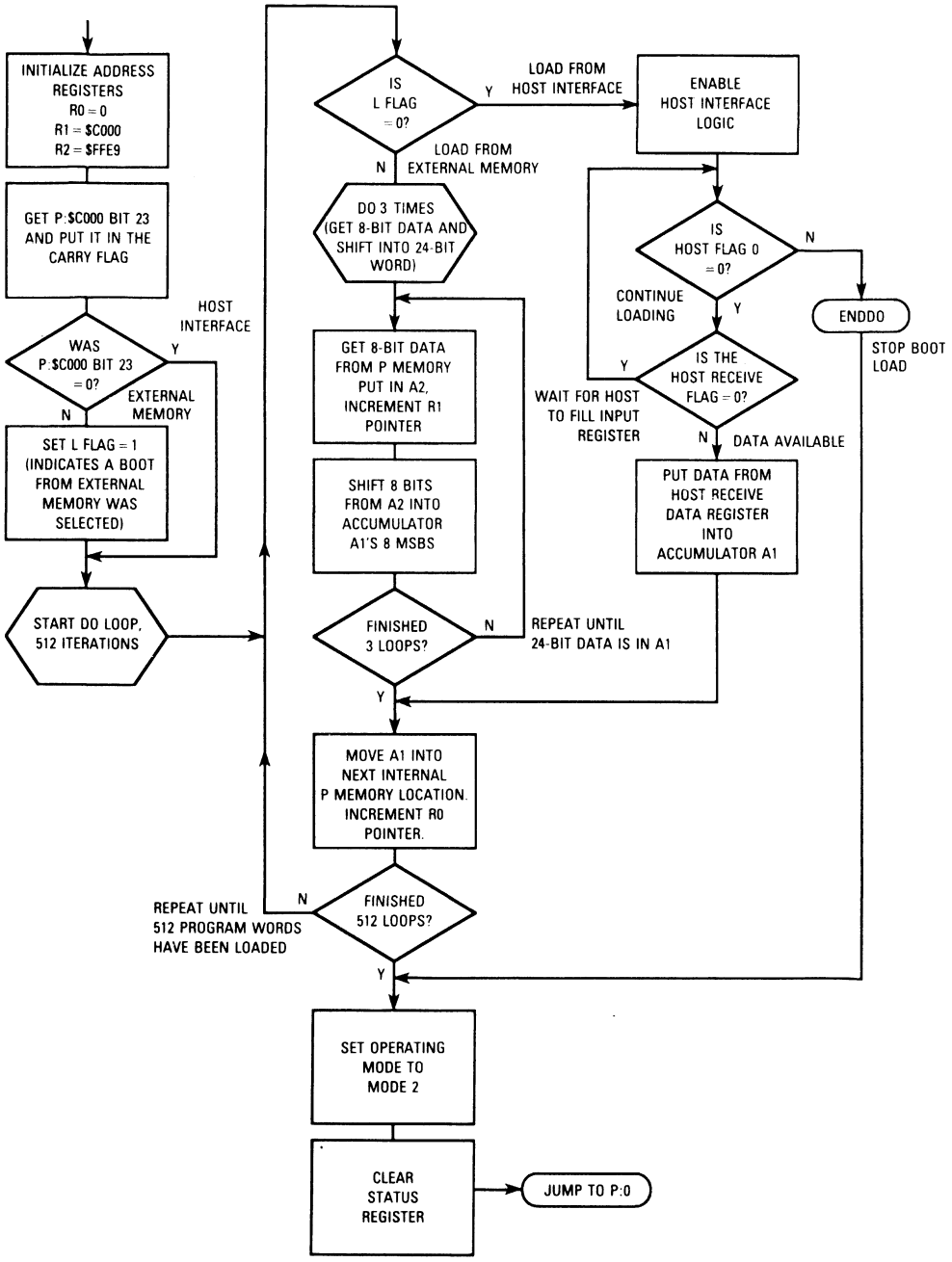


Figure A-1. Bootstrap Program Flowchart

```
; BOOTSTRAP CODE FOR DSP56001 - (C) Copyright 1986 Motorola Inc.
;
; Host algorithm  / AND / external bus method.
;
; This is the Bootstrap program contained in the DSP56001
; 32 word Boot ROM.
; This program can load the internal program memory from one
; of two external sources and contains logic to decide which
; one to load from.  This logic reads P:$C000 bit 23 to
; decide.  If P:$C000 bit 23 = 0 then it loads internal P RAM
; from H0-H7, using the Host Interface logic.
; If P:$C000 bit 23 = 1 then it loads from 1,536 consecutive
; byte-wide P memory locations (starting at P:$C000)

BOOT        EQU     $C000           ; this is the location in P memory
                                    ; on the external memory bus
                                    ; where the external byte-wide
                                    ; EPROM would be located

            ORG     PL:$0,PL:$0     ; bootstrap code starts at P:$0

START       MOVE    #$FFE9,R2       ; R2 = address of the Host
                                    ; Interface data register
            MOVE    #BOOT,R1        ; R1 = External P address of
                                    ; bootstrap byte-wide ROM
            MOVE    #0,R0           ; R0 = Internal P memory location
                                    ; where program will begin loading

            MOVE    P:(R1),A1       ; Get the data at P:$C000 bit 23
            ROL     A               ; Shift bit 23 into the Carry flag
            JCC     <INLOOP         ; Go perform load from Host
                                    ; pins if bit 23 is low.

; IMPORTANT NOTE: this routine assumes that the L bit is already
;    cleared before entering this program.  This would be the
;    case after a reset.  If this program is entered by
;    changing the OMR to bootstrap operating mode, make certain
;    that the L bit is cleared.  If the L bit was set before
;    changing modes, the program will load from the Host Interface.

            ORI     #$40,CCR        ; Set the L bit to indicate
                                    ; that the bootstrap program
                                    ; is being loaded from the
                                    ; external P:$C000 space.

; The first routine will load 1,536 bytes from the external P
; memory space beginning at P:$C000 (bits 7-0).  These will be
; condensed into 512 24-bit words and stored in contiguous P
; memory locations starting at P:$0.

; The shifter moves the 8-bit input data from register A2 into
; register A1 eight-bits-at-a-time.  After assembling one 24-bit
; word (this takes 3 loops) it stores the result in internal
```

```
; P memory and continues until internal P memory is filled.
; Note that the first routine loads data starting with the least
; significant byte of P:$0 first.

;       The second routine loads the internal P memory space
; using the Host Interface interface logic.  If the Host only wants
; to load a portion of the P memory, he can kill the Host Interface
; bootstrap load program, and start execution of the loaded
; program, by setting the Host Flag 0 (HF0) = 1.

INLOOP    DO      #512,_LOOP1       ; Load 512 instruction words

; This is the context switch

          JLC     <_HOSTLD          ; Go load from the Host Interface
                                    ; if the Limit flag is clear

; This is the first routine. It loads from external P memory.

          DO      #3,_LOOP2         ; Each instruction has 3 bytes
          MOVE    P:(R1)+,A2        ; Get the 8 LSB from ext. P mem.
          REP     #8                ; Shift 8 bit data into A1
          ASR     A
_LOOP2                              ; Get another byte.
          JMP     <_STORE           ; Then put the word in P memory

; This is the second routine. It loads from the Host Interface pins.

_HOSTLD   BSET    #0,X:$FFE0        ; Configure Port B as Host
_LBLA     JCLR    #3,X:$FFE9,_LBLB ; if HF0=1, stop loading data.
          ENDDO                     ; Must terminate the do loop
          JMP     <_BOOTEND

_LBLB     JCLR    #0,X:(R2),_LBLA   ; Wait for HRDF to go high
                                    ; (meaning data is present).
          MOVE    X:$FFEB,A1        ; Put 24-bit host data in A1

_STORE    MOVE    A1,P:(R0)+        ; Store 24-bit result in P mem.

_LOOP1                              ; and go get another 24-bit word.

; This is the exit handler that returns execution to normal
; expanded mode and jumps to the RESET vector.

_BOOTEND  MOVEC   #2,OMR            ; Set the operating mode to 2
                                    ; (and trigger an exit from
                                    ; bootstrap mode).
          ANDI    #$0,CCR           ; Clear SR as if RESET to 0.
                                    ; Delay needed for Op. Mode change
          JMP     <$0               ; Then execute the RESET vector.
```

APPLICATION EXAMPLES

The lowest cost DSP56001-based system uses no external memory and requires two chips, the DSP56001 and a low cost EPROM. The EPROM read access time should be less than 780 nanoseconds when the DSP56001 is operating at it's maximum clock rate of 20.5 MHz.

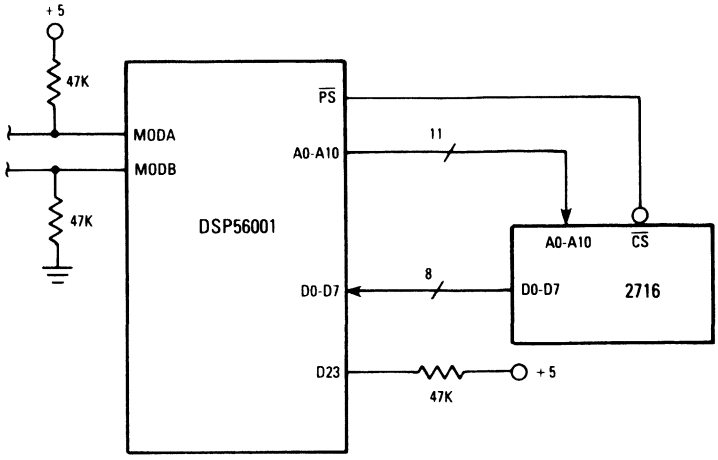


Figure A-2. No Glue, Low Cost Memory Port Bootstrap

A system with external data RAM memory requires no glue logic to select the external EPROM from bootstrap mode. $\overline{PS}$ is used to enable the EPROM and $\overline{DS}$ is used to enable the high speed data memories as shown in Figure A-3.

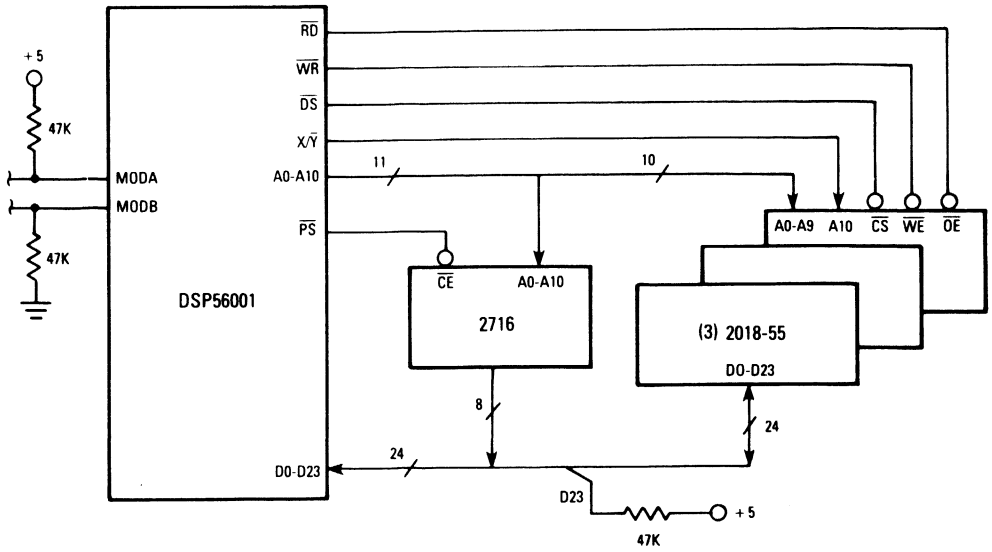


Figure A-3. Bootstrap with External Data RAM

This example (Figure A-4) shows the DSP56001 bootstrapping via the Host Port from a 12.5 MHz MC68000.

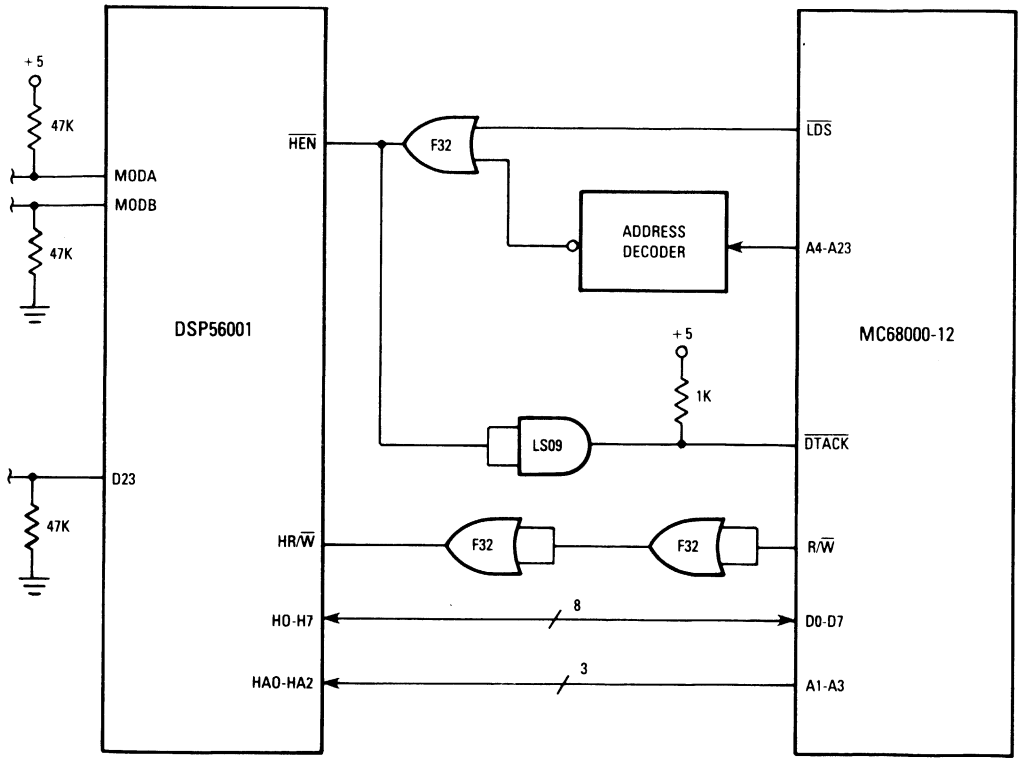


Figure A-4. DSP56001 Bootstrapping Example

Systems with external program memory can load the on-chip PRAM without using the bootstrap mode. In this example (Figure A-5), the DSP56001 is operated in mode 1 with external program memory at location $E000. The programmer can overlay the high speed on-chip PRAM with DSP algorithms by using the MOVEM instruction.

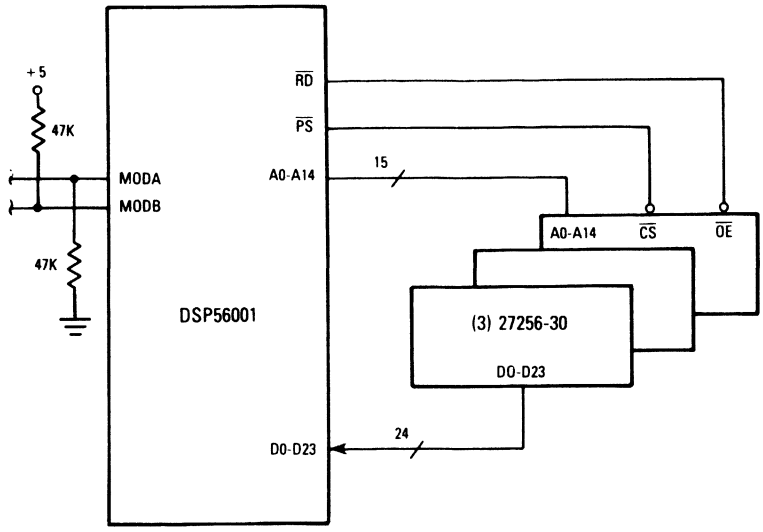


Figure A-5. 32K Words of External Program ROM

The last example (Figure A-6) shows the DSP56001 connected to the bus of an IBM-PC computer.

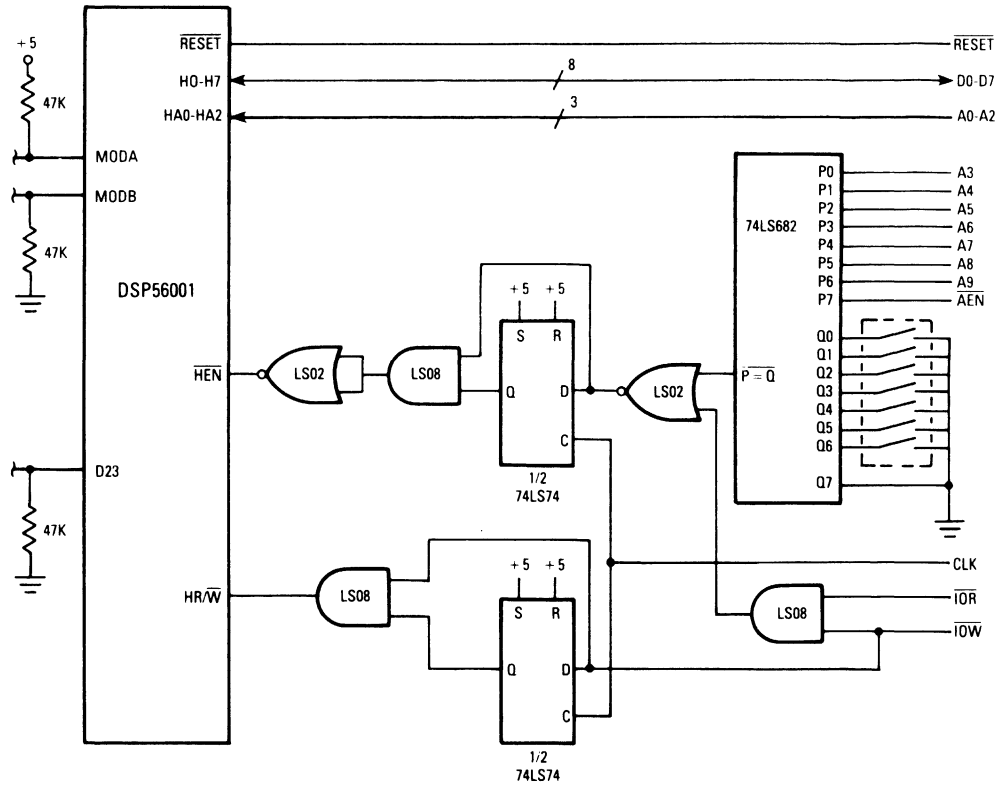


Figure A-6. IBM-PC to DSP56001 Host Port Interface

IBM-PC is a registered trademark of International Business Machines Corp.

APPENDIX II
MU-LAW/A-LAW EXPANSION TABLES

```
        org     x:$100
;
M_00    DC      $7D7C00 ; 8031
M_01    DC      $797C00 ; 7775
M_02    DC      $757C00 ; 7519
M_03    DC      $717C00 ; 7263
M_04    DC      $6D7C00 ; 7007
M_05    DC      $697C00 ; 6751
M_06    DC      $657C00 ; 6495
M_07    DC      $617C00 ; 6239
M_08    DC      $5D7C00 ; 5983
M_09    DC      $597C00 ; 5727
M_0A    DC      $557C00 ; 5471
M_0B    DC      $517C00 ; 5215
M_0C    DC      $4D7C00 ; 4959
M_0D    DC      $497C00 ; 4703
M_0E    DC      $457C00 ; 4447
M_0F    DC      $417C00 ; 4191
M_10    DC      $3E7C00 ; 3999
M_11    DC      $3C7C00 ; 3871
M_12    DC      $3A7C00 ; 3743
M_13    DC      $387C00 ; 3615
M_14    DC      $367C00 ; 3487
M_15    DC      $347C00 ; 3359
M_16    DC      $327C00 ; 3231
M_17    DC      $307C00 ; 3103
M_18    DC      $2E7C00 ; 2975
M_19    DC      $2C7C00 ; 2847
M_1A    DC      $2A7C00 ; 2719
M_1B    DC      $287C00 ; 2591
M_1C    DC      $267C00 ; 2463
M_1D    DC      $247C00 ; 2335
M_1E    DC      $227C00 ; 2207
M_1F    DC      $207C00 ; 2079
M_20    DC      $1EFC00 ; 1983
M_21    DC      $1DFC00 ; 1919
M_22    DC      $1CFC00 ; 1855
M_23    DC      $1BFC00 ; 1791
M_24    DC      $1AFC00 ; 1727
M_25    DC      $19FC00 ; 1663
M_26    DC      $18FC00 ; 1599
M_27    DC      $17FC00 ; 1535
M_28    DC      $16FC00 ; 1471
M_29    DC      $15FC00 ; 1407
M_2A    DC      $14FC00 ; 1343
M_2B    DC      $13FC00 ; 1279
M_2C    DC      $12FC00 ; 1215
M_2D    DC      $11FC00 ; 1151
M_2E    DC      $10FC00 ; 1087
M_2F    DC      $0FFC00 ; 1023
M_30    DC      $0F3C00 ;  975
M_31    DC      $0EBC00 ;  943
M_32    DC      $0E3C00 ;  911
M_33    DC      $0DBC00 ;  879
M_34    DC      $0D3C00 ;  847
M_35    DC      $0CBC00 ;  815
M_36    DC      $0C3C00 ;  783
M_37    DC      $0BBC00 ;  751
M_38    DC      $0B3C00 ;  719
M_39    DC      $0ABC00 ;  687
M_3A    DC      $0A3C00 ;  655
M_3B    DC      $09BC00 ;  623
M_3C    DC      $093C00 ;  591
M_3D    DC      $08BC00 ;  559
M_3E    DC      $083C00 ;  527
M_3F    DC      $07BC00 ;  495
M_40    DC      $075C00 ;  471
M_41    DC      $071C00 ;  455
M_42    DC      $06DC00 ;  439
M_43    DC      $069C00 ;  423
M_44    DC      $065C00 ;  407
M_45    DC      $061C00 ;  391
M_46    DC      $05DC00 ;  375
M_47    DC      $059C00 ;  359
M_48    DC      $055C00 ;  343
M_49    DC      $051C00 ;  327
M_4A    DC      $04DC00 ;  311
M_4B    DC      $049C00 ;  295
M_4C    DC      $045C00 ;  279
M_4D    DC      $041C00 ;  263
M_4E    DC      $03DC00 ;  247
M_4F    DC      $039C00 ;  231
M_50    DC      $036C00 ;  219
M_51    DC      $034C00 ;  211
M_52    DC      $032C00 ;  203
M_53    DC      $030C00 ;  195
M_54    DC      $02EC00 ;  187
M_55    DC      $02CC00 ;  179
M_56    DC      $02AC00 ;  171
M_57    DC      $028C00 ;  163
M_58    DC      $026C00 ;  155
M_59    DC      $024C00 ;  147
M_5A    DC      $022C00 ;  139
M_5B    DC      $020C00 ;  131
M_5C    DC      $01EC00 ;  123
M_5D    DC      $01CC00 ;  115
M_5E    DC      $01AC00 ;  107
M_5F    DC      $018C00 ;   99
M_60    DC      $017400 ;   93
M_61    DC      $016400 ;   89
```

```
M_62    DC      $015400 ;   85
M_63    DC      $014400 ;   81
M_64    DC      $013400 ;   77
M_65    DC      $012400 ;   73
M_66    DC      $011400 ;   69
M_67    DC      $010400 ;   65
M_68    DC      $00F400 ;   61
M_69    DC      $00E400 ;   57
M_6A    DC      $00D400 ;   53
M_6B    DC      $00C400 ;   49
M_6C    DC      $00B400 ;   45
M_6D    DC      $00A400 ;   41
M_6E    DC      $009400 ;   37
M_6F    DC      $008400 ;   33
M_70    DC      $007800 ;   30
M_71    DC      $007000 ;   28
M_72    DC      $006800 ;   26
M_73    DC      $006000 ;   24
M_74    DC      $005800 ;   22
M_75    DC      $005000 ;   20
M_76    DC      $004800 ;   18
M_77    DC      $004000 ;   16
M_78    DC      $003800 ;   14
M_79    DC      $003000 ;   12
M_7A    DC      $002800 ;   10
M_7B    DC      $002000 ;    8
M_7C    DC      $001800 ;    6
M_7D    DC      $001000 ;    4
M_7E    DC      $000800 ;    2
M_7F    DC      $000000 ;    0

A_80    DC      $158000 ;  688
A_81    DC      $148000 ;  656
A_82    DC      $178000 ;  752
A_83    DC      $168000 ;  720
A_84    DC      $118000 ;  560
A_85    DC      $108000 ;  528
A_86    DC      $138000 ;  624
A_87    DC      $128000 ;  592
A_88    DC      $1D8000 ;  944
A_89    DC      $1C8000 ;  912
A_8A    DC      $1F8000 ; 1008
A_8B    DC      $1E8000 ;  976
A_8C    DC      $198000 ;  816
A_8D    DC      $188000 ;  784
A_8E    DC      $1B8000 ;  880
A_8F    DC      $1A8000 ;  848
A_90    DC      $0AC000 ;  344
A_91    DC      $0A4000 ;  328
A_92    DC      $0BC000 ;  376
A_93    DC      $0B4000 ;  360
A_94    DC      $08C000 ;  280
A_95    DC      $084000 ;  264
A_96    DC      $09C000 ;  312
A_97    DC      $094000 ;  296
A_98    DC      $0EC000 ;  472
A_99    DC      $0E4000 ;  456

A_9A    DC      $0FC000 ;  504
A_9B    DC      $0F4000 ;  488
A_9C    DC      $0CC000 ;  408
A_9D    DC      $0C4000 ;  392
A_9E    DC      $0DC000 ;  440
A_9F    DC      $0D4000 ;  424
A_A0    DC      $560000 ; 2752
A_A1    DC      $520000 ; 2624
A_A2    DC      $5E0000 ; 3008
A_A3    DC      $5A0000 ; 2880
A_A4    DC      $460000 ; 2240
A_A5    DC      $420000 ; 2112
A_A6    DC      $4E0000 ; 2496
A_A7    DC      $4A0000 ; 2368
A_A8    DC      $760000 ; 3776
A_A9    DC      $720000 ; 3648
A_AA    DC      $7E0000 ; 4032
A_AB    DC      $7A0000 ; 3904
A_AC    DC      $660000 ; 3264
A_AD    DC      $620000 ; 3136
A_AE    DC      $6E0000 ; 3520
A_AF    DC      $6A0000 ; 3392
A_B0    DC      $2B0000 ; 1376
A_B1    DC      $290000 ; 1312
A_B2    DC      $2F0000 ; 1504
A_B3    DC      $2D0000 ; 1440
A_B4    DC      $230000 ; 1120
A_B5    DC      $210000 ; 1056
A_B6    DC      $270000 ; 1248
A_B7    DC      $250000 ; 1184
A_B8    DC      $3B0000 ; 1888
A_B9    DC      $390000 ; 1824
A_BA    DC      $3F0000 ; 2016
A_BB    DC      $3D0000 ; 1952
A_BC    DC      $330000 ; 1632
A_BD    DC      $310000 ; 1568
A_BE    DC      $370000 ; 1760
A_BF    DC      $350000 ; 1696
A_C0    DC      $015800 ;   43
A_C1    DC      $014800 ;   41
A_C2    DC      $017800 ;   47
A_C3    DC      $016800 ;   45
A_C4    DC      $011800 ;   35
A_C5    DC      $010800 ;   33
A_C6    DC      $013800 ;   39
A_C7    DC      $012800 ;   37
A_C8    DC      $01D800 ;   59
A_C9    DC      $01C800 ;   57
A_CA    DC      $01F800 ;   63
A_CB    DC      $01E800 ;   61
A_CC    DC      $019800 ;   51
A_CD    DC      $018800 ;   49
A_CE    DC      $01B800 ;   55
A_CF    DC      $01A800 ;   53
A_D0    DC      $005800 ;   11
A_D1    DC      $004800 ;    9
A_D2    DC      $007800 ;   15
```

```
A_D3    DC      $006800 ;   13
A_D4    DC      $001800 ;    3
A_D5    DC      $000800 ;    1
A_D6    DC      $003800 ;    7
A_D7    DC      $002800 ;    5
A_D8    DC      $00D800 ;   27
A_D9    DC      $00C800 ;   25
A_DA    DC      $00F800 ;   31
A_DB    DC      $00E800 ;   29
A_DC    DC      $009800 ;   19
A_DD    DC      $008800 ;   17
A_DE    DC      $00B800 ;   23
A_DF    DC      $00A800 ;   21
A_E0    DC      $056000 ;  172
A_E1    DC      $052000 ;  164
A_E2    DC      $05E000 ;  188
A_E3    DC      $05A000 ;  180
A_E4    DC      $046000 ;  140
A_E5    DC      $042000 ;  132
A_E6    DC      $04E000 ;  156
A_E7    DC      $04A000 ;  148
A_E8    DC      $076000 ;  236
A_E9    DC      $072000 ;  228
A_EA    DC      $07E000 ;  252
A_EB    DC      $07A000 ;  244
A_EC    DC      $066000 ;  204
A_ED    DC      $062000 ;  196
A_EE    DC      $06E000 ;  220
A_EF    DC      $06A000 ;  212
A_F0    DC      $02B000 ;   86
A_F1    DC      $029000 ;   82
A_F2    DC      $02F000 ;   94
A_F3    DC      $02D000 ;   90
A_F4    DC      $023000 ;   70
A_F5    DC      $021000 ;   66
A_F6    DC      $027000 ;   78
A_F7    DC      $025000 ;   74
A_F8    DC      $03B000 ;  118
A_F9    DC      $039000 ;  114
A_FA    DC      $03F000 ;  126
A_FB    DC      $03D000 ;  122
A_FC    DC      $033000 ;  102
A_FD    DC      $031000 ;   98
A_FE    DC      $037000 ;  110
A_FF    DC      $035000 ;  106
END
```

3

```
_START xromdos 0000 0000

_DATA X 0100
7D7C00 797C00 757C00 717C00 6D7C00 697C00 657C00 617C00 5D7C00 597C00 557C00
517C00 4D7C00 497C00 457C00 417C00 3E7C00 3C7C00 3A7C00 387C00 367C00 347C00
327C00 307C00 2E7C00 2C7C00 2A7C00 287C00 267C00 247C00 227C00 207C00 1EFC00
1DFC00 1CFC00 1BFC00 1AFC00 19FC00 18FC00 17FC00 16FC00 15FC00 14FC00 13FC00
12FC00 11FC00 10FC00 0FFC00 0F3C00 0EBC00 0E3C00 0DBC00 0D3C00 0CBC00 0C3C00
0BBC00 0B3C00 0ABC00 0A3C00 09BC00 093C00 08BC00 083C00 07BC00 073C00 071C00
06DC00 069C00 065C00 061C00 05DC00 059C00 055C00 051C00 04DC00 049C00 045C00
041C00 03DC00 039C00 036C00 034C00 032C00 030C00 02EC00 02CC00 02AC00 028C00
026C00 024C00 022C00 020C00 01EC00 01CC00 01AC00 018C00 017400 016400 015400
014400 013400 012400 011400 010400 00F400 00E400 00D400 00C400 00B400 00A400
009400 008400 007800 007000 006800 006000 005800 005000 004800 004000 003800
003000 002800 002000 001800 001000 000800 000000 158000 148000 178000 168000
118000 108000 138000 128000 1D8000 1C8000 1F8000 1E8000 198000 188000 1B8000
1A8000 0AC000 0A4000 0BC000 0B4000 08C000 084000 09C000 094000 0EC000 0E4000
0FC000 0F4000 0CC000 0C4000 0DC000 0D4000 560000 520000 5E0000 5A0000 460000
420000 4E0000 4A0000 760000 720000 7E0000 7A0000 660000 620000 6E0000 6A0000
2B0000 290000 2F0000 2D0000 230000 210000 270000 250000 3B0000 390000 3F0000
3D0000 330000 310000 370000 350000 015800 014800 017800 016800 011800 010800
013800 012800 01D800 01C800 01F800 01E800 019800 018800 01B800 01A800 005800
004800 007800 006800 001800 000800 003800 002800 00D800 00C800 00F800 00E800
009800 008800 00B800 00A800 056000 052000 05E000 05A000 046000 042000 04E000
04A000 076000 072000 07E000 07A000 066000 062000 06E000 06A000 02B000 029000
02F000 02D000 023000 021000 027000 025000 03B000 039000 03F000 03D000 033000
031000 037000 035000
_END
```

APPENDIX III
SINE WAVE TABLE

```
        ORG     Y:$100

S_00    DC      $000000 ;  0.000000000000000000000000
S_01    DC      $03242B ;  0.024541258811950683593750
S_02    DC      $0647D9 ;  0.049067616462707519531250
S_03    DC      $096A90 ;  0.073564529418945312500000
S_04    DC      $0C8BD3 ;  0.098017096519470214843750
S_05    DC      $0FAB27 ;  0.122410655021667480468750
S_06    DC      $12C810 ;  0.146730422973632812500000
S_07    DC      $15E214 ;  0.170961856842041015625000
S_08    DC      $18F8B8 ;  0.195090293884277343750000
S_09    DC      $1C0B82 ;  0.219101190567016601562500
S_0A    DC      $1F19F9 ;  0.242980122566223144531250
S_0B    DC      $2223A5 ;  0.266712784767150878906250
S_0C    DC      $25280C ;  0.290284633636474609375000
S_0D    DC      $2826B9 ;  0.313681721687316894531250
S_0E    DC      $2B1F35 ;  0.336889863014221191406250
S_0F    DC      $2E110A ;  0.359894990921020507812500
S_10    DC      $30FBC5 ;  0.382683396339416503906250
S_11    DC      $33DEF3 ;  0.405241370201110839843750
S_12    DC      $36BA20 ;  0.427555084228515625000000
S_13    DC      $398CDD ;  0.449611306190490722656250
S_14    DC      $3C56BA ;  0.471396684646606445312500
S_15    DC      $3F174A ;  0.492898225784301757812500
S_16    DC      $41CE1E ;  0.514102697372436523437500
S_17    DC      $447ACD ;  0.534997582435607910156250
S_18    DC      $471CED ;  0.555570244789123535156250
S_19    DC      $49B415 ;  0.575808167457580566406250
S_1A    DC      $4C3FE0 ;  0.595699310302734375000000
S_1B    DC      $4EBFE9 ;  0.615231633186340332031250
S_1C    DC      $5133CD ;  0.634393334388732910156250
S_1D    DC      $539B2B ;  0.653172850608825683593750
S_1E    DC      $55F5A5 ;  0.671558976173400878906250
S_1F    DC      $5842DD ;  0.689540505409240722656250
S_20    DC      $5A827A ;  0.707106828689575195312500
S_21    DC      $5CB421 ;  0.724247097969055175781250
S_22    DC      $5ED77D ;  0.740951180458068847656250
S_23    DC      $60EC38 ;  0.757208824157714843750000
S_24    DC      $62F202 ;  0.773010492324829101562500
S_25    DC      $64E889 ;  0.788346409797668457031250
S_26    DC      $66CF81 ;  0.803207516670227050781250
S_27    DC      $68A69F ;  0.817584872245788574218750
S_28    DC      $6A6D99 ;  0.831469655036926269531250
S_29    DC      $6C2429 ;  0.844853520393371582031250
S_2A    DC      $6DCA0D ;  0.857728600502014160156250
S_2B    DC      $6F5F03 ;  0.870087027549743652343750
S_2C    DC      $70E2CC ;  0.881921291351318359375000
S_2D    DC      $72552D ;  0.893224358558654785156250
S_2E    DC      $73B5EC ;  0.903989315032958984375000
S_2F    DC      $7504D3 ;  0.914209723472595214843750
```

```
S_30    DC      $7641AF ;  0.92387950420379638671875
S_31    DC      $776C4F ;  0.93299281597137451171875
S_32    DC      $788484 ;  0.94154405593872070312500
S_33    DC      $798A24 ;  0.94952821731567382812500
S_34    DC      $7A7D05 ;  0.95694029331207275390625
S_35    DC      $7B5D04 ;  0.96377611160278320312500
S_36    DC      $7C29FC ;  0.97003126144409179687500
S_37    DC      $7CE3CF ;  0.97570216655731201171875
S_38    DC      $7D8A5F ;  0.98078525066375732421875
S_39    DC      $7E1D94 ;  0.98527765274047851562500
S_3A    DC      $7E9D56 ;  0.98917651176452636718750
S_3B    DC      $7F0992 ;  0.99247956275939941406250
S_3C    DC      $7F6237 ;  0.99518477916717529296875
S_3D    DC      $7FA737 ;  0.99729049205780029296875
S_3E    DC      $7FD888 ;  0.99879550933837890625000
S_3F    DC      $7FF622 ;  0.99969887733459472656250
S_40    DC      $7FFFFF ;  0.99999988079071044921875
S_41    DC      $7FF622 ;  0.99969887733459472656250
S_42    DC      $7FD888 ;  0.99879550933837890625000
S_43    DC      $7FA737 ;  0.99729049205780029296875
S_44    DC      $7F6237 ;  0.99518477916717529296875
S_45    DC      $7F0992 ;  0.99247956275939941406250
S_46    DC      $7E9D56 ;  0.98917651176452636718750
S_47    DC      $7E1D94 ;  0.98527765274047851562500
S_48    DC      $7D8A5F ;  0.98078525066375732421875
S_49    DC      $7CE3CF ;  0.97570216655731201171875
S_4A    DC      $7C29FC ;  0.97003126144409179687500
S_4B    DC      $7B5D04 ;  0.96377611160278320312500
S_4C    DC      $7A7D05 ;  0.95694029331207275390625
S_4D    DC      $798A24 ;  0.94952821731567382812500
S_4E    DC      $788484 ;  0.94154405593872070312500
S_4F    DC      $776C4F ;  0.93299281597137451171875
S_50    DC      $7641AF ;  0.92387950420379638671875
S_51    DC      $7504D3 ;  0.91420972347259521484375
S_52    DC      $73B5EC ;  0.90398931503295898437500
S_53    DC      $72552D ;  0.89322435855865478515625
S_54    DC      $70E2CC ;  0.88192129135131835937500
S_55    DC      $6F5F03 ;  0.87008702754974365234375
S_56    DC      $6DCA0D ;  0.85772860050201416015625
S_57    DC      $6C2429 ;  0.84485352039337158203125
S_58    DC      $6A6D99 ;  0.83146965503692626953125
S_59    DC      $68A69F ;  0.81758487224578857421875
S_5A    DC      $66CF81 ;  0.80320751667022705078125
S_5B    DC      $64E889 ;  0.78834640979766845703125
S_5C    DC      $62F202 ;  0.77301049232482910156250
S_5D    DC      $60EC38 ;  0.75720882415771484375000
S_5E    DC      $5ED77D ;  0.74095118045806884765625
S_5F    DC      $5CB421 ;  0.72424709796905517578125
S_60    DC      $5A827A ;  0.70710682868957519531250
S_61    DC      $5842DD ;  0.68954050540924072265625
S_62    DC      $55F5A5 ;  0.67155897617340087890625
S_63    DC      $539B2B ;  0.65317285060882568359375
S_64    DC      $5133CD ;  0.63439333438873291015625
S_65    DC      $4EBFE9 ;  0.61523163318634033203125
S_66    DC      $4C3FE0 ;  0.59569931030273437500000
S_67    DC      $49B415 ;  0.57580816745758056640625
```

```
S_68    DC      $471CED ;  0.55557024478912353515625
S_69    DC      $447ACD ;  0.53499758243560791015625
S_6A    DC      $41CE1E ;  0.51410269737243652343750
S_6B    DC      $3F174A ;  0.49289822578430175781250
S_6C    DC      $3C56BA ;  0.47139668464660644531250
S_6D    DC      $398CDD ;  0.44961130619049072265625
S_6E    DC      $36BA20 ;  0.42755508422851562500000
S_6F    DC      $33DEF3 ;  0.40524137020111083984375
S_70    DC      $30FBC5 ;  0.38268339633941650390625
S_71    DC      $2E110A ;  0.35989499092102050781250
S_72    DC      $2B1F35 ;  0.33688986301422119140625
S_73    DC      $2826B9 ;  0.31368172168731689453125
S_74    DC      $25280C ;  0.29028463363647460937500
S_75    DC      $2223A5 ;  0.26671278476715087890625
S_76    DC      $1F19F9 ;  0.24298012256622314453125
S_77    DC      $1C0B82 ;  0.21910119056701660156250
S_78    DC      $18F8B8 ;  0.19509029388427734375000
S_79    DC      $15E214 ;  0.17096185684204101562500
S_7A    DC      $12C810 ;  0.14673042297363281250000
S_7B    DC      $0FAB27 ;  0.12241065502166748046875
S_7C    DC      $0C8BD3 ;  0.09801709651947021484375
S_7D    DC      $096A90 ;  0.07356452941894531250000
S_7E    DC      $0647D9 ;  0.04906761646270751953125
S_7F    DC      $03242B ;  0.02454125881195068359375
S_80    DC      $000000 ;  0.00000000000000000000000
S_81    DC      $FCDBD5 ; -0.02454125881195068359375
S_82    DC      $F9B827 ; -0.04906761646270751953125
S_83    DC      $F69570 ; -0.07356452941894531250000
S_84    DC      $F3742D ; -0.09801709651947021484375
S_85    DC      $F054D9 ; -0.12241065502166748046875
S_86    DC      $ED37F0 ; -0.14673042297363281250000
S_87    DC      $EA1DEC ; -0.17096185684204101562500
S_88    DC      $E70748 ; -0.19509029388427734375000
S_89    DC      $E3F47E ; -0.21910119056701660156250
S_8A    DC      $E0E607 ; -0.24298012256622314453125
S_8B    DC      $DDDC5B ; -0.26671278476715087890625
S_8C    DC      $DAD7F4 ; -0.29028463363647460937500
S_8D    DC      $D7D947 ; -0.31368172168731689453125
S_8E    DC      $D4E0CB ; -0.33688986301422119140625
S_8F    DC      $D1EEF6 ; -0.35989499092102050781250
S_90    DC      $CF043B ; -0.38268339633941650390625
S_91    DC      $CC210D ; -0.40524137020111083984375
S_92    DC      $C945E0 ; -0.42755508422851562500000
S_93    DC      $C67323 ; -0.44961130619049072265625
S_94    DC      $C3A946 ; -0.47139668464660644531250
S_95    DC      $C0E8B6 ; -0.49289822578430175781250
S_96    DC      $BE31E2 ; -0.51410269737243652343750
S_97    DC      $BB8533 ; -0.53499758243560791015625
S_98    DC      $B8E313 ; -0.55557024478912353515625
S_99    DC      $B64BEB ; -0.57580816745758056640625
S_9A    DC      $B3C020 ; -0.59569931030273437500000
S_9B    DC      $B14017 ; -0.61523163318634033203125
S_9C    DC      $AECC33 ; -0.63439333438873291015625
S_9D    DC      $AC64D5 ; -0.65317285060882568359375
S_9E    DC      $AA0A5B ; -0.67155897617340087890625
S_9F    DC      $A7BD23 ; -0.68954050540924072265625
```

```
S_A0    DC      $A57D86 ; -0.70710682868957519531250
S_A1    DC      $A34BDF ; -0.72424709796905517578125
S_A2    DC      $A12883 ; -0.74095118045806884765625
S_A3    DC      $9F13C8 ; -0.75720882415771484375000
S_A4    DC      $9D0DFE ; -0.77301049232482910156250
S_A5    DC      $9B1777 ; -0.78834640979766845703125
S_A6    DC      $99307F ; -0.80320751667022705078125
S_A7    DC      $975961 ; -0.81758487224578857421875
S_A8    DC      $959267 ; -0.83146965503692626953125
S_A9    DC      $93DBD7 ; -0.84485352039337158203125
S_AA    DC      $9235F3 ; -0.85772860050201416015625
S_AB    DC      $90A0FD ; -0.87008702754974365234375
S_AC    DC      $8F1D34 ; -0.88192129135131835937500
S_AD    DC      $8DAAD3 ; -0.89322435855865478515625
S_AE    DC      $8C4A14 ; -0.90398931503295898437500
S_AF    DC      $8AFB2D ; -0.91420972347259521484375
S_B0    DC      $89BE51 ; -0.92387950420379638671875
S_B1    DC      $8893B1 ; -0.93299281597137451171875
S_B2    DC      $877B7C ; -0.94154405593872070312500
S_B3    DC      $8675DC ; -0.94952821731567382812500
S_B4    DC      $8582FB ; -0.95694029331207275390625
S_B5    DC      $84A2FC ; -0.96377611160278320312500
S_B6    DC      $83D604 ; -0.97003126144409179687500
S_B7    DC      $831C31 ; -0.97570216655731201171875
S_B8    DC      $8275A1 ; -0.98078525066375732421875
S_B9    DC      $81E26C ; -0.98527765274047851562500
S_BA    DC      $8162AA ; -0.98917651176452636718750
S_BB    DC      $80F66E ; -0.99247956275939941406250
S_BC    DC      $809DC9 ; -0.99518477916717529296875
S_BD    DC      $8058C9 ; -0.99729049205780029296875
S_BE    DC      $802778 ; -0.99879550933837890625000
S_BF    DC      $8009DE ; -0.99969887733459472656250
S_C0    DC      $800000 ; -1.00000000000000000000000
S_C1    DC      $8009DE ; -0.99969887733459472656250
S_C2    DC      $802778 ; -0.99879550933837890625000
S_C3    DC      $8058C9 ; -0.99729049205780029296875
S_C4    DC      $809DC9 ; -0.99518477916717529296875
S_C5    DC      $80F66E ; -0.99247956275939941406250
S_C6    DC      $8162AA ; -0.98917651176452636718750
S_C7    DC      $81E26C ; -0.98527765274047851562500
S_C8    DC      $8275A1 ; -0.98078525066375732421875
S_C9    DC      $831C31 ; -0.97570216655731201171875
S_CA    DC      $83D604 ; -0.97003126144409179687500
S_CB    DC      $84A2FC ; -0.96377611160278320312500
S_CC    DC      $8582FB ; -0.95694029331207275390625
S_CD    DC      $8675DC ; -0.94952821731567382812500
S_CE    DC      $877B7C ; -0.94154405593872070312500
S_CF    DC      $8893B1 ; -0.93299281597137451171875
S_D0    DC      $89BE51 ; -0.92387950420379638671875
S_D1    DC      $8AFB2D ; -0.91420972347259521484375
S_D2    DC      $8C4A14 ; -0.90398931503295898437500
S_D3    DC      $8DAAD3 ; -0.89322435855865478515625
S_D4    DC      $8F1D34 ; -0.88192129135131835937500
S_D5    DC      $90A0FD ; -0.87008702754974365234375
S_D6    DC      $9235F3 ; -0.85772860050201416015625
S_D7    DC      $93DBD7 ; -0.84485352039337158203125
```

```
S_D8    DC      $959267 ; -0.831469655036926269531 25
S_D9    DC      $975961 ; -0.817584872245788574218 75
S_DA    DC      $99307F ; -0.803207516670227050781 25
S_DB    DC      $9B1777 ; -0.788346409797668457031 25
S_DC    DC      $9D0DFE ; -0.773010492324829101562 50
S_DD    DC      $9F13C8 ; -0.757208824157714843750 00
S_DE    DC      $A12883 ; -0.740951180458068847656 25
S_DF    DC      $A34BDF ; -0.724247097969055175781 25
S_E0    DC      $A57D86 ; -0.707106828689575195312 50
S_E1    DC      $A7BD23 ; -0.689540505409240722656 25
S_E2    DC      $AA0A5B ; -0.671558976173400878906 25
S_E3    DC      $AC64D5 ; -0.653172850608256835937 5
S_E4    DC      $AECC33 ; -0.634393334388732910156 25
S_E5    DC      $B14017 ; -0.615231633186340332031 25
S_E6    DC      $B3C020 ; -0.595699310302734375000 00
S_E7    DC      $B64BEB ; -0.575808167457580566406 25
S_E8    DC      $B8E313 ; -0.555570244789123535156 25
S_E9    DC      $BB8533 ; -0.534997582435607910156 25
S_EA    DC      $BE31E2 ; -0.514102697372436523437 50
S_EB    DC      $C0E8B6 ; -0.492898225784301757812 50
S_EC    DC      $C3A946 ; -0.471396684646606445312 50
S_ED    DC      $C67323 ; -0.449611306190490722656 25
S_EE    DC      $C945E0 ; -0.427555084228515625000 00
S_EF    DC      $CC210D ; -0.405241370201110839843 75
S_F0    DC      $CF043B ; -0.382683396339416503906 25
S_F1    DC      $D1EEF6 ; -0.359894990921020507812 50
S_F2    DC      $D4E0CB ; -0.336889863014221191406 25
S_F3    DC      $D7D947 ; -0.313681721687316894531 25
S_F4    DC      $DAD7F4 ; -0.290284633636474609375 00
S_F5    DC      $DDDC5B ; -0.266712784767150878906 25
S_F6    DC      $E0E607 ; -0.242980122566223144531 25
S_F7    DC      $E3F47E ; -0.219101190567016601562 50
S_F8    DC      $E70748 ; -0.195090293884277343750 00
S_F9    DC      $EA1DEC ; -0.170961856842041015625 00
S_FA    DC      $ED37F0 ; -0.146730422973632812500 00
S_FB    DC      $F054D9 ; -0.122410655021667480468 75
S_FC    DC      $F3742D ; -0.098017096519470214843 75
S_FD    DC      $F69570 ; -0.073564529418945312500 00
S_FE    DC      $F9B827 ; -0.049067616462707519531 25
S_FF    DC      $FCDBD5 ; -0.024541258811950683593 75
        END
```

```
_START sinegen 0000 0000

_DATA Y 0100
000000 03242B 0647D9 096A90 0C8BD3 0FAB27 12C810 15E214 18F8B8 1C0B82 1F19F9
2223A5 25280C 2826B9 2B1F35 2E110A 30FBC5 33DEF3 36BA20 398CDD 3C56BA 3F174A
41CE1E 447ACD 471CED 49B415 4C3FE0 4EBFE9 5133CD 539B2B 55F5A5 5842DD 5A827A
5CB421 5ED77D 60EC38 62F202 64E889 66CF81 68A69F 6A6D99 6C2429 6DCA0D 6F5F03
70E2CC 72552D 73B5EC 7504D3 7641AF 776C4F 788484 798A24 7A7D05 7B5D04 7C29FC
7CE3CF 7D8A5F 7E1D94 7E9D56 7F0992 7F6237 7FA737 7FD888 7FF622 7FFFFF 7FF622
7FD888 7FA737 7F6237 7F0992 7E9D56 7E1D94 7D8A5F 7CE3CF 7C29FC 7B5D04 7A7D05
798A24 788484 776C4F 7641AF 7504D3 73B5EC 72552D 70E2CC 6F5F03 6DCA0D 6C2429
6A6D99 68A69F 66CF81 64E889 62F202 60EC38 5ED77D 5CB421 5A827A 5842DD 55F5A5
539B2B 5133CD 4EBFE9 4C3FE0 49B415 471CED 447ACD 41CE1E 3F174A 3C56BA 398CDD
36BA20 33DEF3 30FBC5 2E110A 2B1F35 2826B9 25280C 2223A5 1F19F9 1C0B82 18F8B8
15E214 12C810 0FAB27 0C8BD3 096A90 0647D9 03242B 000000 FCDBD5 F9B827 F69570
F3742D F054D9 ED37F0 EA1DEC E70748 E3F47E E0E607 DDDC5B DAD7F4 D7D947 D4E0CB
D1EEF6 CF043B CC210D C945E0 C67323 C3A946 C0E8B6 BE31E2 BB8533 B8E313 B64BEB
B3C020 B14017 AECC33 AC64D5 AA0A5B A7BD23 A57D86 A34BDF A12883 9F13C8 9D0DFE
9B1777 99307F 975961 959267 93DBD7 9235F3 90A0FD 8F1D34 8DAAD3 8C4A14 8AFB2D
89BE51 8893B1 877B7C 8675DC 8582FB 84A2FC 83D604 831C31 8275A1 81E26C 8162AA
80F66E 809DC9 8058C9 802778 8009DE 800000 8009DE 802778 8058C9 809DC9 80F66E
8162AA 81E26C 8275A1 831C31 83D604 84A2FC 8582FB 8675DC 877B7C 8893B1 89BE51
8AFB2D 8C4A14 8DAAD3 8F1D34 90A0FD 9235F3 93DBD7 959267 975961 99307F 9B177
9D0DFE 9F13C8 A12883 A34BDF A57D86 A7BD23 AA0A5B AC64D5 AECC33 B14017 B3C020
B64BEB B8E313 BB8533 BE31E2 C0E8B6 C3A946 C67323 C945E0 CC210D CF043B D1EEF6
D4E0CB D7D947 DAD7F4 DDDC5B E0E607 E3F47E E70748 EA1DEC ED37F0 F054D9 F3742D
F69570 F9B827 FCDBD5
_END
```

MOTOROLA

Technical Summary

Cascadable Adaptive Finite Impulse Response Digital Filter (CAFIR)

This document provides a technical summary of the DSP56200, a Cascadable Adaptive Finite Impulse Response (CAFIR) digital filter chip. For users not familiar with digital filtering, an appendix on this topic is also included.

The DSP56200 is an algorithm specific, digital signal processing (DSP) peripheral designed to perform computationally-intensive tasks associated with digital filtering. Two principal functions are performed by the DSP56200 — FIR filtering and adaptive FIR filtering using the Least-Mean-Square (LMS) algorithm. A flexible chip-cascading scheme enables the user to easily build filters with extended tap lengths and/or increased speed. Its performance, features, and simple interface make the DSP56200 a natural solution for problems such as echo cancelling, telephone line equalization, noise cancelling, conventional filtering, and many other DSP applications. Key features of the DSP56200 are:

- Three Modes of Operation
  - Single FIR Filter
  - Dual FIR Filter (Two Independent FIR Filters)
  - Single Adaptive FIR Filter
- High Performance Hardware
  - 24 x 16 Bit Multiplication with 40-Bit Accumulation
  - 10.25 MHz Internal Operation
  - Single-Cycle Multiply-Accumulate
  - Single-Cycle Update of a Coefficient
  - Ultra-Low-Power Standby Mode
  - 256 x 24-bit Coefficient RAM
  - 256 x 16-bit Data RAM
  - Unused RAM Available for System Storage
  - 28-Pin Dual-in-Line Package
- Architecture Optimized for Digital Filtering
  - Three Execution Units Operate in Parallel
  - Multiple Internal Buses
- Digital Filtering Features
  - 16-Bit Rounding Option on Filtered Output
  - dc Tap Option
  - Programmable Filter Tap Length (4 to 256 Taps)
  - Programmable Loop Gain[1]
  - Programmable Coefficient Leakage Term[1]
  - Adaptation Disable Capability[1]
  - LMS Adaptation Algorithm[1]
- Unlimited Cascadability Offers[2]
  - Longer-Tap Filters
  - Higher Sampling Rates
- High Throughput Rates — Examples of Possible Configurations
  - 227 kHz FIR Filter (32 Taps, 1 DSP56200)
  - 37 kHz FIR Filter (256 Taps, 1 DSP56200)
  - 115 kHz Adaptive Filter (256 Taps, 8 Cascaded DSP56200s)
  - 19 kHz Adaptive Filter (256 Taps, 1 DSP56200)
  - Many Other Configurations Possible
- Simple Interface to Popular Hosts
  - Microprocessors
  - Microcomputers
  - General Purpose Digital Signal Processors

[1]Options unique to adaptive filtering mode

[2]The DSP56200 implements a true cascade. A true cascade means that the error term in the adaptive filtering mode is calculated from the partial sums of ***ALL*** chips in the cascade.

BRE283/D

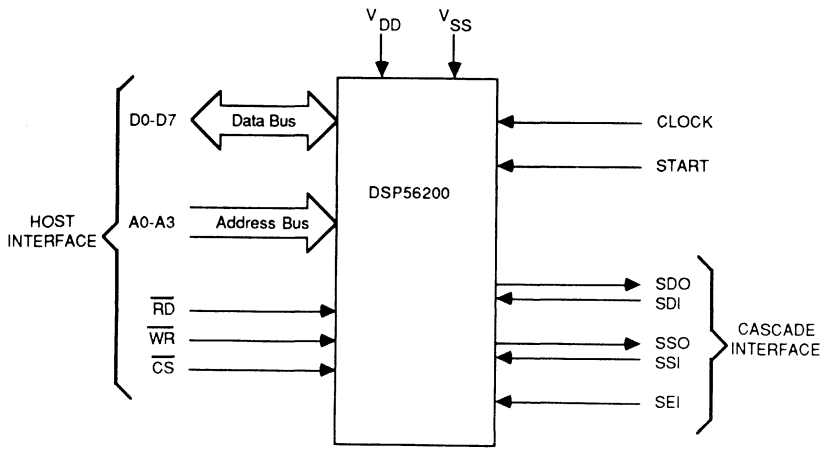


Figure 1. Functional Signal Groups

ARCHITECTURE DESCRIPTION

The DSP56200 offers two advantages over general purpose DSPs — higher performance and minimal development time. The high performance of the DSP56200 results from an algorithm specific architecture featuring three execution units — the Asynchronous Parallel Interface, the Cascade Interface, and the Computation Unit — which execute in parallel (Figure 2). Development time is minimized because the DSP56200 is an off-the-shelf chip which requires no software development. The algorithms are implemented in hardware.

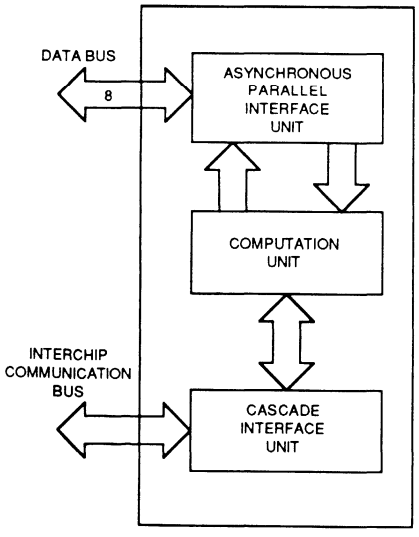


Figure 2. Parallelism Within the DSP56200

Careful design of the interface units has virtually eliminated the need for "glue" logic when interfacing to a host processor or cascading DSP56200 chips. The Parallel Interface resembles that of a fast static RAM, and allows interfacing to fast, general purpose DSPs and MPUs having tight timing requirements. The Cascade Interface performs all the functions associated with cascading, thereby simplifying the design of multi-chip systems.

The Computation Unit performs the arithmetic necessary in FIR and adaptive FIR filtering (Figure 3). It contains the hardware necessary for implementing a 256-tap FIR filter with adaptation capability, including a 256 x 24-bit Coefficient RAM, a 256 × 16-bit Data RAM, and an Arithmetic Unit. The Data RAM is configured as a variable length circular queue, allowing it to function as a virtual shift register. The Arithmetic Unit configures itself for both the LMS adaptation algorithm and the FIR filter calculation, implements the available digital filtering options, performs 100 ns 24 × 16-bit multiply-accumulates, and performs 100 ns coefficient updates. It is further described in the **INTERNAL ARITHMETIC DESCRIPTION**.

MODES OF OPERATION

The DSP56200 is designed to operate in one of three modes — Single FIR Filter, Dual FIR Filter, or Single Adaptive FIR Filter. Functional diagrams of these three configurations are shown in Figure 4. Users unfamiliar with digital filtering should refer to Appendix 1.

FIR filtering is a simple way to perform digital filtering. The Single FIR Filter mode is used to implement one FIR filter, either on a single chip or on several DSP56200s in a cascade (with up to 256 taps per chip). Using software design tools, filter coefficients can be calculated to obtain the desired frequency response for performing functions such as differentiating, bandpass filtering, and lowpass filtering. In this mode, the DSP56200 is configured to implement the FIR filtering equation (see Appendix 1).

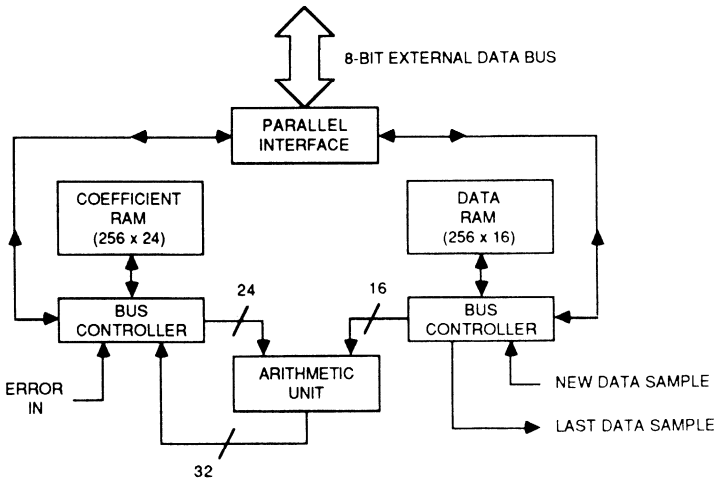
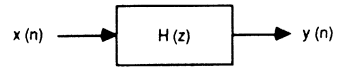


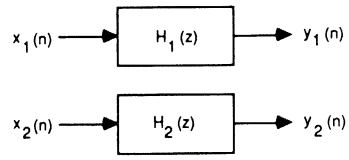
Figure 3. Computation Unit Block Diagram

The Dual FIR Filter mode is an extension of the Single FIR Filter mode. It allows two independent inputs, $x_1(n)$ and $x_2(n)$, to be FIR filtered using only one DSP56200. Note that both filters must use the same number of taps up to a maximum of 128. The DSP56200 is not adaptive or cascadable in the Dual FIR Filter mode.

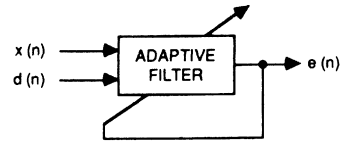
The Single Adaptive FIR Filter mode provides a unique solution to problems such as echo cancelling and adaptive equalization of telephone lines. This mode is used to implement one adaptive filter, either on a single chip or on several DSP56200s in cascade. Adaptive filters must perform the FIR filter multiply-accumulate operation, followed by an adaptation operation to modify the coefficients. The DSP56200 updates every filter coefficient once during each sample period using the Least-Mean-Squares (LMS) adaptation algorithm.



(a) SINGLE FIR FILTER MODE



(b) DUAL FIR FILTER MODE



(c) SINGLE ADAPTIVE FIR FILTER MODE

Figure 4. DSP56200 Configurations

INTERNAL ARITHMETIC DESCRIPTION

The key to the accuracy of the DSP56200 is its Arithmetic Unit. Accuracy is affected by the number of bits in the coefficient and the errors due to rounding. In FIR filter applications, the actual frequency response will deviate from the user's desired response if not enough bits are used to represent the coefficients. Wider coefficient word widths also enable adaptive filters to more closely approximate a desired impulse response, resulting in smaller error terms. Roundoff errors decrease as the size of the accumulator and coefficients increases. The DSP56200 uses a 24-bit coefficient, and will accept data words having up to 16 bits. The results of the multiply-accumulate operation are stored in a 40-bit accumulator. Both the 16-bit data samples and 24-bit coefficients are represented as signed fractional numbers.

In FIR filtering applications, the filtering process is described by the following equation:

$$y(n) = \sum_{i=0}^{N-1} h(i) \times (n-i) \qquad (1)$$

The "ith" coefficient is represented by h(i), and x(n-i) represents one of the previous data samples. In this mode, the Arithmetic Unit is configured as a multiplier-accumulator as shown in Figure 5.

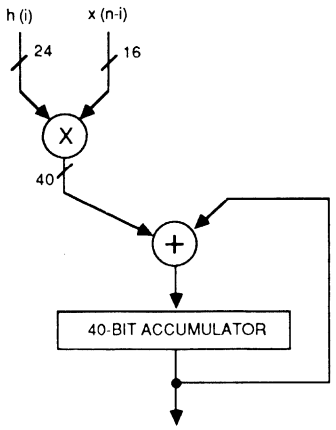


Figure 5. Arithmetic Unit in Multiply-Accumulate Mode

Adaptive filtering is a two-step process. First, the error term (the filter's output) is calculated and second, the error term is used to update the coefficients. The error calculation is described by:

$$e(n) = d(n) - \sum_{i=0}^{N-1} h(i) \times (n-i) \qquad (2)$$

where d(n) represents the reference (desired) input of the adaptive filter. During this first step, an FIR filtering operation is performed so that the Arithmetic Unit is again configured as shown in Figure 5. The second step involves modifying each coefficient using the LMS adaptation equation:

$$h(i)_{new} = h(i)_{old} + Ke \times (n-i) \pm Leakage \qquad (3)$$

where K is a programmable loop gain, and e is the error term calculated in equation (2). The Arithmetic Unit is configured as shown in Figure 6 during the adaptation step, allowing for single-cycle updates.

When a narrowband signal such as a sine wave is applied to the filter's input, the coefficients drift from their true values because there is not enough frequency content present in the signal. The coefficients will erroneously grow in magnitude, resulting in a larger error term.

The leakage term is included to compensate for coefficient drift. This 8-bit user-programmable constant, located in bits 2^{-16} through 2^{-23}, slowly pushes the coefficients towards zero, effectively offsetting the slow growth in coefficient magnitude. The term is small enough that it does not affect the convergence of the filter, but adequate to prevent the slow coefficient drift occurring for narrowband input signals.

Rounding is another function performed within the Arithmetic Unit. When the DSP56200 is multiply-accumulating (equation 1 or 2), the final result can optionally be rounded to a 16 bit fractional result, prior to being output. Also, when updating coefficients (equation 3), each new coefficient is convergently rounded to a 24-bit fractional number, and then written back into the 24-bit Coefficient RAM.

The Arithmetic Unit also includes a dc tap option. This option is useful for an adaptive filter which has a dc component on one of the filter's inputs. An adaptive filter with a dc tap can synthesize a signal to cancel this component (such as a dc signal introduced through an A/D converter). The dc tap can also be used to add a dc offset to the output when configured as an FIR filter.

PERFORMANCE

In measuring the performance of the DSP56200, it is important to consider the nature of real-time applications. In a real-time DSP system dealing with digitized waveforms, all processing associated with the current sample must be completed before a new sample arrives. The simplified flowchart in Figure 7 shows the flow of control in a real-time environment. The performance of the DSP56200 is therefore measured by the amount of time it requires to complete the processing associated with the current sample. This length of time determines the minimal time allowable between samples, and is referred to as the minimum sampling period. The reciprocal of the minimum sampling period is the system's maximum sampling frequency, f_S.

There are four parameters which determine the maximum sampling rate of the DSP56200:

1) The number of DSP56200s cascaded together,
2) The number of taps used on each DSP56200,
3) The clock frequency of the DSP56200, and
4) The selected mode of operation.

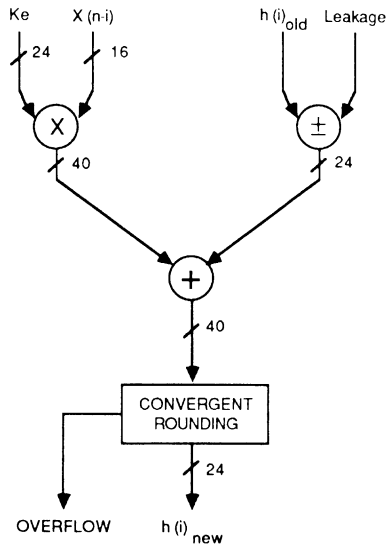


Figure 6. Arithmetic Unit in Coefficient Update Mode

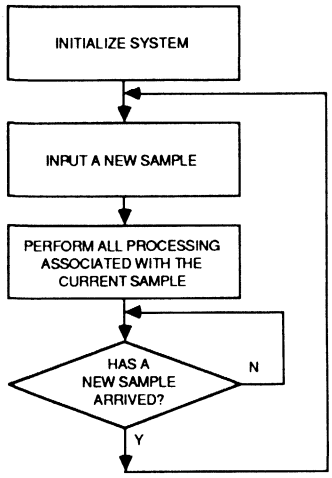


Figure 7. Flowchart for Real-Time Systems

The formulas below are used to calculate the DSP56200's maximum sampling frequency for a given system. In many cases, this maximum rate can be increased by cascading more DSP56200 chips together and using fewer taps on each chip.

$$\text{Maximum } f_s \leq f_{ck}/\#\text{cycles}$$

Where:

f_{ck} = DSP56200 input clock frequency

$$\#\text{ cycles} = \begin{cases} 12+N+q & \text{: Single FIR Filter Mode} \\ 18+2N+q & \text{: Dual FIR Filter Mode} \\ 17+2N+r & \text{: Single Adaptive Filter Mode} \end{cases}$$

$$q = \begin{cases} 29+n\text{-}N & \text{: } (29+n\text{-}N) > 0 \\ 0 & \text{: otherwise} \end{cases}$$

$$r = \begin{cases} 30+n\text{-}N & \text{: } (30+n\text{-}N) > 0 \\ 0 & \text{: otherwise} \end{cases}$$

n = Number of chips cascaded together

N = Number of taps used on each chip

The intermediate terms, q and r, can never be negative. Also note that in Dual FIR Filter mode, N is the number of taps available for each of the two independent filters, and therefore $N \leq 128$. Table 1 shows some performance figures for the DSP56200 in different configurations assuming a 10.0 MHz external clock.

Table 1. DSP56200 Performance Figures

Single Chip

Maximum Sampling Frequency (kHz)				
Mode	**Number of Taps**			
	32	**64**	**128**	**256**
FIR Filter	227	132	71	37
Adaptive Filter	123	69	37	19
Dual FIR Filters	122	68	36	—

Four Chips in Cascade

Maximum Sampling Frequency (kHz)				
Mode	**Total Number of Taps**			
	128	**256**	**512**	**1024**
FIR Filter	222	132	71	37
Adaptive Filter	120	69	37	19

Eight Chips in Cascade

Maximum Sampling Frequency (kHz)				
Mode	**Total Number of Taps**			
	256	**512**	**1024**	**2048**
FIR Filter	204	132	71	37
Adaptive Filter	115	69	37	19

Sixteen Chips in Cascade

Maximum Sampling Frequency (kHz)				
Mode	**Total Number of Taps**			
	512	**1024**	**2048**	**4096**
FIR Filter	175	132	71	37
Adaptive Filter	105	69	37	19

SIGNAL DESCRIPTION

The DSP56200 is a 28-pin dual-in-line package (DIP) integrated circuit (Figure 1). Its signals can logically be grouped into the following categories:

- Host Interface
- Cascade Interface
- Clocks
- Power

Descriptions of these signals are presented in the following paragraphs.

HOST INTERFACE

D0-D7 (Data Bus)

These eight pins provide a bidirectional data bus for communication with a host processor. The pins remain in the high-impedance state unless both $\overline{RD}$ and $\overline{CS}$ are asserted.

A0-A3 (Register Address Pins)

A0-A3 select (in conjunction with the least significant bit of the Configuration Register) which register will be addressed when the Chip Select line is brought low and a read or write operation is performed.

$\overline{CS}$ (Chip Select)

This pin (active low) enables accesses to the chip operating registers. When not asserted, the D0-D7 lines will go into the high-impedance state and all access to the chip will be disabled.

$\overline{RD}$ (Read Strobe)

When $\overline{RD}$ is asserted, the contents of the register specified by A0-A3 will be driven onto D0-D7. When $\overline{RD}$ is high, pins D0-D7 go into the high-impedance state.

$\overline{WR}$ (Write Strobe)

This pin (active low) enables host writes to the register specified by A0-A3. Data on D0-D7 must be valid for the specified setup time before the rising edge of $\overline{WR}$.

CASCADE INTERFACE

SDI (Serial Data Input)

This pin is used in the cascade mode to receive data from the last tap of the data shift register in the preceding DSP56200 chip. It connects to the SDO pin of the previous chip in cascade. If the chip is first in cascade or is used in standalone mode, this pin should be grounded.

SDO (Serial Data Output)

This pin is used in the cascade mode to pass the last data sample in the data shift register to the next DSP56200 in the cascade. It connects to the SDI pin of the next DSP56200. The output of this pin is not connected if the chip is used in standalone mode or if it is the last chip in a cascaded system.

SSI (Serial Sum Input)

This pin is used in the cascade mode to receive the partial sums from preceding stages. If the chip is first in the cascade or is used in standalone mode, this pin should be grounded.

SSO (Serial Sum Out)

This pin is primarily used in the cascade mode to pass the partial sums to the next DSP56200 in the cascade. The SSO pin is usually connected to the SSI pin of the next chip in the cascade. In the adaptive filter mode, the SSO pin of the last chip in the cascade is connected to the SEI pin on all chips cascaded including itself. This pin should not be connected in standalone FIR modes (single and dual FIR filters).

SEI (Serial Error Input)

This pin is used in the adaptive filter mode. It provides the means of receiving the error term output from the last chip in the cascade. In standalone Adaptive Filter mode, this pin is tied to the SSO pin. In cascade Adaptive Filter mode, this pin is tied to the SSO pin of the last chip in the cascade. This pin should be grounded in the Single FIR Filter mode or the Dual FIR Filter mode.

CLOCKS AND POWER

CLOCK (Clock Input)

This pin accepts the input clock for the DSP56200. The internal and external clocking frequencies are the same, and the maximum frequency for this input is 10.25 MHz. In cascaded systems, all DSP56200s must be driven from the same clock source. When CLOCK is held low, the device enters a power-down mode.

START (Start Processing Command)

This pin is used to provide a second clock to the chip at the system's sampling rate. This clock must be synchronized with the signal on the CLOCK pin in order to ensure proper operation.

V_{DD} (Power) — Three Pins

V_{SS} (Ground) — Three Pins

INTERFACE DESCRIPTION

The DSP56200 has been designed for simple interfacing to a large number of host processors. The chip's asynchronous interface meets the tight timing margins of fast DSP processors, and it also interfaces to slower microcomputer/microprocessor and DSP chips. The parallel interface resembles that of a fast static RAM.

The speed required of the host processor is determined by two considerations — the time required for I/O with the DSP56200, and the time required by the host for additional processing of a sample. The sum of these intervals must be less than the time between samples (the sampling period). Slower, single-chip microcomputers may be adequate hosts in systems with lower sampling rates, and one host may even be able to support several different filters. For high sample rate applications, a fast DSP processor may be required to complete the necessary I/O in the allotted time.

An example of a 4-chip adaptive filter interfaced to a DSP56000 host is shown in Figure 8. An external timing

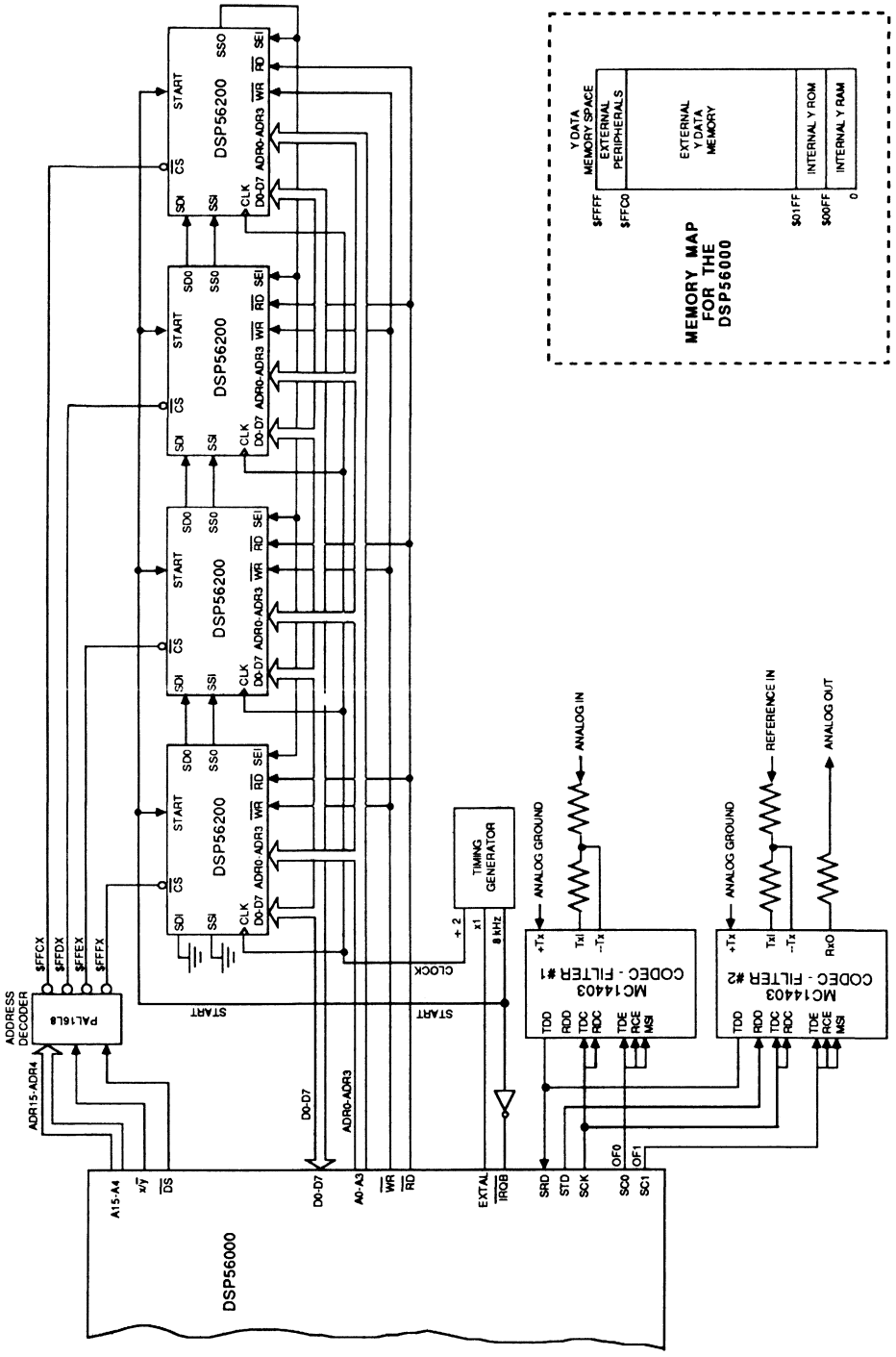


Figure 8. Four-Chip Adaptive Filter System

3

generator is used to provide a chip clock and a START pulse (sample rate clock) which has been synchronized with the chip's clock. Note that this system could be a 1024 tap adaptive filter with a maximum sampling rate of 19 kHz, or it could be a 128 tap adaptive filter with a maximum sampling rate of 120 kHz (32 taps per chip). Other combinations are also possible. Note that applications with higher sampling rates will require faster A/D converters. A 4-chip FIR filter would connect in a similar manner, but the SEI pins would be grounded.

REGISTER MODEL

The DSP56200 is initialized and accessed by the host through a set of control and data transfer registers. In addition, the registers provide access to values in the Coefficient and Data RAMs, allowing unused memory to be used as auxilliary system storage. All register access occurs through the Asynchronous Parallel Interface Unit. The control and data registers are double buffered. Information is only passed from the first buffer into the second when the chip receives a pulse on its start pin. Note that no host access is allowed during the negative transition of the START signal.

Registers in the DSP56200 have been divided into two banks of sixteen registers (Figure 9). Bank 0 contains the registers commonly accessed during real-time processing and Bank 1 registers are used for initializing the chip. The two banks share one common register, the Configuration Register, located at address 0F (hexadecimal) in each bank. Switching banks is done by complementing the least significant bit of this common register. Once the desired bank has been selected, the registers are accessed using A0-A3, $\overline{RD}$ or $\overline{WR}$, and $\overline{CS}$. The registers have been ordered so that they can be accessed by the host using a simple autoincrementing address mode.

Upon power-up, the user must initialize the chip's registers and RAMs. This normally involves writing into the Configuration Register to select the mode of operation and to select Bank 1. Then, the FIR Tap Length register is written, which programs the number of taps and also resets the chip. Upon reset, the chip timing is initialized and the contents of the Data RAM are undefined. Next, the Configuration Register is accessed to change to Bank 0. Then the RAMs are usually initialized by writing a valid coefficient into each location of the Coefficient RAM and a zero into each location of the Data RAM. One Data RAM location and one Coefficient RAM location can be written each sampling period. The DSP56200 is then ready for real-time filtering.

REGISTER DESCRIPTION

X1 Register, X2 Register

The X1 Register is a 16-bit register that functions as the data input register for both the FIR mode and the Adaptive FIR Filter mode. Data from the X1 register is copied into the Data RAM shift register once per START cycle. In the dual FIR mode an additional register called X2 functions as the second filter's data input register. The X2 register operates in a manner similar to X1. Data from the X2 register is copied into the Data RAM shift register of the second FIR filter once per START cycle.

D Register (Adaptive FIR Filter Mode Only)

The D Register is a 16-bit register that functions as the reference (echo) input when the DSP56200 is used in the echo cancel/adaptive FIR filter mode. It is represented as d(n) in the adaptive filtering equations. This register is not used in the nonadaptive modes of operation.

K Register (Adaptive FIR Filter Mode Only)

The K register is a 16-bit register used only in the adaptive filtering mode. K is the loop gain used in the LMS adaptation process. It is multiplied by the error term and tap X(n-i) to generate an updated value for coefficient h(i) (see Appendix 1).

Caution

K must always be a positive number, i.e., Bit 7 of the Most Significant Byte should be zero at all times.

Configuration Register

The Configuration Register is used to configure the modes and options of the DSP56200. The bits are defined in Figure 10.

Bit 7, FIR/Adaptive FIR, determines whether the chip will operate as a finite impulse response (FIR) filter or as an adaptive FIR filter. This bit is set to a "1" for an adaptive FIR filter.

Bit 6, Single FIR/Dual FIR, determines whether the filter will be configured as a single-channel or dual-channel FIR filter. In the dual mode, the tap lengths of both filters are the same and are controlled by the FIR Tap Length (FTL) register. The maximum value for the FTL in dual mode is limited to 127 (128 taps). In the dual mode, Output Data Bytes 3 and 2 contain channel 1 output while Output Data Bytes 1 and 0 contain channel 2 output data (refer to Figure 9).

Table 2 summarizes the valid configurations for the chip.

Table 2. DSP56200 Mode Configurations

Adaptive/ Nonadaptive (Configuration Bit 7)	Single/Dual (Configuration Bit 6)	Mode
0	0	Single FIR Filter
0	1	Dual FIR Filter
1	0	Single Adaptive FIR Filter
1	1	(Operation Undefined)

Bit 5, Position in Cascade, selects whether the chip is configured to operate as stand-alone/first in cascade, or in cascade but not the first chip (Table 3). The first configuration is selected when this bit is a zero. The second configuration is selected when this bit is a one. This bit must be set to a zero whenever the DSP56200 is used in the Dual FIR Filter Mode.

BANK 0

REGISTER #	WRITE
0	X1 - HIGH
1	X1 - LOW
2	D - HIGH
3	D - LOW
4	K - HIGH
5	K - LOW
6	X2 - HIGH
7	X2 - LOW
8	DATA RAM - HIGH
9	DATA RAM - LOW
A	COEFFICIENT RAM - HIGH
B	COEFFICIENT RAM - MID
C	COEFFICIENT RAM - LOW
D	RAM ADDRESS
E	*
F	CONFIGURATION

REGISTER #	READ
0	OUTPUT - 3
1	OUTPUT - 2
2	OUTPUT - 1
3	OUTPUT - 0
4	LAST TAP 1 - HIGH
5	LAST TAP 1 - LOW
6	LAST TAP 2 - HIGH
7	LAST TAP 2 - LOW
8	DATA RAM - HIGH
9	DATA RAM - LOW
A	COEFFICIENT RAM - HIGH
B	COEFFICIENT RAM - MID
C	COEFFICIENT RAM - LOW
D	*
E	CONFIGURATION**
F	CONFIGURATION**

BANK 1

REGISTER #	WRITE
0	LEAKAGE
1	FIR TAP LENGTH
2	*
3	*
4	*
5	*
6	*
7	*
8	*
9	*
A	*
B	*
C	*
D	*
E	*
F	CONFIGURATION

REGISTER #	READ
0	*
1	*
2	*
3	*
4	*
5	*
6	*
7	*
8	*
9	*
A	*
B	*
C	*
D	*
E	CONFIGURATION**
F	CONFIGURATION**

*Not Available for Use
**The Configuration Register is Readable at Addresses 0E and 0F (Hex)

Figure 9. Programming Model

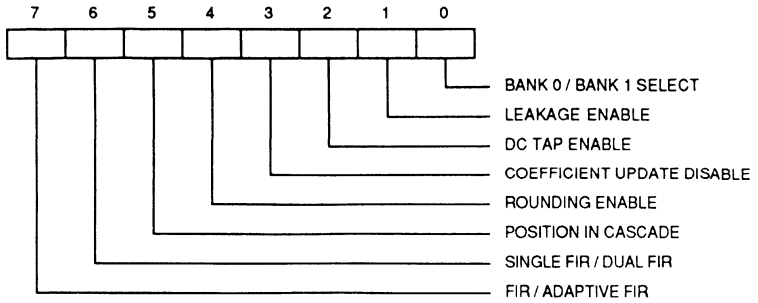


Figure 10. Configuration Register

Table 3. DSP56200 Cascade Configurations

Configuration Bit 5	System Configuration
0	Single DSP56200 System (Standalone)
0	First DSP56200 in a Cascaded System
1	Not First DSP56200 in a Cascaded System

Bit 4, 16-Bit Rounding, selects whether the filter output will be represented as a 32-bit result in the Output Register, or as a rounded 16-bit result. In the latter case, data bytes 3 and 2 in the Output Register contain the valid 16-bit rounded result, and data bytes 1 and 0 contain invalid data. This bit is set to a "1" for 16 bit rounding.

Bit 3, Adaptation Disable, is used to disable the LMS algorithm in the adaptive filter mode. When this bit is set to a "1", the chip will continue to compute error terms using the last set of updated filter coefficients. In echo cancelling applications, this bit is typically set when 'double talk' is detected.

Bit 2, dc Tap Enable, is set to a "1" to turn on the dc tap. The dc tap looks like a tap in the data shift register with a fixed value of 7FFF (hexadecimal). The dc tap is multiplied by its corresponding (last) coefficient during the FIR filtering phase, and is also used when updating the last coefficient in adaptive filter mode. The dc tap is normally used in the adaptive filter mode to remove any dc offset in the A/D converter. The dc tap is substituted for the last tap in the data shift register when it is enabled. The last tap data is not lost, however, and will be transferred correctly.

NOTE

If the dc tap option is desired in cascaded systems, bit 2 is set to a "1" only in the last DSP56200 in the cascade.

Bit 1, Leakage Enable, is set to a "1" when the use of leakage is desired in the coefficient update calculation.

Bit 0, Register Bank Select, selects which Register Bank is to be accessed by the host processor. The configuration register appears in both Bank 0 and Bank 1, allowing this bit to always be available for control of register bank selection. This bit is set to a "1" for access to Bank 1 and operates asynchronously within the Parallel Interface, allowing access to both banks during one sampling period.

Leakage Register (Adaptive FIR Filter Mode Only)

The leakage register is used in the adaptive filter mode when coefficient update is enabled (Bit 4 of the Configuration register) and when the Leakage enable bit is set to a "1". Leakage is an 8-bit magnitude used to control coefficient drift in adaptive filtering.

FIR Tap Length Register

This 8-bit register determines the number of taps used in the FIR filter. The register is loaded with the number of taps minus one. For example, if a 256-tap filter is desired, this register is loaded with 255. Valid values range from 3 to 255 in Single FIR or Single Adaptive FIR Filter modes, and from 3 to 127 in the Dual FIR mode. Writing to this register also resets the chip. Normally this register is written by the host upon power-up.

RAM Address Register

This 8-bit register specifies which location will be selected during accesses to the Coefficient and Data RAM. It allows access to taps being used within the filter and to any memory not used in the FIR filter calculation, and automatically postincrements once each sampling period. Thus, one memory location in the Coefficient RAM and one memory location in the Data RAM at the same address can be accessed during one sampling period. Note that the RAM used for auxiliary system storage will not be overwritten during the FIR filtering process.

Coefficient RAM Access Register

This 24-bit register allows the user to read or write any location in the Coefficient RAM. The host processor reads a RAM location by writing the desired address into the Coefficient/Data Address Register, waiting for two pulses to occur on the START pin, i.e., two sample periods, and then reading the value of this register. A write is performed by writing the desired value to this register. The actual write operation to the Coefficient RAM occurs during the following sampling period. All locations in the Coefficient RAM can be accessed using the RAM Address Register.

Data RAM Access Register

This 16-bit register allows the user to read or write any location in the Data RAM. The host processor reads a

RAM location by writing the desired address into the Coefficient/Data Address Register, waiting for two pulses to occur on the START pin (i.e., two sample periods), and then reading the value of this register. A write is performed by writing the desired value to this register. The actual write operation to the Data RAM occurs during the following sampling period. If the desired address resides within the FIR filter structure, the DSP56200 automatically performs a logical-to-physical address conversion and correctly accesses the desired filter tap.

Last Tap 1, Last Tap 2

The Last Tap 1 Register provides the user with a copy of the last data sample in the data shift register. When in the Dual FIR Filter mode, Last Tap 2 contains the last data sample for the second FIR filter. If the dc tap option is selected, these registers contain the last data sample instead of containing the constant 7FFF (hexadecimal) used in in dc tap calculations. These registers are provided only for convenience and are not required when cascading chips, since the last tap is also transmitted serially to the next chip in the cascade. These registers, in conjunction with the X1 and X2 input registers, are useful for signal power calculations.

Output Data Register

The Output Data Register bytes 3 through 0 contain the final FIR or adaptive FIR filter output. In the single channel mode the result will be four bytes (32 bits) unless the 16-bit rounding mode is set. In this case, bytes 3 and 2 contain a valid rounded 16-bit result and bytes 1 and 0 contain invalid data. Only 16 bits of output are available for each channel in Dual FIR Filter mode. Bytes 3 and 2 contain the output for the first FIR filter and bytes 1 and 0 contain the output for the second. These outputs are rounded to 16 bits if rounding is enabled in the Configuration Register.

APPENDIX A
DIGITAL FILTERING BASICS

Finite Impulse Response Filters

Finite impulse response (FIR) filtering is a common method of performing digital filtering. This filtering process can be viewed as a weighted moving average of past data values. The FIR filtering equation (A-1) describes how the filter's output is related to its input:

$$y(n) = \sum_{i=0}^{N-1} h(i) \times (n-i) \qquad \text{(A-1)}$$

where:

n = the time index
i = the filter tap index
N = the number of taps in the FIR filter
h(i) = the "ith" coefficient in the FIR filter
x(n-i) = the "ith" most recent data sample

Thus, the FIR filtering process is an accumulation of N product terms. The coefficients are usually pre-calculated using software design tools, and are based on the user's desired frequency response. These coefficients represent the impulse response of the desired filter. Equation A-1 describes the discrete convolution of a digitized input waveform with an impulse response function.

FIR filtering can be readily implemented in hardware as shown in Figure A-1. Each z^{-1} represents a memory element with a delay of one sample period. N of these memory elements are cascaded together to form a tapped shift register of length N. This shift register is used to store the N most current data samples, each of which is referred to as a "filter tap". The width of the shift register is the number of bits used to represent the data samples — 16 bits in the case of the DSP56200. At the start of a sample period, a new data sample is entered into the shift register and the oldest data sample is discarded.

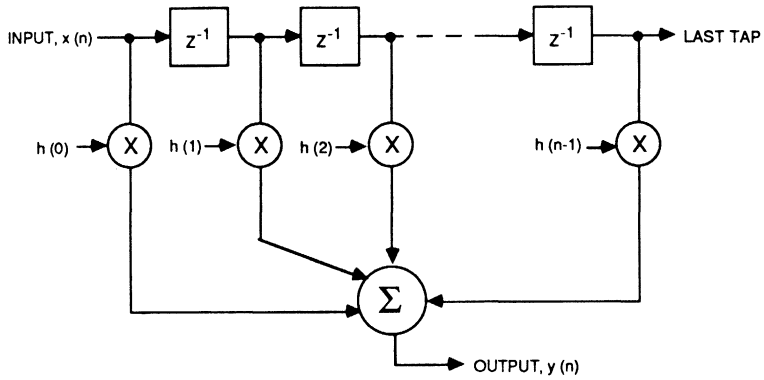


Figure A-1. Structure of a Finite Impulse Response (FIR) Filter

Hardware is also required to calculate and accumulate the product terms. This is usually done with a single multiplier-accumulator (MAC) in order to conserve hardware. The MAC multiplies a coefficient with its corresponding data sample and adds this product with the sum of the previous products already in the accumulator. Thus, N multiply-accumulates occur each time a new sample is shifted into the FIR filter.

FIR filters have numerous advantages. One benefit of digital hardware is that there is no drift with temperature, voltage or age, giving digital filters a significant advantage over their analog counterparts. In addition, FIR filters can be designed to have a linear phase characteristic, and are inherently stable since they have no poles. The linear phase characteristic is desirable since it ensures that an input data signal is always delayed by a constant length of time, independent of its frequency content.

FIR filters find uses in many areas of signal processing. Typical applications include differentiating, notch filtering, bandsplitting filters, matched filtering, filter banks, interpolation, and Hilbert Transforms.

Adaptive Filters

Adaptive filters are a special class of filters used to solve a unique set of signal processing problems. These filters have two inputs, x(n) and d(n),which are usually correlated in some manner (Figure A-2). One input, x(n), is passed through an internal time varying filter, which tries to form an estimate of the desired input, d(n). The parameters of this internal filter eventually converge to a point where the internal filter can accurately estimate the desired input, minimizing the adaptive filter's output. This output represents the difference or error, e(n), between the desired signal and the estimate of the desired signal. There are two aspects to adaptive filters — the internal filter structure and the adaptation algorithm.

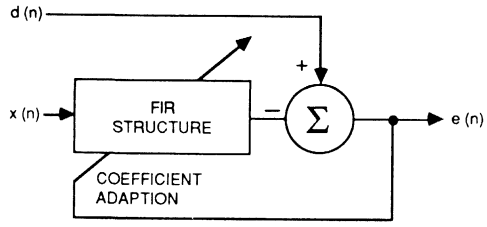


Figure A-2. Block Diagram of an Adaptive Filter

The most common adaptive filter implementation is based on a FIR filter structure whose coefficients are adapted using the Least-Mean-Square (LMS) algorithm. First, the signal x(n) is FIR filtered using equation A-1 to provide an estimate of the second input, d(n). The error in the estimate is then calculated:

$$e(n) = d(n) - \sum_{i=0}^{N-1} h(i) \times (n-i) \qquad \text{(A-2)}$$

This error term is then used to modify every FIR filter coefficient using the following equation derived from the LMS adaptation algorithm:

$$h(i)_{new} = h(i)_{old} + Ke \times (n-i) \qquad \text{(A-3)}$$

where:

$h(i)_{new}$ = the value of the updated "ith" coefficient to be used during the next sample period.
$h(i)_{old}$ = the value of the "ith" coefficient during the current sample period.
K = the gain constant
e = the calculated error term
x(n-i) = the "ith" most recent data sample

At the beginning of the next sample period, two new samples, x(n) and d(n), are shifted into the system and the process repeats.

After several iterations, the FIR filter coefficients converge to values which consistently minimize the mean square error (the filter's output). At this point, the adaptive filter is now able to estimate the d-input by passing the x-input through the FIR filtering hardware. It is interesting to note that once the filter has converged, the coefficients of the internal FIR filter resemble the impulse response of a filter whose input is x(n) and output is d(n). Equation A-3 is derived from an approximation of an equation from the steepest descent algorithm, where the minimum error point is found by updating in the direction opposite the gradient.[1,2]

The unique characteristics of adaptive filters allow them to be used in applications such as echo cancellers, adaptive line equalization of telephone lines, noise cancelling, system modeling, prediction, deconvolution, and adaptive control.

APPENDIX B
ECHO CANCELLING WITH THE DSP56200

One popular application of adaptive filters is in the area of echo cancellation. Consider the telephone system shown in Figure B-1. A four-wire link is used for long distance transmission and is converted to a local two-wire link through a hybrid transformer. Ideally, all of the transmitted message should pass through the transformer to the two-wire link, but due to impedance mismatches, some of the signal is actually reflected into the Rx path at the hybrid. This reflection results in an audible echo received by the speaker. As the distance of transmission increases, the delay of the echo also increases.

[1] M. Bellanger, *Digital Processing of Signals*, John Wiley & Sons, New York, N.Y., 1984.
[2] B. Widrow and S. D. Stearns, *Adaptive Signal Processing*, Prentice-Hall Inc., Englewood Cliffs, N.J., 19895.

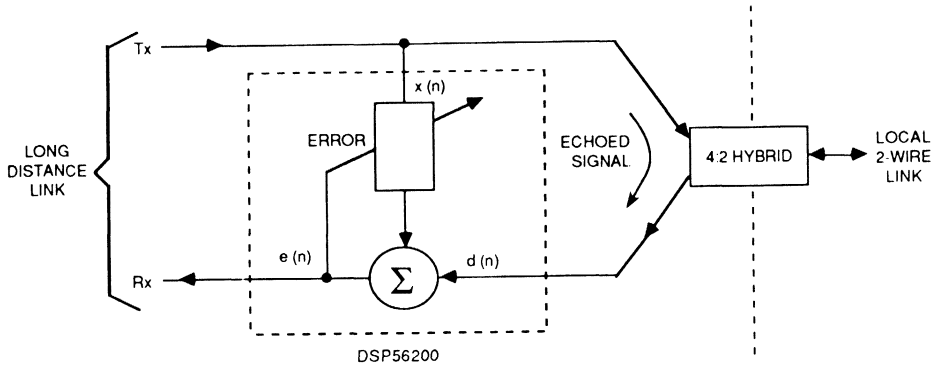


Figure B-1. Echo Canceller Application

An adaptive filter provides an excellent solution to this problem. The filter synthesizes an impulse response modeling the hybrid connection and the transmission delays. The input is passed through the FIR structure, producing a synthetic echo which is then subtracted from the actual echo. As the adaptive filter converges, the error decreases, resulting in less echo returned to the speaker.

The Motorola DSP56200 is well suited to solving the above problem. Long delays can be cancelled by a set of chips in cascade. The adaptation process can be inhibited with a control bit, eliminating any incorrect adaptation when both parties talk simultaneously, a situation called doubletalk. A programmable leakage term is included on the chip to prevent the coefficient drift which results from narrowband input signals such as tones. The DSP56200 can also be used in a similar manner to provide acoustic echo cancellation for speaker phones.

MOTOROLA

MC3417, MC3517
MC3418, MC3518

Specifications and Applications Information

CONTINUOUSLY VARIABLE SLOPE DELTA MODULATOR/DEMODULATOR

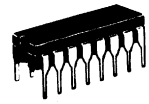
LASER-TRIMMED INTEGRATED CIRCUIT

3

CONTINUOUSLY VARIABLE SLOPE DELTA MODULATOR/DEMODULATOR

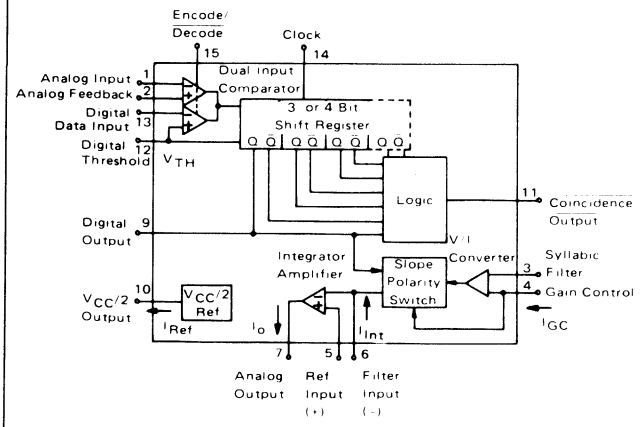
Providing a simplified approach to digital speech encoding/decoding, the MC3517/18 series of CVSDs is designed for military secure communication and commercial telephone applications. A single IC provides both encoding and decoding functions.

- Encode and Decode Functions on the Same Chip with a Digital Input for Selection
- Utilization of Compatible I^2L – Linear Bipolar Technology
- CMOS Compatible Digital Output
- Digital Input Threshold Selectable ($V_{CC}/2$ reference provided on chip)
- MC3417/MC3517 has a 3-Bit Algorithm (General Communications)
- MC3418/MC3518 has a 4-Bit Algorithm (Commercial Telephone)

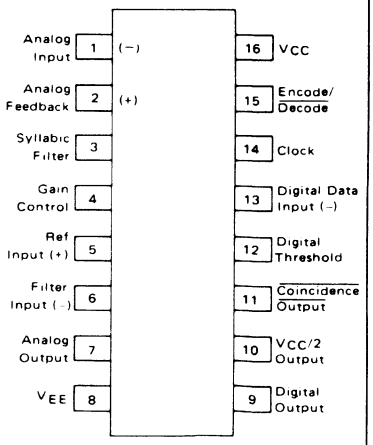


L SUFFIX
CERAMIC PACKAGE
CASE 620

CVSD BLOCK DIAGRAM



PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Temperature Range
MC3417L	Ceramic DIP	0°C to +70°C
MC3418L	Ceramic DIP	0°C to +70°C
MC3517L	Ceramic DIP	−55°C to +125°C
MC3518L	Ceramic DIP	−55°C to +125°C

DS9488R1

MAXIMUM RATINGS

(All voltages referenced to V_{EE}, T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.4 to +18	Vdc
Differential Analog Input Voltage	V_{ID}	±5.0	Vdc
Digital Threshold Voltage	V_{TH}	−0.4 to V_{CC}	Vdc
Logic Input Voltage (Clock, Digital Data, Encode/$\overline{\text{Decode}}$)	V_{Logic}	−0.4 to +18	Vdc
Coincidence Output Voltage	$V_{O(Con)}$	−0.4 to +18	Vdc
Syllabic Filter Input Voltage	$V_{I(Syl)}$	−0.4 to V_{CC}	Vdc
Gain Control Input Voltage	$V_{I(GC)}$	−0.4 to V_{CC}	Vdc
Reference Input Voltage	$V_{I(Ref)}$	V_{CC}/2 − 1.0 to V_{CC}	Vdc
V_{CC}/2 Output Current	I_{Ref}	−25	mA

ELECTRICAL CHARACTERISTICS

(V_{CC} = 12 V, V_{EE} = Gnd, T_A = 0°C to +70°C for MC3417/18, T_A = −55°C to +125°C for MC3517/18 unless otherwise noted.)

Characteristic	Symbol	MC3417/MC3517			MC3418/MC3518			Unit
		Min	Typ	Max	Min	Typ	Max	
Power Supply Voltage Range (Figure 1)	V_{CCR}	4.75	12	16.5	4.75	12	16.5	Vdc
Power Supply Current (Figure 1) (Idle Channel)	I_{CC}							mA
(V_{CC} = 5.0 V)		–	3.7	5.0	–	3.7	5.0	
(V_{CC} = 15 V)		–	6.0	10	–	6.0	10	
Clock Rate	SR	–	16 k	–	–	32 k	–	Samples/s
Gain Control Current Range (Figure 2)	I_{GCR}	0.001	–	3.0	0.001	–	3.0	mA
Analog Comparator Input Range (Pins 1 and 2) (4.75 V ≤ V_{CC} ≤ 16.5 V)	V_I	1.3	–	V_{CC} − 1.3	1.3	–	V_{CC} − 1.3	Vdc
Analog Output Range (Pin 7) (4.75 V ≤ V_{CC} ≤ 16.5 V, I_O = ± 5.0 mA)	V_O	1.3	–	V_{CC} − 1.3	1.3	–	V_{CC} − 1.3	Vdc
Input Bias Currents (Figure 3) (Comparator in Active Region)	I_{IB}							μA
Analog Input (I1)		–	0.5	1.5	–	0.25	1.0	
Analog Feedback (I2)		–	0.5	1.5	–	0.25	1.0	
Syllabic Filter Input (I3)		–	0.06	0.5	–	0.06	0.3	
Reference Input (I5)		–	−0.06	−0.5	–	−0.06	−0.3	
Input Offset Current (Comparator in Active Region)	I_{IO}							μA
Analog Input/Analog Feedback |I1 − I2| − Figure 3		–	0.15	0.6	–	0.05	0.4	
Integrator Amplifier |I5 − I6| − Figure 4		–	0.02	0.2	–	0.01	0.1	
Input Offset Voltage V/I Converter (Pins 3 and 4) − Figure 5	V_{IO}	–	2.0	6.0	–	2.0	6.0	mV
Transconductance	gm							mA/mV
V/I Converter, 0 to 3.0 mA		0.1	0.3	–	0.1	0.3	–	
Integrator Amplifier, 0 to ± 5.0 mA Load		1.0	10	–	1.0	10	–	
Propagation Delay Times (Note 1)								μs
Clock Trigger to Digital Output	t_{PLH}	–	1.0	2.5	–	1.0	2.5	
(C_L = 25 pF to Gnd)	t_{PHL}	–	0.8	2.5	–	0.8	2.5	
Clock Trigger to Coincidence Output	t_{PLH}	–	1.0	3.0	–	1.0	3.0	
(C_L = 25 pF to Gnd) (R_L = 4 kΩ to V_{CC})	t_{PHL}	–	0.8	2.0	–	0.8	2.0	
Coincidence Output Voltage − Low Logic State ($I_{OL(Con)}$ = 3.0 mA)	$V_{OL(Con)}$	–	0.12	0.25	–	0.12	0.25	Vdc
Coincidence Output Leakage Current − High Logic State (V_{OH} = 15.0 V, 0°C ≤ T_A ≤ 70°C)	$I_{OH(Con)}$	–	0.01	0.5	–	0.01	0.5	μA

NOTE 1. All propagation delay times measured 50% to 50% from the negative going (from V_{CC} to +0.4 V) edge of the clock.

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	MC3417/MC3517 Min	MC3417/MC3517 Typ	MC3417/MC3517 Max	MC3418/MC3518 Min	MC3418/MC3518 Typ	MC3418/MC3518 Max	Unit
Applied Digital Threshold Voltage Range (Pin 12)	V_{TH}	+1.2	–	V_{CC} – 2.0	+1.2	–	V_{CC} – 2.0	Vdc
Digital Threshold Input Current ($1.2\ V \leq V_{th} \leq V_{CC} - 2.0\ V$)	$I_{I(th)}$							μA
(V_{IL} applied to Pins 13, 14 and 15)		–	–	5.0	–	–	5.0	
(V_{IH} applied to Pins 13, 14 and 15)		–	– 10	–50	–	–10	–50	
Maximum Integrator Amplifier Output Current	I_O	±5.0	–	–	±5.0	–	–	mA
$V_{CC}/2$ Generator Maximum Output Current (Source only)	I_{Ref}	+10	–	–	+10	–	–	mA
$V_{CC}/2$ Generator Output Impedance (0 to +10 mA)	z_{Ref}	–	3.0	6.0	–	3.0	6.0	Ω
$V_{CC}/2$ Generator Tolerance ($4.75\ V \leq V_{CC} \leq 16.5\ V$)	ϵ_r	–	–	±3.5	–	–	±3.5	%
Logic Input Voltage (Pins 13, 14 and 15)								Vdc
Low Logic State	V_{IL}	Gnd	–	V_{th} – 0.4	Gnd	–	V_{th} – 0.4	
High Logic State	V_{IH}	V_{th} + 0.4	–	18.0	V_{th} + 0.4	–	18.0	
Dynamic Total Loop Offset Voltage (Note 2) – Figures 3, 4 and 5	ΣV_{offset}							mV
I_{GC} = 12.0 μA, V_{CC} = 12 V								
$T_A = 25^oC$		–	–	–	–	± 0.5	± 1.5	
$0^oC \leq T_A \leq +70^oC$ MC3417/18		–	–	–	–	± 0.75	± 2.3	
$-55^oC \leq T_A \leq +125^oC$ MC3517/18		–	–	–	–	± 1.5	± 4.0	
I_{GC} = 33.0 μA, V_{CC} = 12 V								
$T_A = 25^oC$		–	± 2.5	± 5.0	–	–	–	
$0^oC \leq T_A \leq +70^oC$ MC3417/18		–	± 3.0	± 7.5	–	–	–	
$-55^oC \leq T_A \leq +125^oC$ MC3517/18		–	± 4.5	± 10	–	–	–	
I_{GC} = 12.0 μA, V_{CC} = 5.0 V								
$T_A = 25^oC$		–	–	–	–	± 1.0	± 2.0	
$0^oC \leq T_A \leq +70^oC$ MC3417/18		–	–	–	–	± 1.3	± 2.8	
$-55^oC \leq T_A \leq +125^oC$ MC3517/18		–	–	–	–	± 2.5	± 5.0	
I_{GC} = 33.0 μA, V_{CC} = 5.0 V								
$T_A = 25^oC$		–	± 4.0	± 6.0	–	–	–	
$0^oC \leq T_A \leq +70^oC$ MC3417/18		–	± 4.5	± 8.0	–	–	–	
$-55^oC \leq T_A \leq +125^oC$ MC3517/18		–	± 5.5	± 10	–	–	–	
Digital Output Voltage								Vdc
(I_{OL} = 3.6 mA)	V_{OL}	–	0.1	0.4	–	0.1	0.4	
(I_{OH} = –0.35 mA)	V_{OH}	V_{CC} – 1.0	V_{CC} – 0.2	–	V_{CC} – 1.0	V_{CC} – 0.2	–	
Syllabic Filter Applied Voltage (Pin 3) (Figure 2)	$V_{I(Syl)}$	+3.2	–	V_{CC}	+3.2	–	V_{CC}	Vdc
Integrating Current (Figure 2)	$\lvert I_{Int}\rvert$							
(I_{GC} = 12.0 μA)		8.0	10	12	8.0	10	12	μA
(I_{GC} = 1.5 mA)		1.45	1.50	1.55	1.45	1.50	1.55	mA
(I_{GC} = 3.0 mA)		2.75	3.0	3.25	2.75	3.0	3.25	mA
Dynamic Integrating Current Match (I_{GC} = 1.5 mA) Figure 6	$V_{O(Ave)}$	–	± 100	± 250	–	± 100	± 250	mV
Input Current – High Logic State (V_{IH} = 18 V)	I_{IH}							μA
Digital Data Input		–	–	+5.0	–	–	+5.0	
Clock Input		–	–	+5.0	–	–	+5.0	
Encode/$\overline{\text{Decode}}$ Input		–	–	+5.0	–	–	+5.0	
Input Current – Low Logic State (V_{IL} = 0 V)	I_{IL}							μA
Digital Data Input		–	–	–10	–	–	–10	
Clock Input		–	–	–360	–	–	–360	
Encode/Decode Input		–	–	–36	–	–	–36	
Clock Input, V_{IL} = 0.4 V		–	–	–72	–	–	–72	

NOTE 2. Dynamic total loop offset (ΣV_{offset}) equals V_{IO} (comparator) (Figure 3) minus V_{IOX} (Figure 5). The input offset voltages of the analog comparator and of the integrator amplifier include the effects of input offset current through the input resistors. The slope polarity switch current mismatch appears as an average voltage across the 10 k integrator resistor. For the MC3417/MC3517, the clock frequency is 16.0 kHz. For the MC3418/MC3518, the clock frequency is 32.0 kHz. Idle channel performance is guaranteed if this dynamic total loop offset is less than one-half of the change in integrator output voltage during one clock cycle (ramp step size). Laser trimming is used to insure good idle channel performance.

DEFINITIONS AND FUNCTION OF PINS

Pin 1 – Analog Input

This is the analog comparator inverting input where the voice signal is applied. It may be ac or dc coupled depending on the application. If the voice signal is to be level shifted to the internal reference voltage, then a bias resistor between pins 1 and 10 is used. The resistor is used to establish the reference as the new dc average of the ac coupled signal. The analog comparator was designed for low hysteresis (typically less than 0.1 mV) and high gain (typically 70 dB).

Pin 2 – Analog Feedback

This is the non-inverting input to the analog signal comparator within the IC. In an encoder application it should be connected to the analog output of the encoder circuit. This may be pin 7 or a low pass filter output connected to pin 7. In a decode circuit pin 2 is not used and may be tied to $V_{CC}/2$ on pin 10, ground or left open.

The analog input comparator has bias currents of 1.5 μA max, thus the driving impedances of pins 1 and 2 should be equal to avoid disturbing the idle channel characteristics of the encoder.

Pin 3 – Syllabic Filter

This is the point at which the syllabic filter voltage is returned to the IC in order to control the integrator step size. It is an NPN input to an op amp. The syllabic filter consists of an RC network between pins 11 and 3. Typical time constant values of 6 ms to 50 ms are used in voice codecs.

Pin 4 – Gain Control Input

The syllabic filter voltage appears across C_S of the syllabic filter and is the voltage between V_{CC} and pin 3. The active voltage to current (V-I) converter drives pin 4 to the same voltage at a slew rate of typically 0.5 V/μs. Thus the current injected into pin 4 (I_{GC}) is the syllabic filter voltage divided by the R_X resistance. Figure 6 shows the relationship between I_{GC} (x-axis) and the integrating current, I_{Int} (y-axis). The discrepancy, which is most significant at very low currents, is due to circuitry within the slope polarity switch which enables trimming to a low total loop offset. The R_X resistor is then varied to adjust the loop gain of the codec, but should be no larger than 5.0 kΩ to maintain stability.

Pin 5 – Reference Input

This pin is the non-inverting input of the integrator amplifier. It is used to reference the dc level of the output signal. In an encoder circuit it must reference the same voltage as pin 1 and is tied to pin 10.

Pin 6 – Filter Input

This inverting op amp input is used to connect the integrator external components. The integrating current (I_{Int}) flows into pin 6 when the analog input (pin 1) is high with respect to the analog feedback (pin 2) in the encode mode or when the digital data input (pin 13) is high in the decode mode. For the opposite states, I_{Int} flows out of Pin 6. Single integration systems require a capacitor and resistor between pins 6 and 7. Multipole configurations will have different circuitry. The resistance between pins 6 and 7 should always be between 8 kΩ and 13 kΩ to maintain good idle channel characteristics.

Pin 7 – Analog Output

This is the integrator op amp output. It is capable of driving a 600-ohm load referenced to $V_{CC}/2$ to +6 dBm and can otherwise be treated as an op amp output. Pins 5, 6, and 7 provide full access to the integrator op amp for designing integration filter networks. The slew rate of the internally compensated integrator op amp is typically 0.5 V/μs. Pin 7 output is current limited for both polarities of current flow at typically 30 mA.

Pin 8 – V_{EE}

The circuit is designed to work in either single or dual power supply applications. Pin 8 is always connected to the most negative supply.

Pin 9 – Digital Output

The digital output provides the results of the delta modulator's conversion. It swings between V_{CC} and V_{EE} and is CMOS or TTL compatible. Pin 9 is inverting with respect to pin 1 and non-inverting with respect to pin 2. It is clocked on the falling edge of pin 14. The typical 10% to 90% rise and fall times are 250 ns and 50 ns respectively for V_{CC} = 12 V and C_L = 25 pF to ground.

Pin 10 – $V_{CC}/2$ Output

An internal low impedance mid-supply reference is provided for use of the MC3417/18 in single supply applications. The internal regulator is a current source and must be loaded with a resistor to insure its sinking capability. If a +6 dBmo signal is expected across a 600 ohm input bias resistor, then pin 10 must sink 2.2 V/600 Ω = 3.66 mA. This is only possible if pin 10 sources 3.66 mA into a resistor normally and will source only the difference under peak load. The reference load resistor is chosen accordingly. A 0.1 μF bypass capacitor from pin 10 to V_{EE} is also recommended. The $V_{CC}/2$ reference is capable of sourcing 10 mA and can be used as a reference elsewhere in the system circuitry.

Pin 11 – $\overline{\text{Coincidence Output}}$

The duty cycle of this pin is proportional to the voltage across C_S. The coincidence output will be low whenever the content of the internal shift register is all 1s or all 0s. In the MC3417 the register is 3 bits long

DEFINITIONS AND FUNCTIONS OF PINS (continued)

while the MC3418 contains a 4 bit register. Pin 11 is an open collector of an NPN device and requires a pull-up resistor. If the syllabic filter is to have equal charge and discharge time constants, the value of R_P should be much less than R_S. In systems requiring different charge and discharge constants, the charging constant is $R_S C_S$ while the decaying constant is $(R_S + R_P)C_S$. Thus longer decays are easily achievable. The NPN device should not be required to sink more than 3 mA in any configuration. The typical 10% to 90% rise and fall times are 200 ns and 100 ns respectively for R_L = 4 kΩ to +12 V and C_L = 25 pF to ground.

Pin 12 – Digital Threshold

This input sets the switching threshold for pins 13, 14, and 15. It is intended to aid in interfacing different logic families without external parts. Often it is connected to the $V_{CC}/2$ reference for CMOS interface or can be biased two diode drops above V_{EE} for TTL interface.

Pin 13 – Digital Data Input

In a decode application, the digital data stream is applied to pin 13. In an encoder it may be unused or may be used to transmit signaling message under the control of pin 15. It is an inverting input with respect to pin 9. When pins 9 and 13 are connected, a toggle flip-flop is formed and a forced idle channel pattern can be transmitted. The digital data input level should be maintained for 0.5 μs before and after the clock trigger for proper clocking.

Pin 14 – Clock Input

The clock input determines the data rate of the codec circuit. A 32K bit rate requires a 32 kHz clock. The switching threshold of the clock input is set by pin 12. The shift register circuit toggles on the falling edge of the clock input. The minimum width for a positive-going pulse on the clock input is 300 ns, whereas for a negative-going pulse, it is 900 ns.

Pin 15 – Encode/$\overline{\text{Decode}}$

This pin controls the connection of the analog input comparator and the digital input comparator to the internal shift register. If high, the result of the analog comparison will be clocked into the register on the falling edge at pin 14. If low, the digital input state will be entered. This allows use of the IC as an encoder/decoder or simplex codec without external parts. Furthermore, it allows non-voice patterns to be forced onto the transmission line through pin 13 in an encoder.

Pin 16 – V_{CC}

The power supply range is from 4.75 to 16.5 volts between pin V_{CC} and V_{EE}.

FIGURE 1 – POWER SUPPLY CURRENT

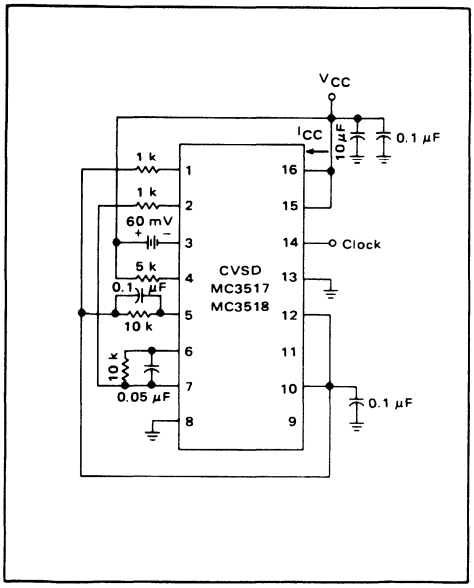
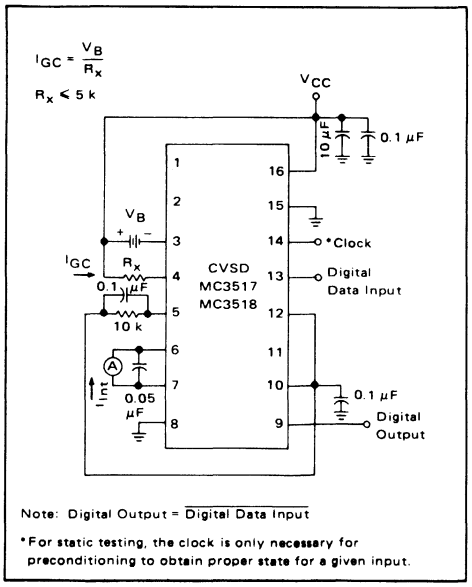


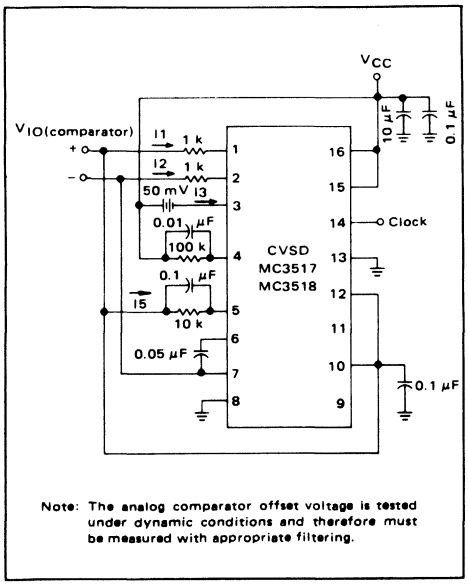
FIGURE 2 – I_{GCR}, GAIN CONTROL RANGE and I_{Int} – INTEGRATING CURRENT



Note: Digital Output = $\overline{\text{Digital Data Input}}$

*For static testing, the clock is only necessary for preconditioning to obtain proper state for a given input.

FIGURE 3 – INPUT BIAS CURRENTS, ANALOG COMPARATOR OFFSET VOLTAGE AND CURRENT



Note: The analog comparator offset voltage is tested under dynamic conditions and therefore must be measured with appropriate filtering.

FIGURE 4 – INTEGRATOR AMPLIFIER OFFSET VOLTAGE AND CURRENT

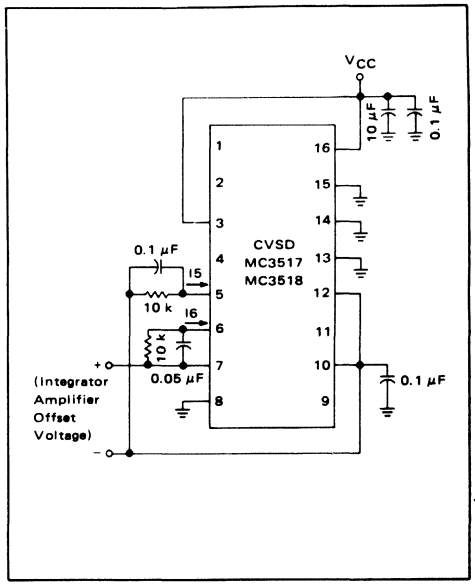
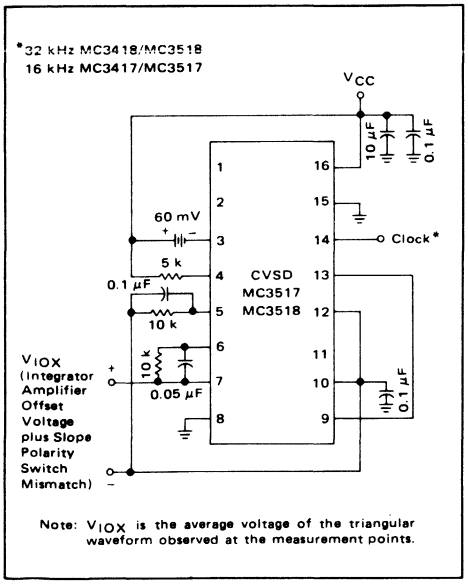
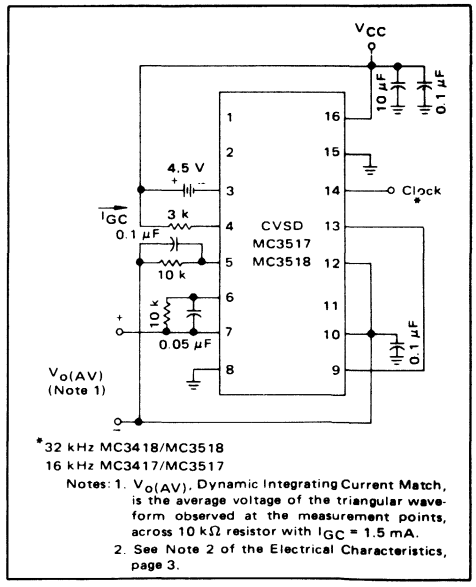


FIGURE 5 – V/I CONVERTER OFFSET VOLTAGE, V_{IO} and V_{IOX}



Note: V_{IOX} is the average voltage of the triangular waveform observed at the measurement points.

FIGURE 6 – DYNAMIC INTEGRATING CURRENT MATCH



*32 kHz MC3418/MC3518
16 kHz MC3417/MC3517

Notes: 1. $V_{O(AV)}$, Dynamic Integrating Current Match, is the average voltage of the triangular waveform observed at the measurement points, across 10 kΩ resistor with I_{GC} = 1.5 mA.

2. See Note 2 of the Electrical Characteristics, page 3.

TYPICAL PERFORMANCE CURVES

FIGURE 7 – TYPICAL I_{Int} versus I_{GC} (Mean ± 2σ)

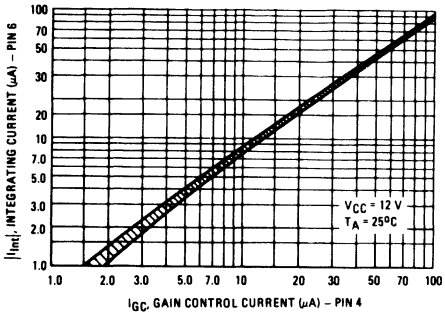


FIGURE 8 – NORMALIZED DYNAMIC INTEGRATING CURRENT MATCH versus V_{CC}

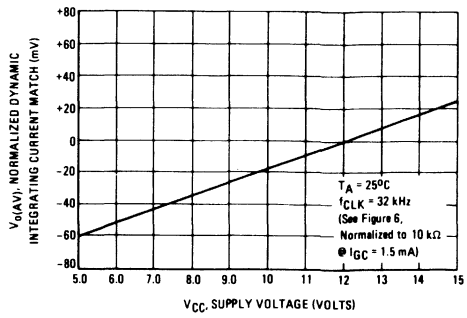


FIGURE 9 – NORMALIZED DYNAMIC INTEGRATING CURRENT MATCH versus CLOCK FREQUENCY

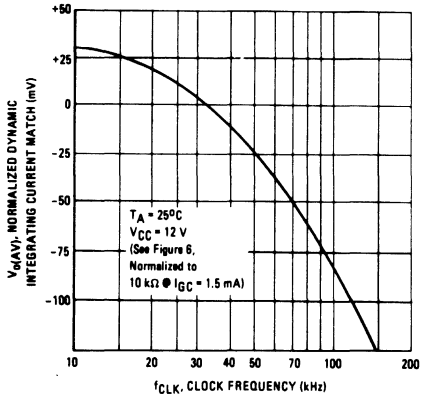


FIGURE 10 – DYNAMIC TOTAL LOOP OFFSET versus CLOCK FREQUENCY

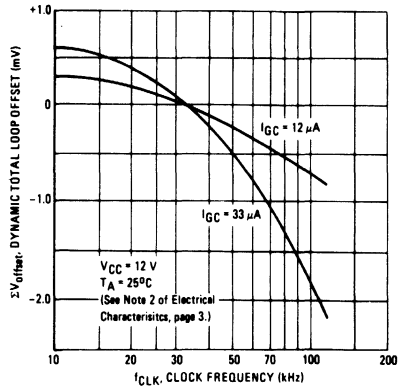


FIGURE 11 – BLOCK DIAGRAM OF THE CVSD ENCODER

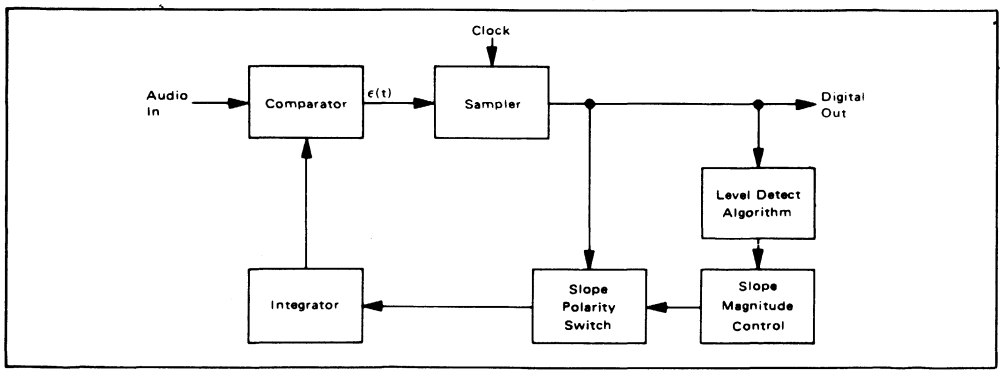


FIGURE 12 – CVSD WAVEFORMS

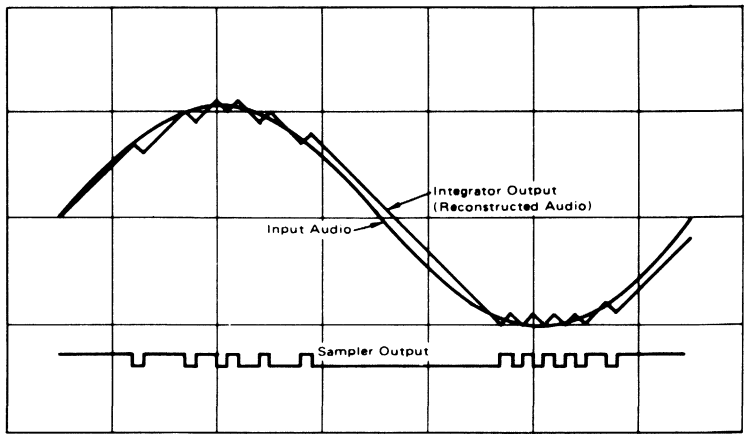


FIGURE 13 – BLOCK DIAGRAM OF THE CVSD DECODER

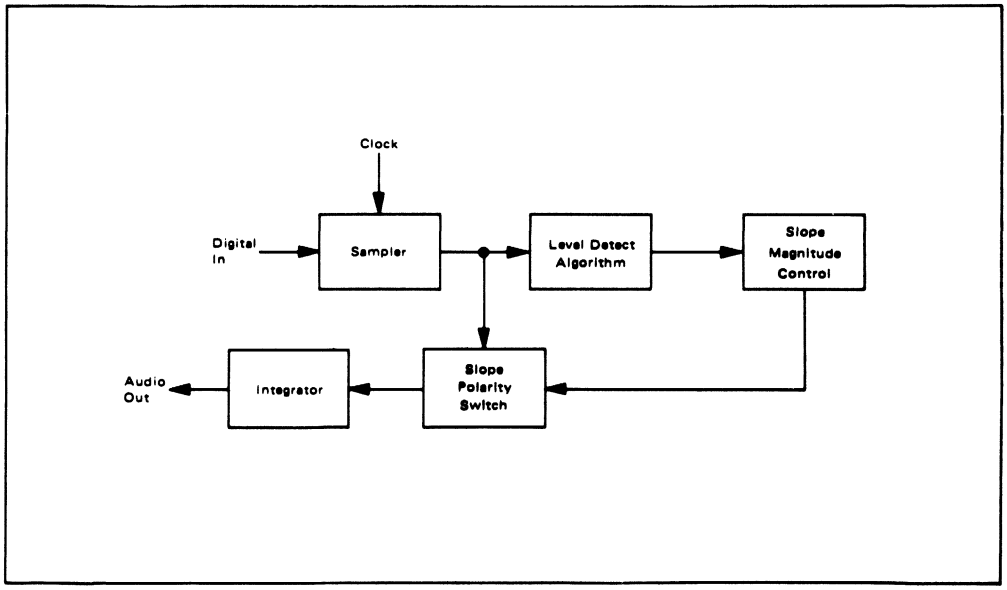
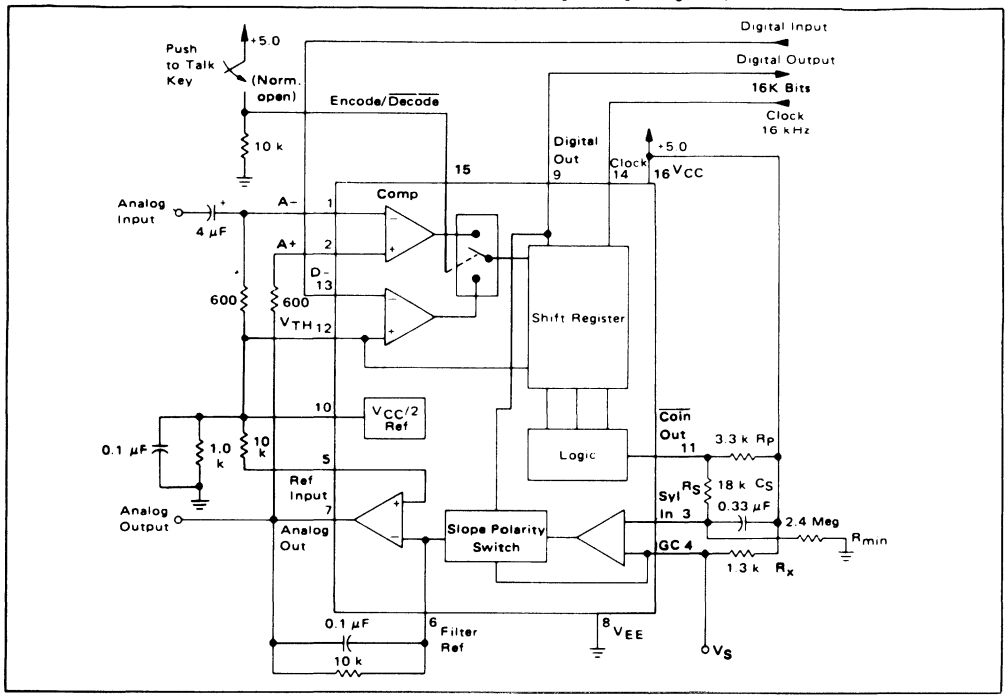


FIGURE 14 – 16 kHz SIMPLEX VOICE CODEC
(Using MC3417, Single Pole Companding and Single Integration)



CIRCUIT DESCRIPTION

The continuously variable slope delta modulator (CVSD) is a simple alternative to more complex conventional conversion techniques in systems requiring digital communication of analog signals. The human voice is analog, but digital transmission of any signal over great distance is attractive. Signal/noise ratios do not vary with distance in digital transmission and multiplexing, switching and repeating hardware is more economical and easier to design. However, instrumentation A to D converters do not meet the communications requirements. The CVSD A to D is well suited to the requirements of digital communications and is an economically efficient means of digitizing analog inputs for transmission.

The Delta Modulator

The innermost control loop of a CVSD converter is a simple delta modulator. A block diagram CVSD Encoder is shown in Figure 11. A delta modulator consists of a comparator in the forward path and an integrator in the feedback path of a simple control loop. The inputs to the comparator are the input analog signal and the integrator output. The comparator output reflects the sign of the difference between the input voltage and the integrator output. That sign bit is the digital output and also controls the direction of ramp in the integrator. The comparator is normally clocked so as to produce a synchronous and band limited digital bit stream.

If the clocked serial bit stream is transmitted, received, and delivered to a similar integrator at a remote point, the remote integrator output is a copy of the transmitting control loop integrator output. To the extent that the integrator at the transmitting locations tracks the input signal, the remote receiver reproduces the input signal. Low pass filtering at the receiver output will eliminate most of the quantizing noise, if the clock rate of the bit stream is an octave or more above the bandwidth of the input signal. Voice bandwidth is 4 kHz and clock rates from 8 k and up are possible. Thus the delta modulator digitizes and transmits the analog input to a remote receiver. The serial, unframed nature of the data is ideal for communications networks. With no input at the transmitter, a continuous one zero alternation is transmitted. If the two integrators are made leaky, then during any loss of contact the receiver output decays to

CIRCUIT DESCRIPTION (continued)

zero and receive restart begins without framing when the receiver reacquires. Similarly a delta modulator is tolerant of sporadic bit errors. Figure 12 shows the delta modulator waveforms while Figure 13 shows the corresponding CVSD decoder block diagram.

The Companding Algorithm

The fundamental advantages of the delta modulator are its simplicity and the serial format of its output. Its limitations are its ability to accurately convert the input within a limited digital bit rate. The analog input must be band limited and amplitude limited. The frequency limitations are governed by the nyquist rate while the amplitude capabilities are set by the gain of the integrator.

The frequency limits are bounded on the upper end; that is, for any input bandwidth there exists a clock frequency larger than that bandwidth which will transmit the signal with a specific noise level. However, the amplitude limits are bounded on both upper and lower ends. For a signal level, one specific gain will achieve an optimum noise level. Unfortunately, the basic delta modulator has a small dynamic range over which the noise level is constant.

The continuously variable slope circuitry provides increased dynamic range by adjusting the gain of the integrator. For a given clock frequency and input bandwidth the additional circuitry increases the delta modulator's dynamic range. External to the basic delta modulator is an algorithm which monitors the past few outputs of the delta modulator in a simple shift register. The register is 3 or 4 bits long depending on the application. The accepted CVSD algorithm simply monitors the contents of the shift register and indicates if it contains all 1s or 0s. This condition is called coincidence. When it occurs, it indicates that the gain of the integrator is too small. The coincidence output charges a single pole low pass filter. The voltage output of this syllabic filter controls the integrator gain through a pulse amplitude modulator whose other input is the sign bit or up/down control.

The simplicity of the all ones, all zeros algorithm should not be taken lightly. Many other control algorithms using the shift register have been tried. The key to the accepted algorithm is that it provides a measure of the average power or level of the input signal. Other techniques provide more instantaneous information about the shape of the input curve. The purpose of the algorithm is to control the gain of the integrator and to increase the dynamic range. Thus a measure of the average input level is what is needed.

The algorithm is repeated in the receiver and thus the level data is recovered in the receiver. Because the algorithm only operates on the past serial data, it changes the nature of the bit stream without changing the channel bit rate.

The effect of the algorithm is to compand the input signal. If a CVSD encoder is played into a basic delta modulator, the output of the delta modulator will reflect the shape of the input signal but all of the output will be at an equal level. Thus the algorithm at the output is needed to restore the level variations. The bit stream in the channel is as if it were from a standard delta modulator with a constant level input.

The delta modulator encoder with the CVSD algorithm provides an efficient method for digitizing a voice input in a manner which is especially convenient for digital communciations requirements.

APPLICATIONS INFORMATION

CVSD DESIGN CONSIDERATIONS

A simple CVSD encoder using the MC3417 or MC3418 is shown in Figure 14. These ICs are general purpose CVSD building blocks which allow the system designer to tailor the encoder's transmission characteristics to the application. Thus, the achievable transmission capabilities are constrained by the fundamental limitations of delta modulation and the design of encoder parameters. The performance is not dictated by the internal configuration of the MC3417 and MC3418. There are seven design considerations involved in designing these basic CVSD building blocks into a specific codec application.

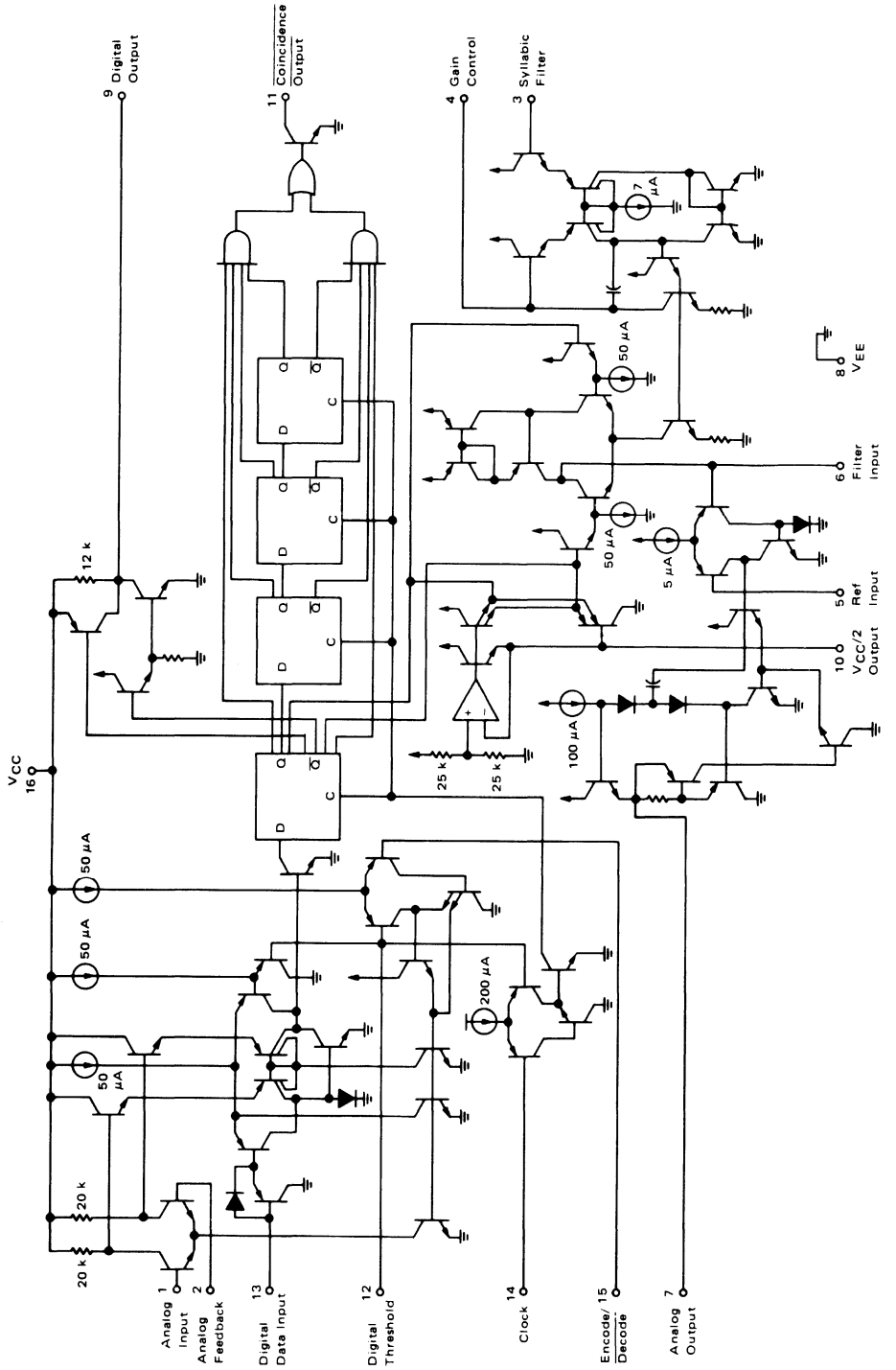
These are listed below:

1. Selection of clock rate
2. Required number of shift register bits
3. Selection of loop gain
4. Selection of minimum step size
5. Design of integration filter transfer function
6. Design of syllabic filter transfer function
7. Design of low pass filter at the receiver

The circuit in Figure 14 is the most basic CVSD circuit possible. For many applications in secure radio or other intelligible voice channel requirements, it is entirely sufficient. In this circuit, items 5 and 6 are reduced to their simplest form. The syllabic and integration filters are both single pole networks. The selection of items 1 through 4 govern the codec performance.

3

CVSD CIRCUIT SCHEMATIC



CVSD DESIGN CONSIDERATIONS (continued)

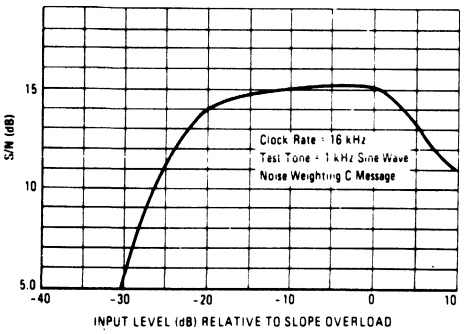
Layout Considerations

Care should be exercised to isolate all digital signal paths (pins 9, 11, 13, and 14) from analog signal paths (pins 1-7 and 10) in order to achieve proper idle channel performance.

Clock Rate

With minor modifications the circuit in Figure 14 may be operated anywhere from 9.6 kHz to 64 kHz clock rates. Obviously the higher the clock rate the higher the S/N performance. The circuit in Figure 14 typically produces the S/N performance shown in Figure 15. The selection of clock rate is usually dictated by the bandwidth of the transmission medium. Voice bandwidth systems will require no higher than 9600 Hz. Some radio systems will allow 12 kHz. Private 4-wire telephone systems are often operated at 16 kHz and commercial telephone performance can be achieved at 32K bits and above. Other codecs may use bit rates up to 200K bits/sec.

FIGURE 15 – SIGNAL-TO-NOISE PERFORMANCE OF MC3417 WITH SINGLE INTEGRATION, SINGLE-POLE AND COMPANDING AT 16K BITS – TYPICAL



Shift Register Length (Algorithm)

The MC3417 has a three-bit algorithm and the MC3418 has a four-bit algorithm. For clock rates of 16 kHz and below, the 3-bit algorithm is well suited. For 32 kHz and higher clock rates, the 4-bit system is preferred. Since the algorithm records a fixed past history of the input signal, a longer shift register is required to obtain the same internal hsitory. At 16 bits and below, the 4-bit algorithm will produce a slightly wider dynamic range at the expense of level change response. Basically the MC3417 is designed for low bit rate systems and the MC3418 is intended for high performance, high bit rate system. At bit rates above 64K bits either part will work well.

Selection of Loop Gain

The gain of the circuit in Figure 14 is set by resistor R_X. R_X must be selected to provide the proper integrator step size for high level signals such that the companding ratio does not exceed about 25%. The companding ratio is the active low duty cycle of the coincidence output on pin 11 of the codec circuit. Thus the system gain is dependent on:

1. The maximum level and frequency of the input signal.
2. The transfer function of the integration filter.

For voice codecs the typical input signal is taken to be a sine wave at 1 kHz of 0 dBmo level. In practice, the useful dynamic range extends about 6 dB above the design level. In any system the companding ratio should not exceed 30%.

To calculate the required step size current, we must describe the transfer characteristics of the integration filter. In the basic circuit of Figure 14, a single pole of 160 Hz is used.

$$R = 10\ k\Omega,\ C = 0.1\ \mu F$$

$$\frac{V_o}{I_i} = \frac{1}{C(S + 1/RC)} \equiv \frac{K}{S + \omega_o}$$

$$\omega_o = 2\pi f$$

$$10^3 = \omega_o = 2\pi f$$

$$f = 159.2\ Hz$$

Note that the integration filter produces a single-pole response from 300 to 3 kHz. The current required to move the integrator output a specific voltage from zero is simply:

$$I_i = \frac{V_o}{R} + \frac{C_d V_o}{dt}$$

Now a 0 dBmo sine wave has a peak value of 1.0954 volts. In 1/8 of a cycle of a sine wave centered around the zero crossing, the sine wave changes by approximately its peak value. The CVSD step should trace that change. The required current for a 0 dBm 1 kHz sine wave is:

$$I_i = \frac{1.1\ V}{*2(10\ k\Omega)} + \frac{0.1\ \mu F(1.1)}{0.125\ ms} = 0.935\ mA$$

*The maximum voltage across RI when maximum slew is required is:

$$\frac{1.1\ V}{2}$$

Now the voltage range of the syllabic filter is the power supply voltage, thus:

$$R_X = 0.25(V_{CC})\ \frac{1}{0.935\ mA}$$

A similar procedure can be followed to establish the proper gain for any input level and integration filter type.

CVSD DESIGN CONSIDERATIONS (continued)

Minimum Step Size

The final parameter to be selected for the simple codec in Figure 14 is idle channel step size. With no input signal, the digital output becomes a one-zero alternating pattern and the analog output becomes a small triangle wave. Mismatches of internal currents and offsets limit the minimum step size which will produce a perfect idle channel pattern. The MC3417 is tested to ensure that a 20 mVp-p minimum step size at 16 kHz will attain a proper idle channel. The idle channel step size must be twice the specified total loop offset if a one-zero idle pattern is desired. In some applications a much smaller minimum step size (e.g., 0.1 mV) can produce quiet performance without providing a 1-0 pattern.

To set the idle channel step size, the value of R_{min} must be selected. With no input signal, the slope control algorithm is inactive. A long series of ones or zeros never occurs. Thus, the voltage across the syllabic filter capacitor (C_S) would decay to zero. However, the voltage divider of R_S and R_{min} (see Figure 14) sets the minimum allowed voltage across the syllabic filter capacitor. That voltage must produce the desired ramps at the analog output. Again we write the filter input current equation:

$$I_i = \frac{V_o}{R} + C\frac{dV_o}{dt}$$

For values of V_o near $V_{CC}/2$ the V_o/R term is negligible; thus

$$I_i = C_S\frac{\Delta V_o}{\Delta T}$$

where ΔT is the clock period and ΔV_o is the desired peak-to-peak value of the idle output. For a 16K-bit system using the circuit in Figure 14

$$I_i = \frac{0.1\,\mu F\ \ 20\,mV}{62.5\,\mu s} = 33\,\mu A$$

The voltage on C_S which produces a 33 μA current is determined by the value of R_x.

$$I_i R_x = V_{Smin};\ \text{for } 33\,\mu A,\ V_{Smin} = 41.6\,mV$$

In Figure 14 R_S is 18 kΩ. That selection is discussed with the syllabic filter considerations. The voltage divider of R_S and R_{min} must produce an output of 41.6 mV.

$$V_{CC}\frac{R_S}{R_S + R_{min}} = V_{Smin} \qquad R_{min} \simeq 2.4\,M\Omega$$

Having established these four parameters — clock rate, number of shift register bits, loop gain and minimum step size — the encoder circuit in Figure 14 will function at near optimum performance for input levels around 0 dBm.

INCREASING CVSD PERFORMANCE

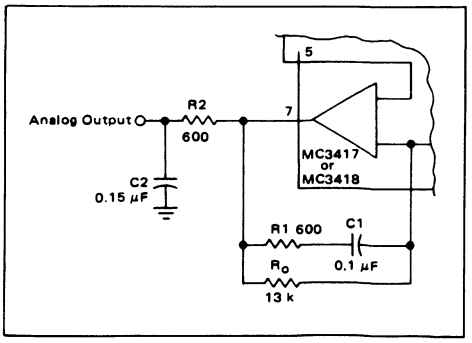
Integration Filter Design

The circuit in Figure 14 uses a single-pole integration network formed with a 0.1 μF capacitor and a 10 kΩ resistor. It is possible to improve the performance of the circuit in Figure 14 by 1 or 2 dB by using a two-pole integration network. The improved circuit is shown.

The first pole is still placed below 300 Hz to provide the 1/S voice content curve and a second pole is placed somewhere above the 1 kHz frequency. For telephony circuits, the second pole can be placed above 1.8 kHz to exceed the 1633 touchtone frequency. In other communication systems, values as low as 1 kHz may be selected. In general, the lower in frequency the second pole is placed, the greater the noise improvement. Then, to ensure the encoder loop stability, a zero is added to keep the phase shift less than 180°. This zero should be placed slightly above the low-pass output filter break frequency so as not to reduce the effectiveness of the second pole. A network of 235 Hz, 2 kHz and 5.2 kHz is typical for telephone applications while 160 Hz, 1.2 kHz and 2.8 kHz might be used in voice only channels. (Voice only channels can use an output low-pass filter which breaks at about 2.5 kHz.) The two-pole network in Figure 16 has a transfer function of:

$$\frac{V_o}{I_i} = \frac{R_0R_1\left(S + \frac{1}{R_1C_1}\right)}{R_2C_2(R_0 + R_1)\left(S + \frac{1}{(R_0 + R_1)C_1}\right)S + \left(\frac{1}{R_2C_2}\right)}$$

FIGURE 16 – IMPROVED FILTER CONFIGURATION



These component values are for the telephone channel circuit poles described in the text. The R2, C2 product can be provided with different values of R and C. R2 should be chosen to be equal to the termination resistor on pin 1.

INCREASING CVSD PERFORMANCE (continued)

Thus the two poles and the zero can be selected arbitrarily as long as the zero is at a higher frequency than the first pole. The values in Figure 16 represent one implementation of the telephony filter requirement.

The selection of the two-pole filter network effects the selection of the loop gain value and the minimum step size resistor. The required integrator current for a given change in voltage now becomes:

$$I_i = \frac{V_o}{R_0} + \left(\frac{R_2C_2}{R_0} + \frac{R_1C_1}{R_0} + C_1\right)\frac{\Delta V_o}{\Delta T} + \left(R_2C_2C_1 + \frac{R_1C_1R_2C_2}{R_0}\right)\frac{\Delta V_o^2}{\Delta T^2}.$$

The calculation of desired gain resistor R_X then proceeds exactly as previously described.

Syllabic Filter Design

The syllabic filter in Figure 14 is a simple single-pole network of 18 kΩ and 0.33 μF. This produces a 6.0 ms time constant for the averaging of the coincidence output signal. The voltage across the capacitor determines the integrator current which in turn establishes the step size. The integrator current and the resulting step size determine the companding ratio and the S/N performance. The companding ratio is defined as the voltage across C_S/V_{CC}.

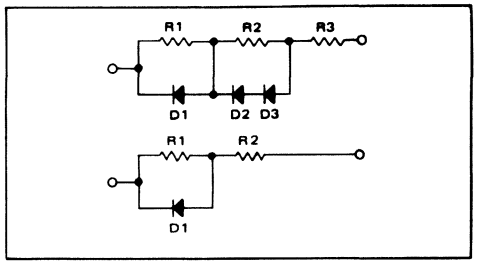
The S/N performance may be improved by modifying the voltage to current transformation produced by R_X. If different portions of the total R_X are shunted by diodes, the integrator current can be other than $(V_{CC} - V_S)/R_X$. These breakpoint curves must be designed experimentally for the particular system application. In general, one would wish that the current would double with input level. To design the desired curve, supply current to pin 4 of the codec from an external source. Input a signal level and adjust the current until the S/N performance is optimum. Then record the syllabic filter voltage and the current. Repeat this for all desired signal levels. Then derive the resistor diode network which produces that curve on a curve tracer.

Once the network is designed with the curve tracer, it is then inserted in place of R_X in the circuit and the forced optimum noise performance will be achieved from the active syllabic algorithm.

Diode breakpoint networks may be very simple or moderately complex and can improve the usable dynamic range of any codec. In the past they have been used in high performance telephone codecs.

Typical resistor-diode networks are shown in Figure 17.

FIGURE 17 – RESISTOR-DIODE NETWORKS



If the performance of more complex diode networks is desired, the circuit in Figure 18 should be used. It simulates the companding characteristics of nonlinear R_X elements in a different manner.

Output Low Pass Filter

A low pass filter is required at the receiving circuit output to eliminate quantizing noise. In general, the lower the bit rate, the better the filter must be. The filter in Figure 20 provides excellent performance for 12 kHz to 40 kHz systems.

TELEPHONE CARRIER QUALITY CODEC USING MC3418

Two specifications of the integrated circuit are specifically intended to meet the performance requirements of commercial telephone systems. First, slope polarity switch current matching is laser trimmed to guarantee proper idle channel performance with 5 mV minimum step size and a typical 1% current match from 15 μA to 3 mA. Thus a 300 to 1 range of step size variation is possible. Second, the MC3418 provides the four-bit algorithm currently used in subscriber loop telephone systems. With these specifications and the circuit of Figure 18, a telephone quality codec can be mass produced.

The circuit in Figure 18 provides a 30 dB S/Nc ratio over 50 dB of dynamic range for a 1 kHz test tone at a 37.7K bit rate. At 37.7K bits, 40 voice channels may be multiplexed on a standard 1.544 megabit T1 facility. This codec has also been tested for 10^{-7} error rates with asynchronous and synchronous data up to 2400 baud and for reliable performance with DTMF signaling. Thus, the design is applicable in telephone quality subscriber loop carrier systems, subscriber loop concentrators and small PABX installations.

The Active Companding Network

The unique feature of the codec in Figure 18 is the step size control circuit which uses a companding ratio reference, the present step size, and the present syllabic filter output to establish the optimum companding ratios and step sizes for any given input level. The companding ratio of a CVSD codec is defined as the duty cycle of the coincidence output. It is the parameter measured by the syllabic filter and is the voltage across C_S divided by the voltage swing of the coincidence output. In Figure 18, the voltage swing of pin 11 is 6 volts. The operating companding ratio is analoged by the voltage between pins 10 and 4 by means of the virtual short across pins 3 and 4 of the V to I op amp within the integrated circuit. Thus, the instantaneous companding ratio of the codec is always available at the negative input of A1.

The diode D1 and the gain of A1 and A2 provide a companding ratio reference for any input level. If the output of A2 is more than 0.7 volts below $V_{CC}/2$, then the positive input of A1 is ($V_{CC}/2$ – 0.7). The on diode drop at the input of A1 represents a 12% companding ratio (12% = 0.7 V/6 V).

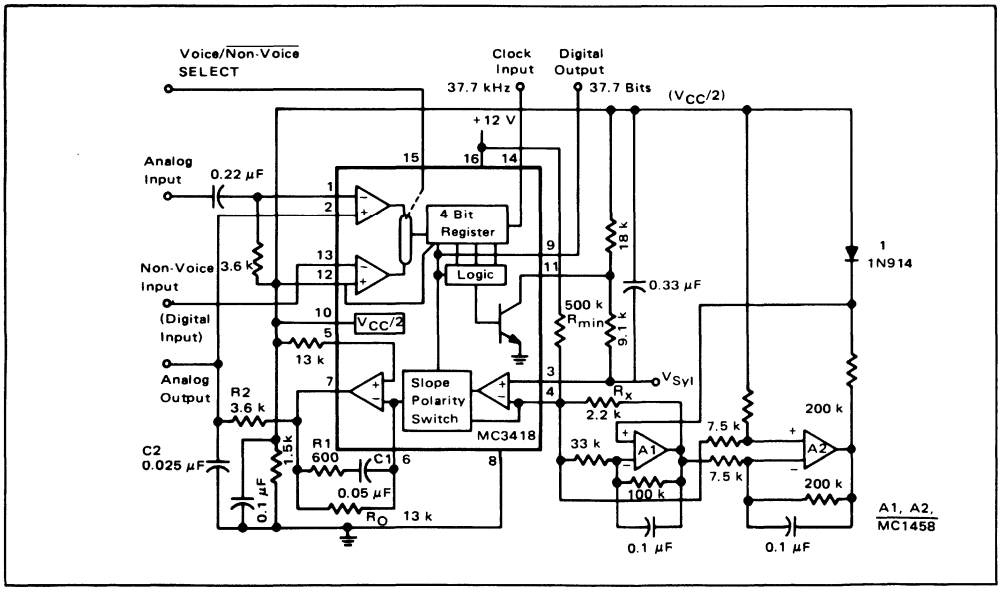
The present step size of the operating codec is directly related to the voltage across R_X, which established the integrator current. In Figure 18, the voltage across R_X is amplified by the differential amplifier A2 whose output is single ended with respect to pin 10 of the IC.

For large signal inputs, the step size is large and the output of A2 is lower than 0.7 volts. Thus D1 is fully on. The present step size is not a factor in the step size control. However, the difference between 12% companding ratio and the instantaneous companding ratio at pin 4 is amplified by A1. The output of A1 changes the voltage across R_X in a direction which reduces the difference between the companding reference and the operating ratio by changing the step size. The ratio of R4 and R3 determines how closely the voltage at pin 4 will be forced to 12%. The selection of R3 and R4 is initially experimental. However, the resulting companding control is dependent on R_X, R3, R4, and the full diode drop D1. These values are easy to reproduce from codec to codec.

For small input levels, the companding ratio reference becomes the output of A2 rather than the diode drop. The operating companding ratio on pin 4 is then compared to a companding ratio smaller than 12% which is determined by the voltage drop across R_X and the gain of A2

FIGURE 18 – TELEPHONE QUALITY DELTAMOD CODER

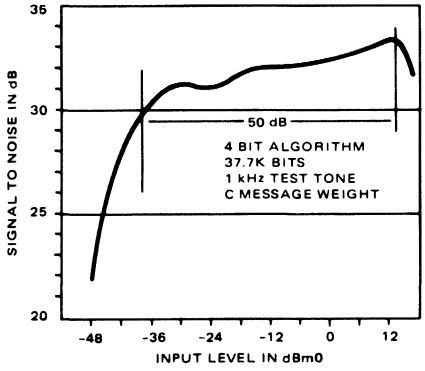
(Both double integration and active companding control are used to obtain improved CVSD performance. Laser trimming of the integrated circuit provides reliable idle channel and step size range characteristics.)



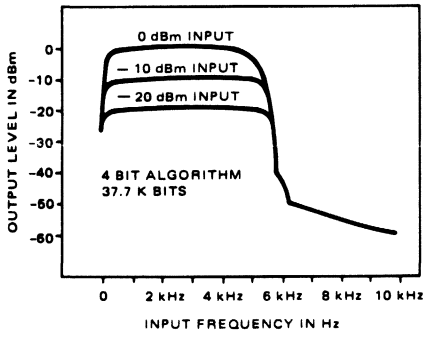
TELEPHONE CARRIER QUALITY CODEC USING MC3418 (continued)

FIGURE 19 – SIGNAL-TO-NOISE PERFORMANCE AND FREQUENCY RESPONSE
(Showing the improvement realized with the circuit in Figure 18.)

a. SIGNAL-TO-NOISE PERFORMANCE OF TELEPHONY QUALITY DELTAMODULATOR



b. FREQUENCY RESPONSE versus INPUT LEVEL (SLOPE OVERLOAD CHARACTERISTIC)



and A1. The gain of A2 is also experimentally determined, but once determined, the circuitry is easily repeated.

With no input signal, the companding ratio at pin 4 goes to zero and the voltage across R_X goes to zero. The voltage at the output of A2 becomes zero since there is no drop across R_X. With no signal input, the actively controlled step size vanished.

The minimum step size is established by the 500 k resistor between V_{CC} and $V_{CC}/2$ and is therefore independently selectable.

The signal to noise results of the active companding network are shown in Figure 19. A smooth 2 dB drop is realized from +12 dBm to -24 under the control of A1. At -24 dBm, A2 begins to degenerate the companding reference and the resulting step size is reduced so as to extend the dynamic range of the codec by 20 dBm.

The slope overload characteristic is also shown. The active companding network produces improved performance with frequency. The 0 dBm slope overload point is raised to 4.8 kHz because of the gain available in controlling the voltage across R_X. The curves demonstrate that the level linearity has been maintained or improved.*

The codec in Figure 18 is designed specifically for 37.7K bit systems. However, the benefits of the active companding network are not limited to high bit rate systems. By modifying the crossover region (changing the gain of A2), the active technique may be used to improve the performance of lower bit rate systems.

The performance and repeatability of the codec in Figure 18 represents a significant step forward in the art and cost of CVSD codec designs.

*A larger value for C2 is required in the decoder circuit than in the encoder to adjust the level linearity with frequency. In Figure 18, 0.050 μF would work well.

FIGURE 20 – HIGH PERFORMANCE ELLIPTIC FILTER FOR CVSD OUTPUT

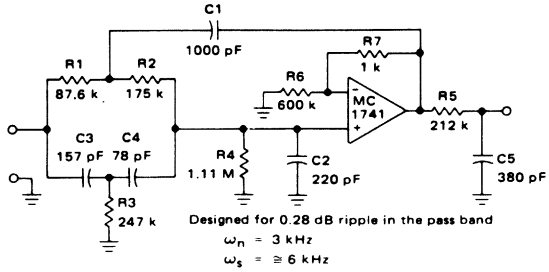
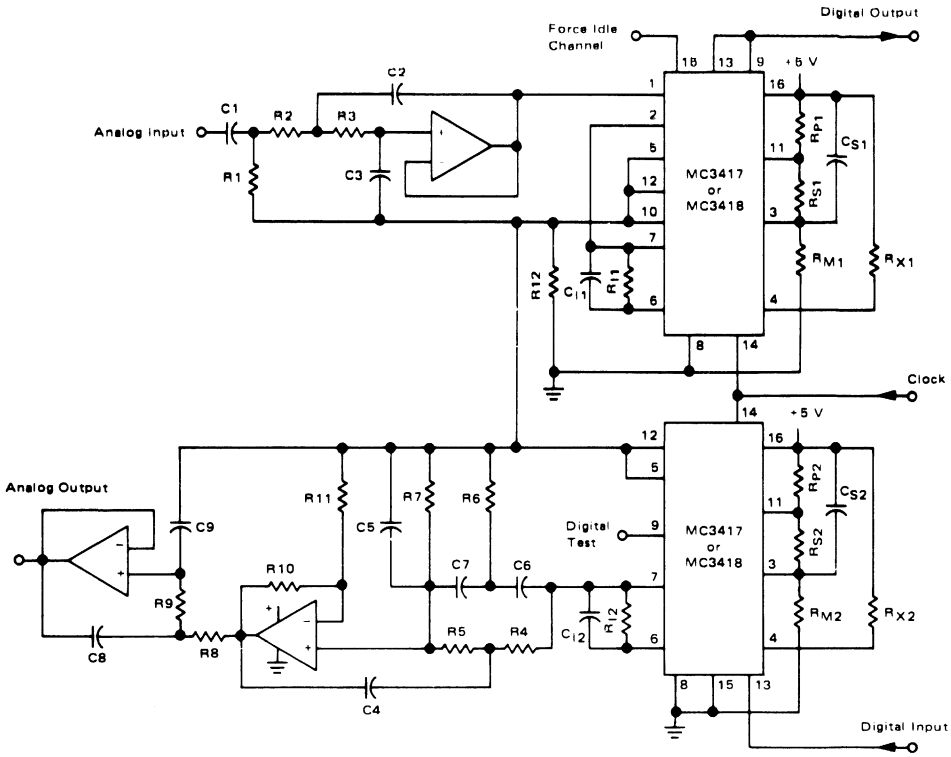


FIGURE 21 – FULL DUPLEX/32K BIT CVSD VOICE CODEC USING MC3517/18 AND MC3503/6 OP AMP



Codec Components

R_{X1}, R_{X2} – 3.3 kΩ
R_{P1}, R_{P2} – 3.3 kΩ
R_{S1}, R_{S2} – 100 kΩ
R_{I1}, R_{I2} – 20 kΩ
R_{12} – 1 kΩ
R_{M1}, R_{M2} – 5 MΩ (MC3417)
Minimum step size = 20 mV
R_{M1}, R_{M2} – 15 MΩ (MC3418)
Minimum step size = 6 mV

C_{S1}, C_{S2} – 0.05 μF
C_{I1}, C_{I2} – 0.05 μF

2 MC3417 (or MC3418)
1 MC3403 (or MC3406)

Note: All Res. 5%
All Cap. 5%

Input Filter Specifications

12 dB/Octave Rolloff above 3.3 kHz
6 dB/Octave Rolloff below 50 Hz

Output Filter Specifications

Break Frequency – 3.3 kHz
Stop Band – 9 kHz
Stop Band Atten. – 50 dB
Rolloff – > 40 dB/Octave

Filter Components

R1 – 965 Ω
R2 – 72 kΩ
R3 – 72 kΩ
R4 – 63.46 kΩ
R5 – 127 kΩ
R6 – 365.5 kΩ
R7 – 1.645 MΩ
R8 – 72 kΩ
R9 – 72 kΩ
R10 – 29.5 kΩ
R11 – 72 kΩ

C1 – 3.3 μF
C2 – 837 pF
C3 – 536 pF
C4 – 1000 pF
C5 – 222 pF
C6 – 77 pF
C7 – 38 pF
C8 – 837 pF
C9 – 536 pF

Note: All Res. 0.1% to 1%.
All Cap. 1.0%

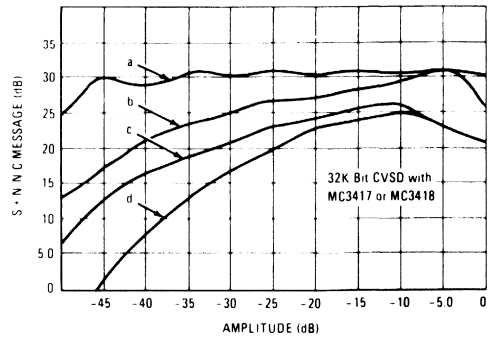
COMPARATIVE CODEC PERFORMANCE

The salient feature of CVSD codecs using the MC3517 and MC3518 family is versatility. The range of codec complexity tradeoffs and bit rate is so wide that one cannot grasp the interdependency of parameters for voice applications in a few pages.

Design of a specific codec must be tailored to the digital channel bandwidth, the analog bandwidth, the quality of signal transmission required and the cost objectives. To illustrate the choices available, the data in Figure 22 compares the signal-to-noise ratios and dynamic range of various codec design options at 32K bits. Generally, the relative merits of each design feature will remain intact in any application. Lowering the bit rate will reduce the dynamic range and noise performance of all techniques. As the bit rate is increased, the overall performance of each technique will improve and the need for more complex designs diminishes.

Non-voice applications of the MC3517 and MC3518 are also possible. In those cases, the signal bandwidth and amplitude characteristics must be defined before the specification of codec parameters can begin. However, in general, the design can proceed along the lines of the voice applications shown here, taking into account the different signal bandwidth requirements.

FIGURE 22 – COMPARATIVE CODEC PERFORMANCE – SIGNAL-TO-NOISE RATIO FOR 1 kHz TEST TONE



These curves demonstrate the improved performance obtained with several codec designs of varying complexity.

- Curve a – Complex companding and double integration (Figure 18 – MC3418)
- Curve b – Double integration (Figure 21 using Figure 6 – MC3418)
- Curve c – Single integration (Figure 21 – MC3418) with 6 mV step size
- Curve d – Single integration (Figure 21 – MC3417) with 25 mV step size

3

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA}\,(Typ)}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst-case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA}(Typ)$ = Typical Thermal Resistance Junction to Ambient

MOTOROLA

MC3419-1L
MC3419A-1L
MC3419C-1L

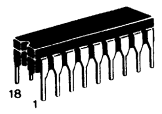
SUBSCRIBER LOOP INTERFACE CIRCUIT (SLIC)

BIPOLAR LASER-TRIMMED INTEGRATED CIRCUIT

TELEPHONE LINE-FEED CIRCUIT

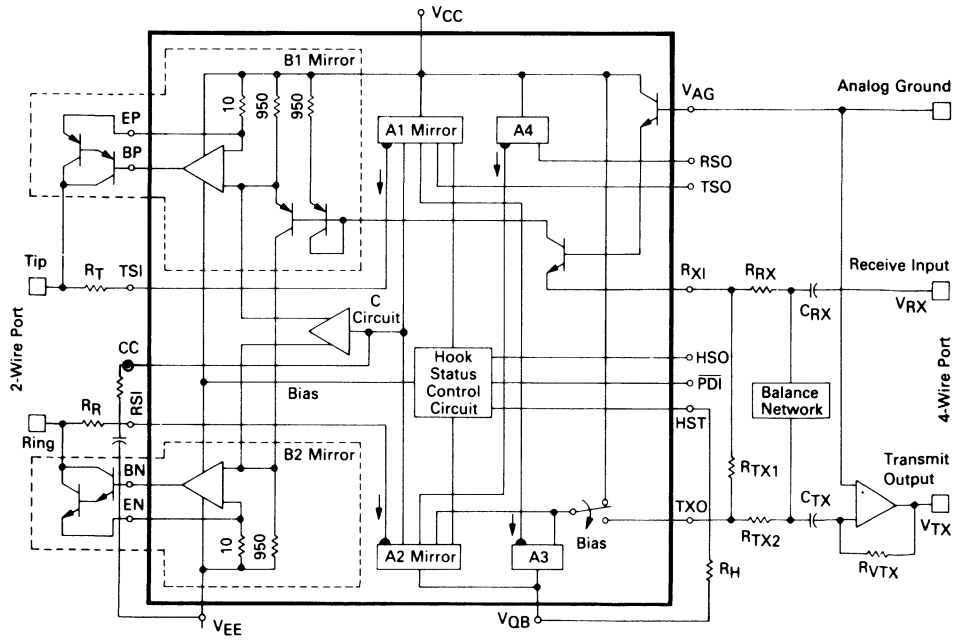
. . . designed as the heart of a circuit to provide BORSHT functions for telephone service in Central Office, PABX, and Subscriber Carrier equipment. This circuit provides dc power for the telephone (Battery), Overvoltage protection, Supervision features such as hook status and dial pulsing, two-wire differential to four-wire single-ended conversions and suppression of longitudinal signals at the two-wire input (Hybrid), and facilitates ringing insertion, Ring trip detection and Testing.

- Totally Upward Compatible with the MC3419
- All Key Parameters Externally Programmable
- Current Sensing Outputs Monitor Status of Both Tip and Ring Leads for Auxiliary Functions such as: Ground Key, Ring Trip, Message Waiting Lamp, etc.
- On-Hook Power Below 5.0 mW
- Digital Hook Status Output
- Powerdown Input
- Ground Fault Protection
- Operates from Single −20 V to −56 V Power Source
- Size and Weight Reduction Over Conventional Approaches
- The sale of this product is licensed under Patent No. 4,004,109. All royalties related to this patent are included in the unit price.



L SUFFIX
CERAMIC PACKAGE
CASE 726

FUNCTIONAL BLOCK DIAGRAM



DS9605

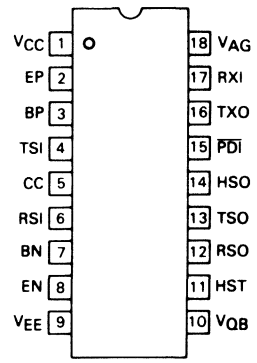
MAXIMUM RATINGS (Voltages Referenced to V_{CC}.)

Rating	Symbol	Value	Unit
Voltage	V_{EE} V_{QB}	−60 V_{EE} − 1.0 V	Vdc
Powerdown Input Voltage Range	$V_{\overline{PDI}}$	+15 to −15	Vdc
Sense Current Steady State Pulse — Figure 4	I_{TSI}, I_{RSI}	 100 200	mAdc
Storage Temperature Range	T_{stg}	−65 to +150	°C
Operating Junction Temperature (θ_{JA} = 100°C/W Typ)	T_J	150	°C

OPERATING CONDITIONS (Voltages Referenced to V_{CC}.)

Rating	Symbol	Value	Unit
Operating Ambient Temperature Range	T_A	0 to +70	°C
Loop Current	I_L	10 to 120	mA
Voltage	V_{EE} V_{QB}	−20 to −56 −20 to V_{EE}	Vdc
Analog Ground (I_L = 0 to 60 mA) (I_L = 0 to 120 mA)	V_{AG}	 0 to −12 −2.5 to −12	Vdc
Supervisory Output Voltage Compliance Range	V_{RSO}, V_{TSO}	−2.0 to −20	Vdc
Hook Status Output	V_{HSO}	+15 to −20	Vdc
Loop Resistance	R_L	0 to 2500	Ω

PIN CONNECTIONS



TRANSMISSION CHARACTERISTICS (R_L = 600 Ω unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Transmit and Receive Gain Variation (Insertion Loss) (1.0 kHz @ 0 dBm Input)	1	V_{TX}/V_L, V_L/V_{RX}				dB
MC3419-1			−0.3	0	+0.3	
MC3419A-1			−0.15	0	+0.15	
MC3419C-1			−0.4	0	+0.4	
Transhybrid Rejection (Input — 1 kHz @ 0 dBm) Fixed (1%) Resistor Balance Network	1	V_{TX}/V_{RX}				dB
MC3419-1, MC3419C-1			−23	−35	—	
MC3419A-1			−33	−40	—	
Trimmed Balance Network All Types			—	−55	—	
Level Linearity (−48 to +3.0 dBm, referenced to 0 dBm @ 1 kHz)	1					dB
Transmission		V_{TX}/V_L	−0.1	0	+0.1	
Reception		V_L/V_{RX}	−0.1	0	+0.1	
Frequency Response (200–3400 Hz referenced to 1.0 kHz @ 0 dBm)	1					dB
Transmission		V_{TX}/V_L	−0.1	0	+0.1	
Reception		V_L/V_{RX}	−0.1	0	+0.1	
Total Distortion @ 1.0 kHz, 0 dBm (C-Message Filtered)	1	V_L/V_{RX} V_{TX}/V_L	— —	−60 −60	— —	dB

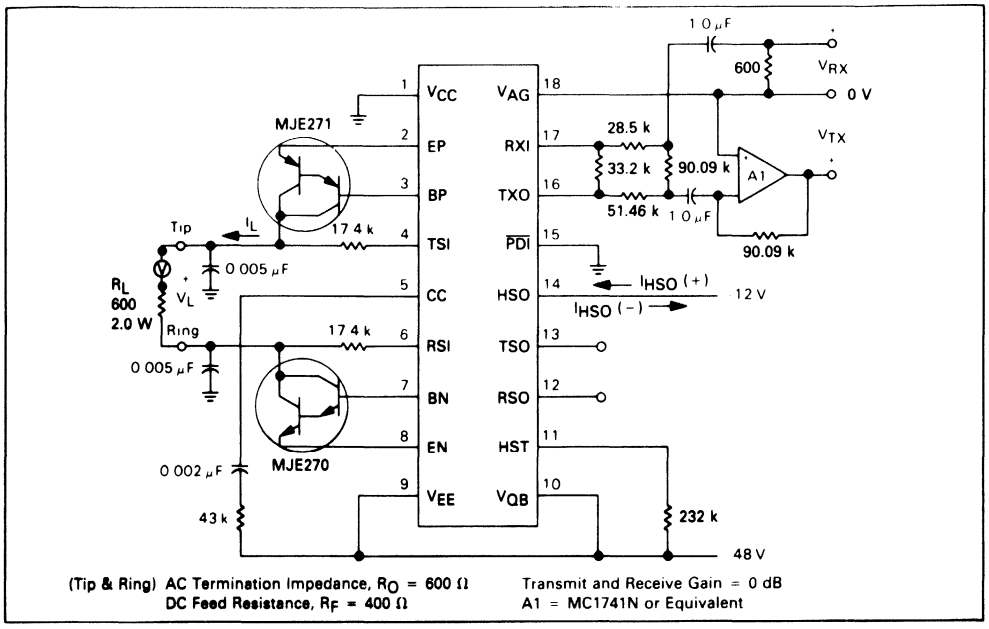
TRANSMISSION CHARACTERISTICS (continued) (R_L = 600 Ω unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Idle Channel Noise (V_{RX} = 0 V) MC3419-1, MC3419A-1 MC3419C-1	1	V_{TX}, V_L	 — —	 3.0 4.0	 10 13	dBrnC
Return Loss (referenced to 600 ohms) @ 1.0 kHz, 0 dBm MC3419A-1 MC3419-1, MC3419C-1	1	$20 \text{ Log } \left\lvert \frac{R_0 - 600}{R_0 + 600} \right\rvert$	 36 30	 — —	 — —	 dB dB
Longitudinal Induction (60 Hz) (I_{LON} = 35 mA RMS)	2	V_{TX}	--	5.0	—	dBrnC
Longitudinal Balance MC3419-1 (200–3000 Hz) MC3419A-1 (200–1000 Hz) MC3419A-1 (3000 Hz) MC3419C-1 (200–3000 Hz)	2	V_{TX}/V_{LON}, V_L/V_{LON}	 -45 -50 -48 -40	 — — — —	 — — — —	dB

ELECTRICAL CHARACTERISTICS (V_{EE} = -48 V, V_{QB} = V_{EE}, V_{AG} = 0 V, R_L = 600 Ω, T_A = 25°C unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Propagation Delay	1	T_P, V_{RX} to V_L V_{RX} to I_{TX}	— —	750 1.2	— —	ns μs
Supply Current — On-Hook (V_{EE} = V_{QB} = 56 V, R_L > 100 MΩ) MC3419-1, MC3419A-1 MC3419C-1	3	I_{VCC}	 — —	 40 100	 200 500	μA
On-Hook Power Dissipation (R_L > 100 MΩ) MC3419-1, MC3419A-1 MC3419C-1	3	P_D	 — —	 1.0 2.5	 — —	mW
Power Supply Noise Rejection (1.0 kHz @ 1.0 V_{RMS}) MC3419-1, MC3419A-1 MC3419C-1	3	V_{TX}/V_{ee}	 -40 -30	 — —	 — —	dB
Quiet Battery Noise Rejection (1.0 kHz @ 1.0 V_{RMS})	3	V_{TX}/V_{qb}	--	-6.0	—	dB
Sense Current Tip Ring	4	 I_{TSO}/I_{TSI} I_{RSO}/I_{RSI}	 0.15 0.15	 0.17 0.17	 0.19 0.19	mA/mA
Fault Currents Tip to V_{CC} Ring to V_{CC} Tip to Ring Tip and Ring to V_{CC}	1	 I_{Tip} I_{Ring} I_{Loop} I_{Tip} and I_{Ring}	 — — — —	 0 2.5 120 2.5	 — — — —	mA
Analog Ground Current	1	I_{VAG}	—	0.1	2.0	μA
Powerdown Logic Levels		$I_{\overline{PDI}}$ V_{IH} V_{IL}	— -1.2 —	-1.0 — —	-10 — -4.0	μA Vdc Vdc
Hook Status Output Current (R_L < 2.5 kΩ, V_{HSO} = +0.4 Vdc) V_{HSO} = -0.4 Vdc) (R_L > 10 kΩ, V_{HSO} = +12 Vdc) V_{HSO} = -12 Vdc)	1	I_{HSO}	 +1.0 -0.4 — —	 +3.0 -1.5 0 0	 — — +50 -2.0	 mA mA μA μA

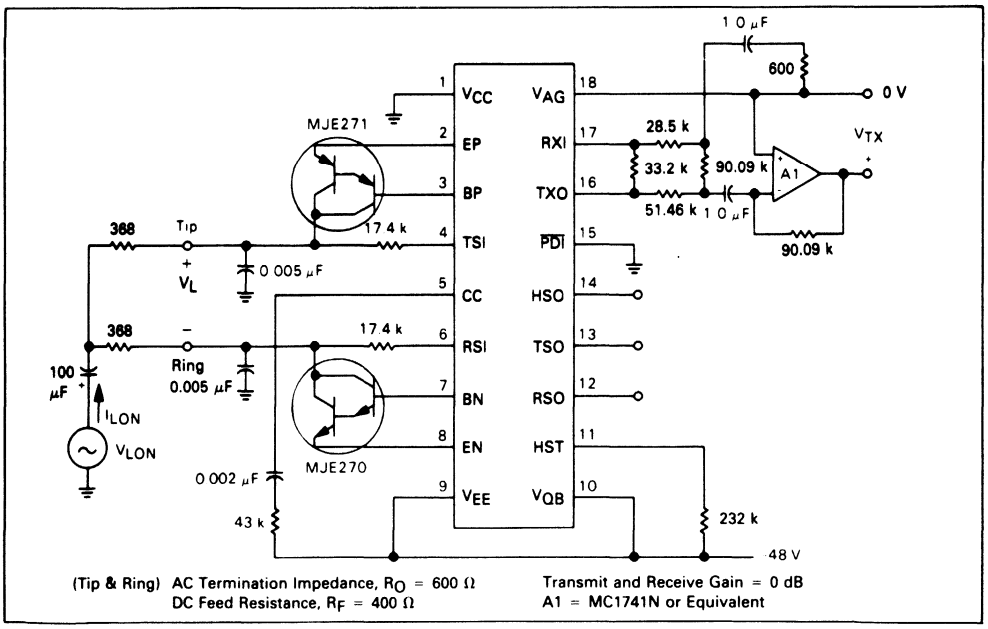
FIGURE 1 — AC TEST CIRCUIT



(Tip & Ring) AC Termination Impedance, R_O = 600 Ω
DC Feed Resistance, R_F = 400 Ω

Transmit and Receive Gain = 0 dB
A1 = MC1741N or Equivalent

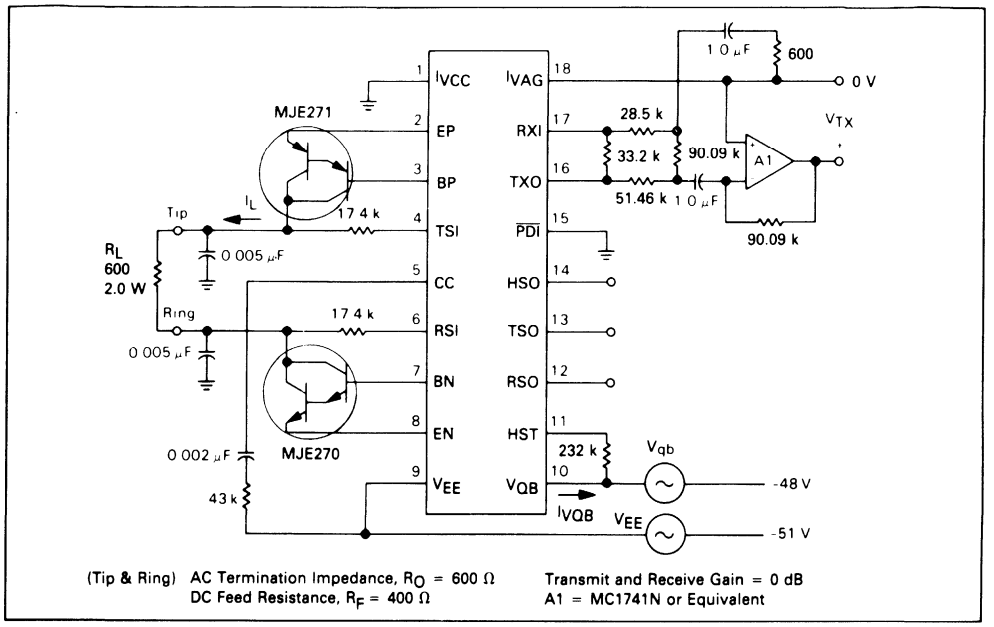
FIGURE 2 — LONGITUDINAL BALANCE TEST CIRCUIT



(Tip & Ring) AC Termination Impedance, R_O = 600 Ω
DC Feed Resistance, R_F = 400 Ω

Transmit and Receive Gain = 0 dB
A1 = MC1741N or Equivalent

FIGURE 3 — SUPPLY NOISE REJECTION TEST CIRCUIT



(Tip & Ring) AC Termination Impedance, R_O = 600 Ω
DC Feed Resistance, R_F = 400 Ω

Transmit and Receive Gain = 0 dB
A1 = MC1741N or Equivalent

FIGURE 4 — TSO AND RSO SUPERVISORY OUTPUT TEST CIRCUIT

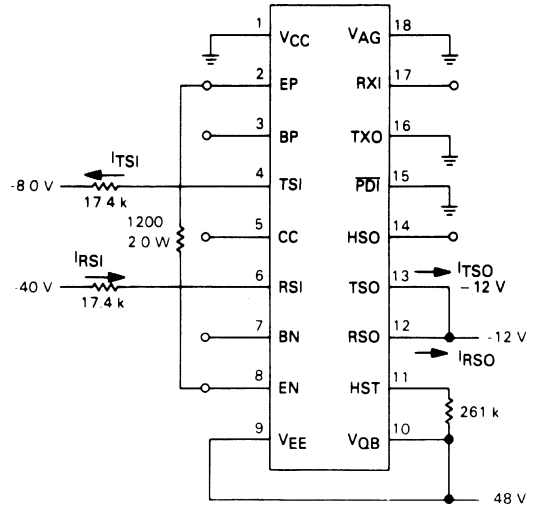


FIGURE 5 — QUIET BATTERY CURRENT I_{VQB} versus LOOP CURRENT I_L

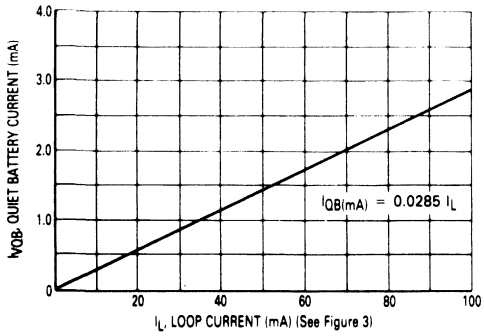
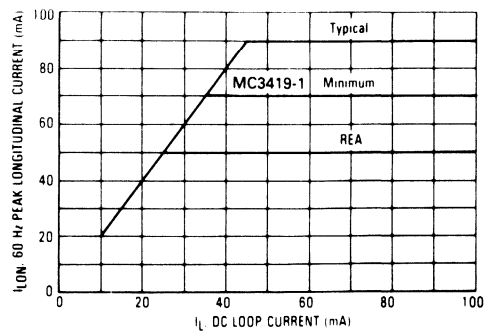


FIGURE 6 — LONGITUDINAL CAPACITY



3

PIN DESCRIPTIONS

Pin	Name	Function
1	V_{CC}	The positive supply voltage. This point is ground in typical applications.
2, 8	EP & EN	Loop current sensing inputs. These are connected to the emitters of the PNP and NPN Darlington transistors. They are tied through 10 Ω resistors to V_{CC} and V_{EE}, respectively. The maximum continuous current through these inputs is 240 mA.
3, 7	BP & BN	Base drive outputs. These pins drive the bases of the PNP and NPN transistors and are able to sink or source, respectively, up to 5.0 mA.
4, 6	TSI & RSI	Tip and Ring voltage Sensing Inputs. They are low impedance inputs (approximately 600 Ω each i.e., 400 Ω + 3 diodes) that translate the voltages on Tip and Ring to a current through resistors R_T and R_R. TSI is referenced to V_{CC} and RSI is referenced to V_{QB}. These pins have 6.0 V zener diodes (to their respective reference) for protection against overvoltage line surges.
5	CC	Compensation Capacitor pin. This pin is used to stabilize the longitudinal or common mode circuitry.
9	V_{EE}	Negative supply voltage. This pin ties to the chip substrate. Its operating voltage range is −20 V to −56 V. It can withstand −60 V without damage and can sustain a voltage surge to −75 V for less than 4.0 ms without significant degradation of performance. Most of the loop current and bias currents flow through this pin.
10	V_{QB}	Quiet Battery Voltage reference. This is the voltage reference for the RSI pin. Its voltage must not go more negative than V_{EE}. The current through this pin, while powered up, is proportional to the loop current, allowing it to be used for loop current limiting. The voltage on this pin, less 4 volts, is the "effective battery feed voltage for the 2-wire lines even though most of the power comes from the V_{EE} supply.
11	HST	Hook Status Threshold programming resistor input. R_H determines the value of loop resistance at which on-hook and off-hook status is switched.
12	RSO	Ring Sense current Output. This output reflects the voltage status of the Ring terminal for voltages more positive than V_{QB}. The current is sourced from this output, it is one-sixth I_{RSI}, its voltage range is 0 to −20 V and its saturation voltage is approximately −2.0 V.
13	TSO	Tip Sense current Output. This output reflects the voltage status of the Tip terminal for voltages more negative than V_{CC}. The current is sourced from this output, it is one-sixth I_{TSI}, its voltage range is 0 V to −20 V and its saturation voltage is approximately −2.0 V.
14	HSO/$\overline{\text{HSO}}$	Hook Status Output. This is a digital output that reflects the condition of the loop resistance. If loop resistance is less than a predetermined value established by R_H, usually R_L < 2.5 kΩ, the HSO pin will be active, i.e., with positive voltage logic (a resistor tied from a +5.0 V or +12 V supply to HSO), this pin will sink current to V_{CC} ($V_{HSO} \cong 0$ V); with negative voltage logic (a resistor tied from a −12 V supply to HSO), this pin will source current from V_{CC} ($V_{HSO} \cong 0$ V). If loop resistance is greater than a predetermined value again established by the same resistor R_H, usually R_L > 10 kΩ, the HSO pin is inactive, i.e., V_{HSO} = logic supply voltage.
15	$\overline{\text{PDI}}$	Powerdown Input pin. This pin is used to deny service to the subscriber. A logic level "0" (V_{IL} < −4.0 V) powers down tne MC3419-1 except for HSO, TSO and RSO. The voltage range of this high impedance input pin is ±15 V.
16	TXO	Transmit current Output. This output sinks current to V_{QB} and is proportional to I_{TSI} + I_{RSI} by a ratio of K1 where: K1 = 1.02. Its saturation voltage is V_{QB} + 2.5 V typ. (+3.5 V over the temperature range). This pin is only active during the off-hook power-up condition.
17	RXI	Receive Input. This input sums ac currents from TXO and the receive voltage input (V_{RX}) and sources all the dc current to TXO. It has a low input impedance (15 Ω) typically biased 4.5 V below the V_{AG} pin voltage during off-hook power-up conditions. During powerdown conditions, the voltages on RXI and TXO can drift up to V_{AG}.
18	V_{AG}	Analog Ground Voltage reference input. The input impedance of this pin is much greater than 1.0 MΩ. It should be ac coupled to system ground and could be direct coupled if system ground is between 0 V and −12 V. AC coupling requires 300 kΩ to V_{CC} and 0.1 μF to system ground. If V_{CC} and system ground are common, tie V_{AG} directly to V_{CC}. If dc loop currents are allowed to go higher than 60 mA, V_{AG} should be biased from −2.5 V to −12 V to avoid problems at high ambient temperatures.

FUNCTIONAL DESCRIPTION

Referring to the functional block diagram on page 1, line sensing resistors (R_R and R_T) at the TSI and RSI pins convert voltages at the Tip and Ring terminals into currents which are fed into current mirrors* A1 and A2. An output of A1 is mirrored by A3 and summed together with an output of A2 at the TXO terminal. Thus, a differential to single-ended conversion is performed from the ac line signals to the TXO output.

All the dc current at the TXO output is fed back through the RXI terminals to the B1 mirror input. The inputs to B1 and B2 are made equal by mirroring the B1 input current to the B2 input through a unity gain output of the B1 mirror. Both B1 and B2 mirrors have high gain outputs (x95) which drive the subscriber lines with balanced currents that are equal in amplitude and 180° out of phase. The feedback from the TXO output, through the B-Circuit mirrors, to the subscriber line produces a dc feed resistance significantly less, but proportional to the loop sensing resistors.

In most line-interface systems, the ac termination impedance is desired to be greater than the dc feed impedance. A differential ac generator on the subscriber loop would be terminated by the dc feed impedance if the total ac current at the TXO output were returned to the B1 input along with the dc current. Instead, the MC3419-1 system diverts part of the ac current from the B-Circuit mirrors. This decreases the ac feedback current, causing the ac termination impedance at the line interface to be greater than the dc feed impedance.

The ac current that is diverted from the B1 mirror input is coupled to a current-to-voltage converter circuit that has a low input impedance. This circuit consists of an op amp (external to the MC3419-1) and a feedback resistor which produces the transmit output voltage (V_{TX}) at the 4-wire interface. Transmission gain is programmed by the op amp feedback resistor (R_{VTX}).

Reception gain is realized by converting the ac coupled receive input voltage (V_{RX}) to a current through an external resistor (R_{RX}) at the low impedance RXI terminal. This current is summed at RXI with the dc and ac feedback current from the A-Circuit mirrors and drives the B1 mirror input. The B-Circuit mirror outputs drive the 2-wire port with balanced ac current proportional to the receive input voltage. Reception gain is programmed by the R_{RX} resistor.

Since receive input signals are transmitted through the MC3419-1 to the 2-wire port, and the 2-wire port signals are returned to the 4-wire transmit output, a means of cancellation must be provided to maintain 4-wire signal separation (transhybrid rejection). Cancellation is complicated because the gain from the receive port to the transmit port depends on the impedance of the subscriber loop. A passive "balance network" is used to achieve transhybrid rejection by cancelling, at the low impedance input to the transmit op amp, the current reflected by the loop impedance to the 4-wire transmit output. For a resistive loop impedance, a single resistor provides the cancellation. For reactive loops, the balance network should be reactive.

Longitudinal (common-mode) currents that may be present on the subscriber lines are suppressed in the MC3419-1 by two methods. The first is inherent in the mirror configuration. Positive-going longitudinal currents into Tip and Ring create common-mode voltages that cause a decreasing current through the Tip Sensing resistor and an increasing current through the Ring Sensing resistor. When these equal and opposite signal currents are reflected through the A-Circuit mirrors and summed together at TXO, the total current at TXO remains unchanged. Therefore, the ac currents due to the common-mode signal are cancelled before reaching the transmit output.

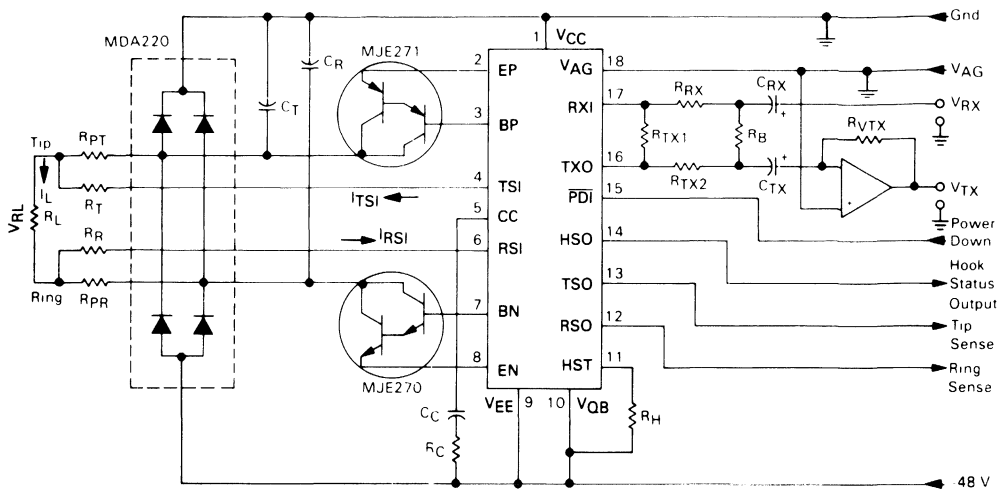
The second longitudinal suppression method is more dominant, since it limits the amplitude of common-mode voltages that appear at the Tip and Ring terminals.

A common-mode suppression circuit detects common-mode inputs and drives the loop with balanced currents to reduce the input amplitude. Subtracting currents from outputs of the A1 and A2 mirrors produces a signal current at the CC terminal in response to the common-mode voltage at Tip and Ring. A transconductance amplifier (C-Circuit) generates a current proportional to the CC terminal voltage which is summed with the current from the RXI terminal at the inputs of current mirrors B1 and B2. The weighting and polarity of the summing networks produce common-mode B1 and B2 mirror output currents at the 2-wire port. The common-mode input impedance is inversely proportional to the gain of the longitudinal suppression circuit. R_C and C_C compensate the common-mode feedback loop. At 60 Hz with typical component values, the 2-wire common-mode impedance is less than 5 Ω.

The longitudinal suppression circuit output currents are generated by modulating dc current fed to the loop by the B1 and B2 current mirrors. This configuration avoids the increased power dissipation attributed to current mode loop drive because dc and longitudinal currents are not cumulatively sourced to the loop. However, driving common-mode currents through the B-circuit current mirrors in this manner limits the longitudinal suppression capability. The suppression circuit is unable to reverse 2-wire current polarities to maintain a low-impedance termination when longitudinal currents exceed the dc loop current. At low dc loop currents, the common-mode signal capability, known as longitudinal capacity, is limited by the loop current (Figure 6). At high-loop currents, longitudinal capacity is limited by the maximum voltage swing of the CC terminal and is therefore independent of dc loop current.

*A current mirror is a circuit which behaves as a current controlled current source. It has a single low-impedance input terminal with respect to a reference point and one or more high impedance outputs.

FIGURE 7 — BASIC SLIC CIRCUIT



The hook status control circuit supplies the bias currents to activate the B-Circuit op amps and other sections of the MC3419-1. To activate the bias currents, the control circuit compares the current through the sense resistors, R_R and R_T, and the load resistance R_L with the current through the hook status threshold programming resistor, R_H, by using outputs from both A1 and A2 mirrors. The A1 mirror output sources current to the R_H resistor. (This reduces all internal currents to near zero during the on-hook state in order to eliminate unnecessary power consumption.) If this current is large enough the voltage on the HST pin will trip an internal comparator, then another circuit compares the current from the A1 output with that of an A2 output. These currents must match within ±15%. If so, HSO will be activated and the bias circuits will turn on provided the voltage on $\overline{PDI}$ is greater than −1.2 V. The HSO pin can have either a pull-up resistor or a pull-down resistor and when activated it will switch to V_{CC} (0 volts).

Once the MC3419-1 is powered up, a circuit with a gain of 20 feeds current to the R_H resistor in order to keep the bias circuitry active. (The sense resistors are paralleled with the Darlington transistors which reduces the sense input currents.) Should the sense input currents drop below one-twentieth of the required power-up current, the bias currents will be removed, forcing a power-down condition.

Current mode analog signal processing is critically dependent on voltage to current conversion at the 2-wire and 4-wire inputs. Precise, low-noise voltage sensing through resistors R_T, R_R and R_{RX} requires quiet, low impedance terminations at terminals TSI, RSI and RXI respectively. For 2-wire signals, terminal V_{QB} isolates the loop-sensing resistors and current mirrors from noise at the high-current V_{EE} terminal. External filtering from V_{CC} to V_{QB} ("quiet battery" terminal) ensures loop voltages are sensed without interference from system supply noise. V_{EE} noise rejection at audio frequencies is typically 60 dB or greater.

Receive input terminal RXI is referenced to the V_{AG} terminal which references the 4-wire input to the "analog ground" of the 4-wire signal source, thus isolating the input from power ground voltage transients. This isolation offers 70 dB of noise rejection at audio frequencies.

SYSTEM EQUATIONS

K1 — The current gain from $I_{TSI} + I_{RSI}$ to TXO only during an off-hook power-up condition. K1 = 1.02 ± 1%.

K2 — The current gain from RXI to the collectors of the off-chip Darlington transistors only during an off-hook power-up condition. K2 = 95 ± 1%.

For simplicity, the following equations do not use K1 or K2. Instead the actual numerical value is used, for instance (1 + K1K2) = 1 + 1.02 x 95 = 97.9 is approximately 98.

R_L — Loop resistance. This is a load resistance from Tip to Ring and can be either ac or dc depending on context.

LOOP CURRENT REGULATIONS

FIGURE 8(a)

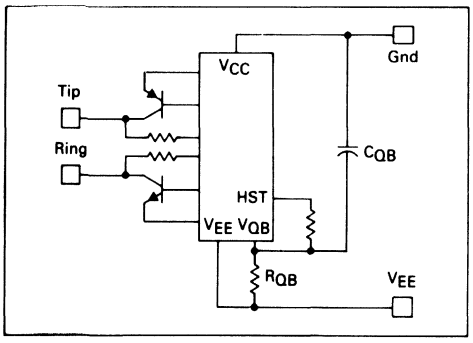


FIGURE 9(a)

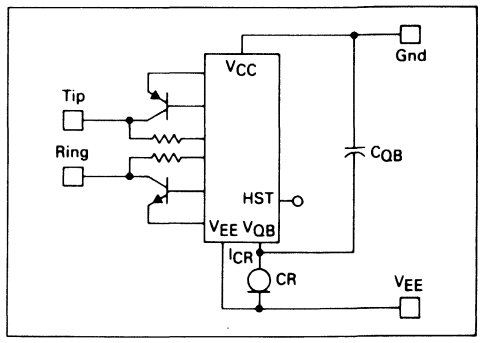


FIGURE 8(b)

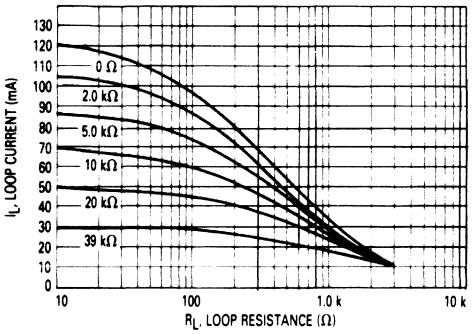
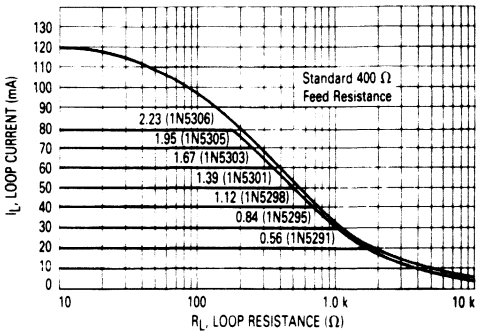


FIGURE 9(b)



SYSTEM EQUATIONS (continued)

Z_L — Loop impedance. This is used only to connote a complex impedance loading on Tip and Ring.

I_L — Loop current. The dc current flow through R_L.

R_F — Dc feed resistance. The synthesized resistance from which battery (V_{CC} and V_{EE}) current is fed to R_L. The battery feed resistance is balanced differential feed. See Figure 7. (This assumes $V_{QB} = V_{EE}$.) The first order equation is:

$$R_F = \frac{R_R + R_T + 1200\ \Omega}{98} \quad (1)$$

Because of the diode voltage drops on TSI and RSI, the actual dc feed resistance is higher. The second order equation is:

$$R_F = \frac{|V_{QB}|(98\ R_L + R_R + R_T + 1200\ \Omega)}{98\ (|V_{QB}| - 4.0\ V)} - R_L \quad (2)$$

ignoring the effects of R_L

$$R_F = \frac{|V_{QB}|(R_R + R_T + 1200\ \Omega)}{98\ (|V_{QB}| - 4.0\ V)} \quad (3)$$

So:

$$R_R = R_T = \frac{49R_F\ (|V_{QB}| - 4.0\ V)}{|V_{QB}|} - 600 \quad (4)$$

The minimum value for R_R and R_T is 5.0 kΩ.

The first order value of R_F can not be greater than the desired value of the termination impedance (usually 600 Ω or 900 Ω). To achieve dc feed resistances that are greater, a resistor can be placed between V_{QB} and V_{EE} along with a filter capacitor C_{QB} which restores the desired termination impedance and filters power supply noise. A diode should also be placed between V_{QB} and V_{EE} to prevent damage in case a catastrophic power supply failure occurs.

I_{VQB} — This is the current that is sourced from the V_{QB} pin and is proportional to the currents into and out of RSI and TSI. When the SLIC is in the off-hook power-up mode, I_{VQB} is also proportional to I_L.

$$I_{VQB} = 2.15\,I_{RSI} + 0.7\,I_{TSI} \quad (5)$$

$$I_{VQB} = 0.029\,I_L \quad (6)$$

R_{FQ} — Dc feed resistance. The synthesized resistance from which battery current is fed to R_L, see Figure 8. (This assumes V_{QB} is tied to V_{EE} through a resistor R_{QB}.) R_{QB} synthesizes additional dc feed resistance to the R_F value previously stated.

When using R_{QB}, the dc feed is effectively balance fed from V_{CC} and V_{QB} instead of V_{EE}. The sense resistors (R_R and R_T) should be selected to make R_F (first order) less than the termination impedance.

$$R_{FQ} = \frac{|V_{EE}|(98R_L + R_R + R_T + 1200 + 2.85R_{QB})}{98(|V_{EE}| - 4.0\ V)} - R_L \quad (7)$$

Ignoring R_L, this simplifies to:

$$R_{FQ} = \frac{|V_{EE}|(R_R + R_T + 1200 + 2.85R_{QB})}{98(|V_{EE}| - 4.0\ V)} \quad (8)$$

Therefore:

$$R_{QB} = \frac{98R_{FQ}(|V_{EE}| - 4.0\ V) - |V_{EE}|(R_R + R_T + 1200\ \Omega)}{2.85|V_{EE}|} \quad (9)$$

C_{QB} — Power supply noise filter capacitor.

$$C_{QB} = \frac{2.85\,R_{QB} + R_R + R_T + 1200\ \Omega}{2\pi f\,R_{QB}\,(R_R + R_T + 1200\ \Omega)} \quad (10)$$

Figure 9B shows R_{QB} replaced with a current regulating device such as Motorola's 1N5283 family.

I_{CRQB} — The current that is sourced to a current regulating device from the V_{QB} pin. When this current reaches the regulated value, the voltage differential between V_{EE} and V_{QB} increases causing the effective battery voltage to decrease which limits I_L to a maximum value as determined below:

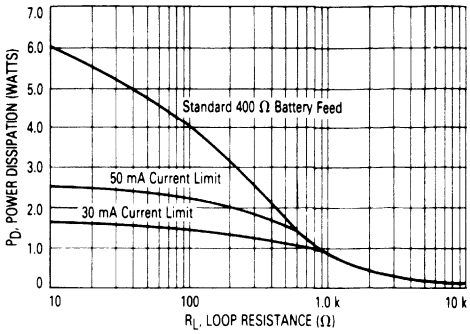
$$I_L = 34.5\,I_{CRQB} \quad (11)$$

The graph, Figure 9B, shows loop current versus loop resistance using several values of I_{CRQB}. The closest current regulating diode part number to that value is also shown. A typical value for C_{QB} in this case is 10 μF, 60 Vdc.

Figure 10 shows how power can be conserved on the shorter loop lengths by utilizing current limiting techniques.

Overvoltage protection on the 2-wire port is achieved with the MDA220 diode bridge and the protection resistors R_{PR} and R_{PT}. Whenever the voltage on the 2-wire port exceeds the power supply rails (V_{CC} and V_{EE}), the MDA220 diodes will forward bias and "clamp" to the rail voltage. The current is limited by the protection resistors. These resistors should be as large in value as possible. However, if they are too large, they will interfere with the performance of the SLIC under worst case conditions.

FIGURE 10 — TOTAL SLIC POWER DISSIPATION versus LOOP RESISTANCE



$$R_{PT} < R_T/196 - 15 \quad (12)$$

Using the voltage of V_{QB} when I_L is at its minimum off-hook value (Typ. 20 mA):

$$R_{PR} < R_R/196 + 25|V_{EE} - V_{QB}| - 15 \quad (13)$$

The tolerance of these resistors is not critical due to placement inside a closed loop. Positive temperature co-efficient resistors (PTC) may be considered here. Consult resistor manufacturers for component selections that will meet the surge current and peak voltage requirements.

Because the MC3419-1 is a broadband device it requires compensation components to keep its circuits stable.

C_R & C_T — Compensates the longitudinal gain of the A and the B circuit mirrors. Their values range from 2000 pF to 5000 pF.

R_C & C_C — Compensates the longitudinal "C" circuitry. Their values can be ratioed according to:

$$R_C \times C_C = R_T \times C_T. \quad (14)$$

Two off-chip power Darlington transistors are used with the MC3419-1. These transistors reduce any temperature gradiant problems with the precision matched devices on-chip and they alleviate thermal stress conditions that could occur for every on-hook and off-hook transition. The power dissipation in these devices is:

$$P_{QT} = I_L^2(R_T/98 - R_{PT} - 4) + (2.0\ V)I_L \quad (15)$$

$$P_{QR} = I_L\,[|V_{EE}| - 2 - I_L(R_T/98 + R_L + R_{PR} + 16)] \quad (16)$$

where $I_L = |V_{EE}|/R_{FQ}$ or I_L(max) in current limited designs.

SYSTEM EQUATIONS (continued)

R_H — The resistor that determines the hook status threshold values of R_L. R_H is selected from a graph of the following two equations:

Off-hook threshold

$$R_H = 6(R_L + R_R + R_T) \quad (17)$$

On-hook threshold

$$R_H = 27.25\,[R_L + 0.01(R_R + R_T)] \quad (18)$$

FIGURE 11 — HOOK STATUS DETECTION

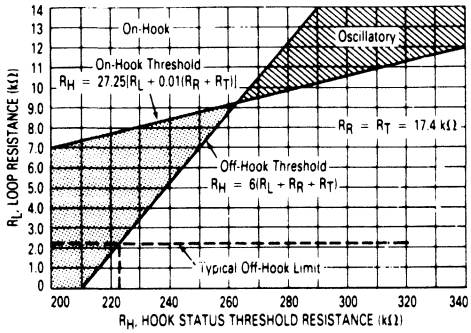


Figure 11 shows such a graph using 17.4 kΩ as the values for R_R and R_T. Note the oscillatory condition to the right of the crossing point. Selection of R_H in this region is usually not a problem since the majority of telephone lines do not fall into this resistance range. R_H always ties to V_{QB} and HST and will give reliable hook status information regardless of power supply voltages and $\overline{PDI}$.

R_O — Termination impedance of the 2-wire port. This impedance is greater than the dc feed resistance R_F because of a current splitting network in the feedback loop, R_{TX1} and R_{TX2}.

K3 — A constant, formed by R_{TX1} and R_{TX2}, between 0 and 1, which determines the ratio of the first order value of R_F to R_O.

$$R_O = \frac{R_R + R_T + 1200\ \Omega}{1 + 97K3} \quad (19)$$

So:

$$K3 = \frac{R_R + R_T + 1200\ \Omega - R_O}{97R_O} \quad (20)$$

and

$$K3 = \frac{R_{TX2} + Z_{in}}{R_{TX1} + R_{TX2} + Z_{in}} \quad (21)$$

Z_{in} — The input impedance of the current to voltage converter op amp. This impedance is usually negligible, it can be used to sway the selection of a 1% component value.

$$Z_{in} = \frac{(R_R + R_T + 1200\ \Omega)\,G_{TX}}{1020\,(1 - K3)} = \frac{R_{VTX}}{1000} \quad (22)$$

R_{TX1} — Feeds most of the TXO dc current to the RXI pin. To keep TXO from saturation the maximum value of R_{TX1} is as follows:

$$R_{TX1} < \frac{(R_R + R_T + 1200\ \Omega)\,(|V_{QB}|min - |V_{AG}|max - 6.5\ V)}{|V_{QB}|min - 5.4\ V} \quad (23)$$

Where:

$$|V_{QB}|min = \frac{(R_R + R_T + 1200\ \Omega)\,(|V_{EE}|min - 4)}{(R_R + R_T + 1200\ \Omega + 2.8\,R_{QB})} \quad (24)$$

or if a current regulator diode is used:

$$R_{TX1} < \frac{0.01\ I_L(max)\,(R_R + R_T + 600\ \Omega) - |V_{AG}|max - 3.9\ V}{0.01\ I_L(max)} \quad (25)$$

It is beneficial to make R_{TX1} as large as possible. Typical values range from 15 k to 24 kΩ.

$$R_{TX2} = \frac{K3\,R_{TX1}}{1 - K3} - Z_{in} \quad (26)$$

$$C_{TX} = \frac{R_R + R_T + 1200\ \Omega}{7R_{TX2}} \quad \text{The result is in } \mu F. \quad (27)$$

G_{TX} — The voltage gain from the 2-wire port to V_{TX} which is adjustable by R_{VTX}.

$$G_{TX} = \frac{1.02\,(1 - K3)\,R_{VTX}}{R_R + R_T + 1200\ \Omega} \quad (28)$$

$$R_{VTX} = \frac{G_{TX}(R_R + R_T + 1200\ \Omega)}{1.02\,(1 - K3)} \quad (29)$$

G_{RX} — The voltage gain from the V_{RX} input to the 2-wire port which is adjustable by R_{RX}.

$$G_{RX} = \frac{-95\,R_L\,(R_R + R_T + 1200\ \Omega)}{R_{RX}\,[(R_R + R_T + 1200\ \Omega) + R_L(1 + 97K3)]} \quad (30)$$

$$G_{RX} = \frac{-95\,R_L\,R_O}{R_{RX}(R_L + R_O)} \quad (31)$$

$$R_{RX} = \frac{95\,R_L\,R_O}{G_{RX}(R_L + R_O)} \quad (32)$$

$$C_{RX} > \frac{R_{RX} + R_B}{2\pi\,f\,R_{RX}R_B} \quad (33)$$

Where f is the minimum passband frequency, usually 200 Hz.

Transhybrid Rejection — The voltage gain from V_{RX} to V_{TX}. It is expressed in dB, the number should be negative and the larger the value the better. Transhybrid rejection is achieved by summing a current from the V_{RX} input (R_B) with the TXO current that flows to the current to voltage converter. R_B balances a resistive load, R_L.

$$R_B = \frac{R_{RX}(1 + 97K3)\,(R_O + R_L)}{97R_L\,(1 - K3)} \quad (34)$$

FIGURE 12 — BALANCE NETWORK FOR CAPACITIVE LINES

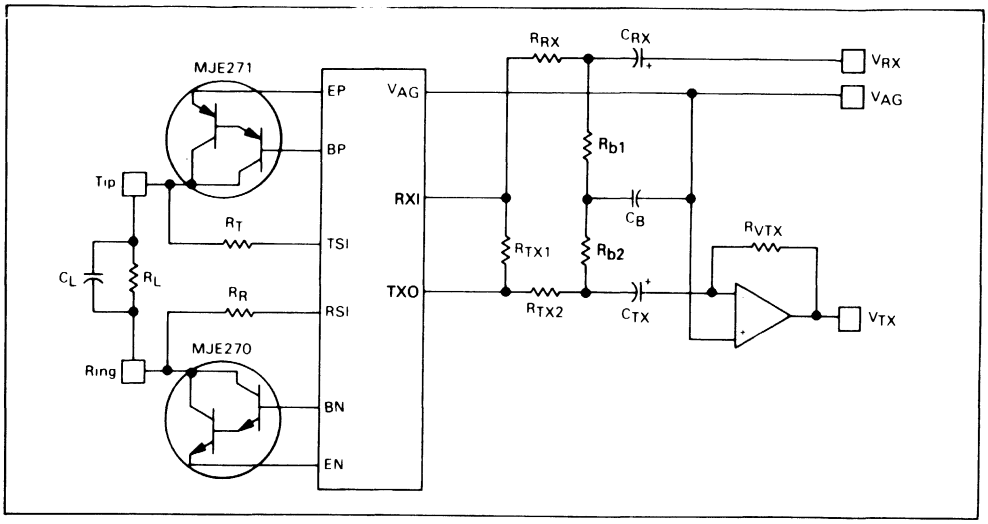
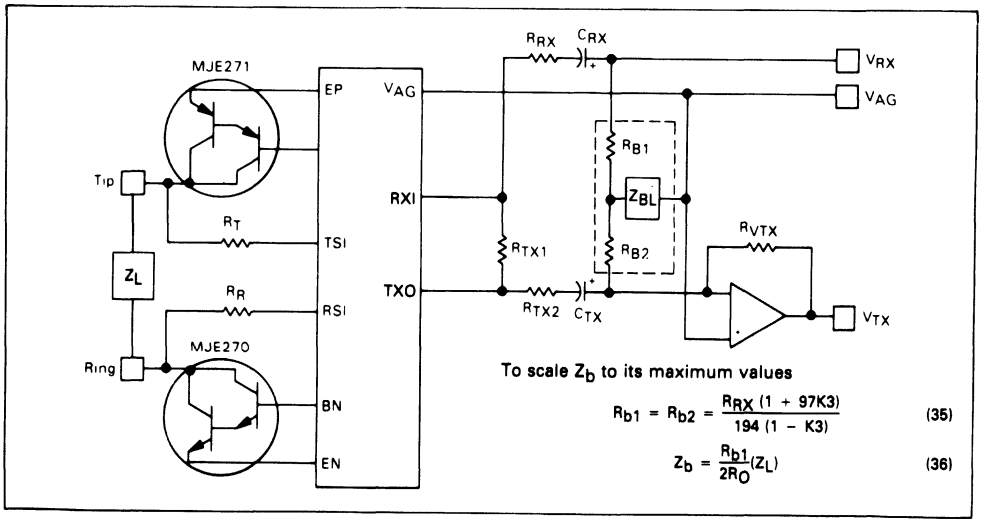


FIGURE 13 — BALANCE NETWORK FOR COMPLEX LOAD IMPEDANCES



To scale Z_b to its maximum values

$$R_{b1} = R_{b2} = \frac{R_{RX}(1 + 97K3)}{194(1 - K3)} \quad (35)$$

$$Z_b = \frac{R_{b1}}{2R_O}(Z_L) \quad (36)$$

When the 2-wire port has a parallel R and C load, then (see Figure 12):

$$R_{b1} = \frac{R_{RX}(R_R + R_T + 1200\ \Omega)}{97R_L(1 - K3)} \quad (37)$$

$$R_{b2} = \frac{R_{RX}(R_R + R_T + 1200\ \Omega)}{97R_O(1 - K3)} \quad (38)$$

$$C_b = \frac{R_L C_L}{R_{b2}} \quad (39)$$

When it is desirable to balance complex load impedances using component values that are equal to the load values (see Figure 13) then:

$$R_{b1} = \frac{R_{RX}(1 + 97K3)}{194(1 - K3)} + \sqrt{\left[\frac{R_{RX}(1 + 97K3)}{194(1 - K3)}\right]^2 - \frac{R_O R_{RX}(1 + 97K3)}{97(1 - K3)}} \quad (40)$$

$$R_{b2} = \frac{R_{RX}(1 + 97K3)}{97(1 - K3)} - R_{b1} \quad (41)$$

$$Z_b = Z_L \quad (42)$$

R_{b1} and R_{b2} values are interchangeable.

SYSTEM EQUATIONS (continued)

The Tip and Ring Sense Output currents are proportional to the currents out of and into TSI and RSI, respectively.

$$I_{TSO} = \frac{I_{TSI}}{6} \quad (43)$$

$$I_{RSO} = \frac{I_{RSI}}{6} \quad (44)$$

$$I_{TSO} = \frac{|V_{Tip} - V_{CC}| - 2.0\ V}{6\ (R_T + 600\ \Omega)} \text{ for } V_{Tip} < V_{CC} \quad (45)$$

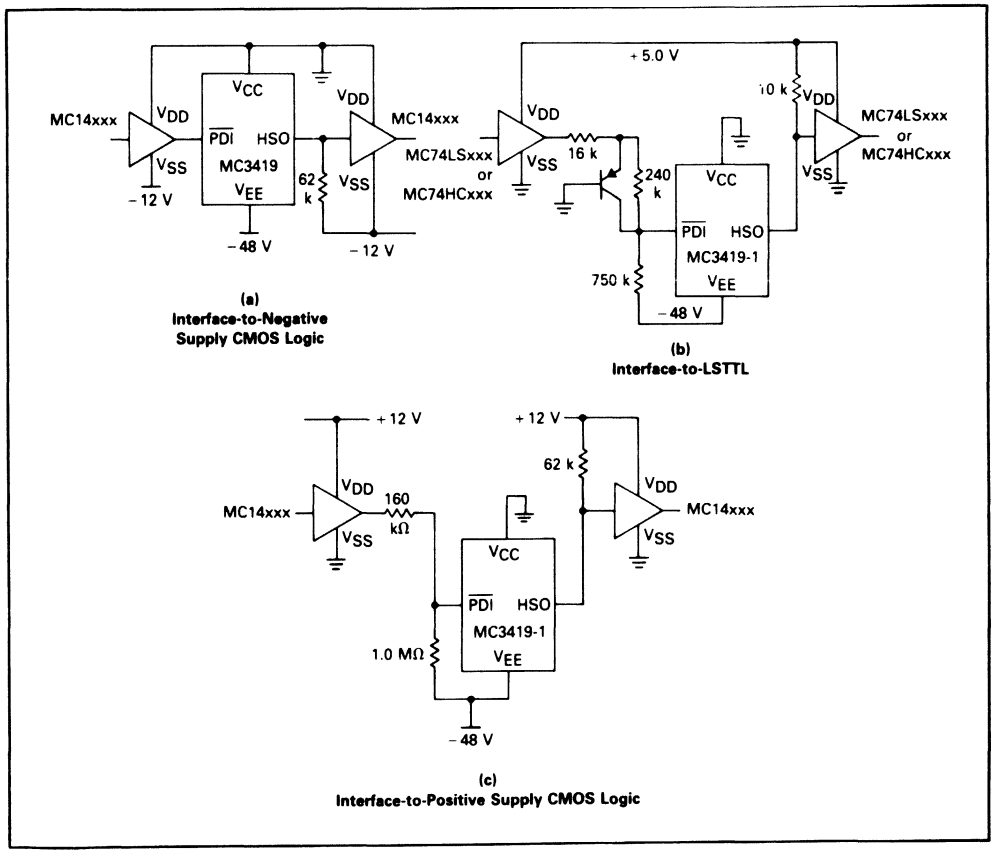
$$I_{RSO} = \frac{|V_{Ring} - V_{QB}| - 2.0\ V}{6(R_R + 600\ \Omega)} \text{ for } V_{Ring} > V_{QB} \quad (46)$$

Digital interfacing to the MC3419-1 $\overline{PDI}$ pin and the HSO pin is shown in Figures 14a, 14b and 14c. If the $\overline{PDI}$ pin is not used it should be terminated to V_{CC} and if HSO is not used, it can be left open.

Figure 15 is an application circuit showing solid state ringing insertion using an MOC3030 zero-crossing detector optocoupled triac to replace the conventional electromechanical relay. This device inserts the ringing signal on a zero voltage crossing which eliminates noise in adjacent cable pairs and removes the signal on a zero current crossing which eliminates inductive voltage spikes that commonly destroy relay contacts. The ringing generator provides a continuous 40 V to 120 V RMS signal from 15 to 66 Hz superimposed upon −48 Vdc. Ringing cadencing is inserted with the Ring Enable Input. The 2N6558 and MPSA42 replace the MJE270 for systems that use ringing generator voltages greater than 70 V_{RMS}. The MDA220 diode bridge is replaced with a series 1N4007 on the Tip lead and a shunting 1N4004 to V_{EE} and to allow ringing voltage

3

FIGURE 14 — INTERFACE-TO-DIGITAL LOGIC



3

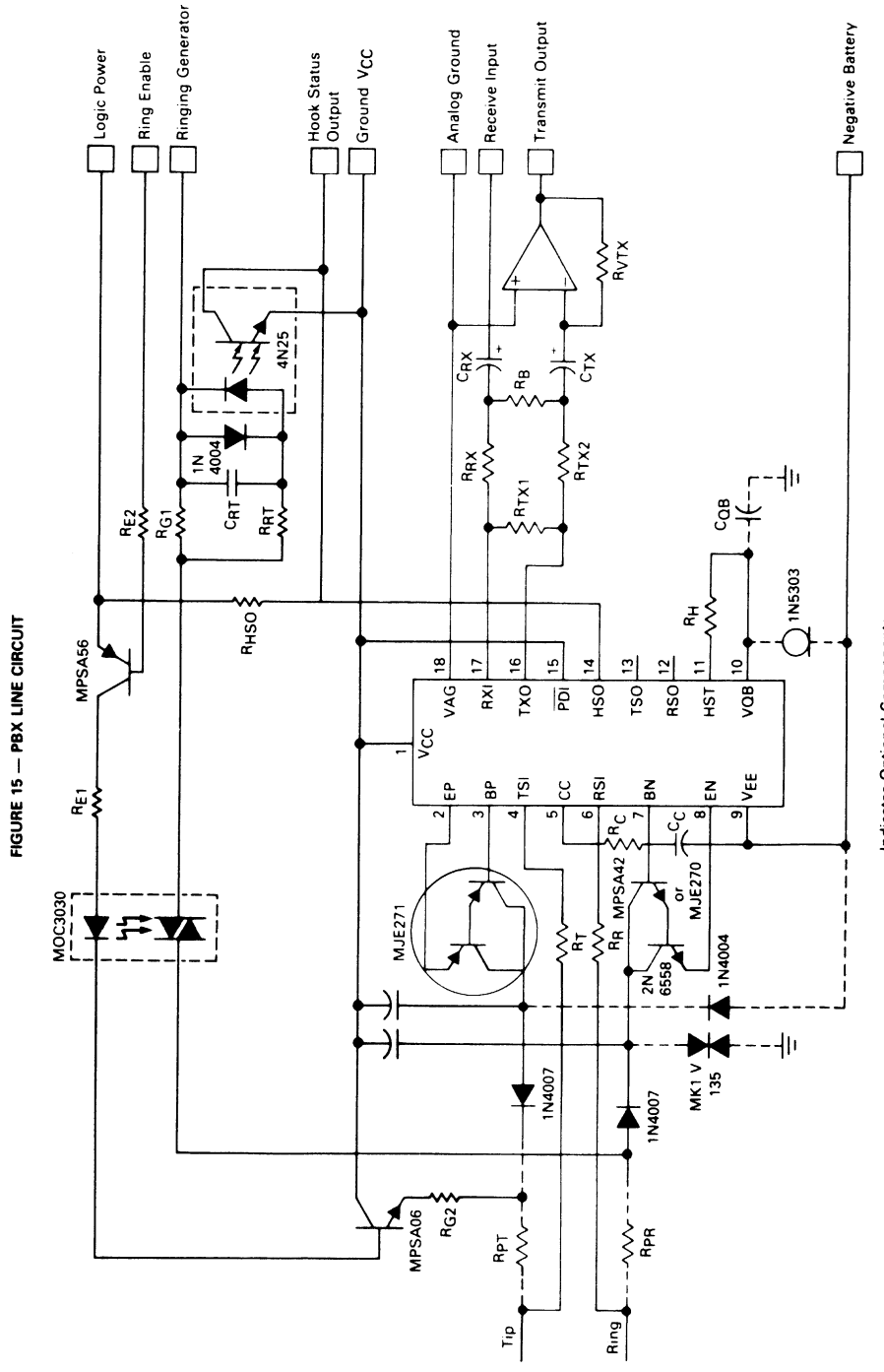


FIGURE 15 — PBX LINE CIRCUIT

SYSTEM EQUATIONS (continued)

on the Ring lead to exceed the power supply voltages, a 1N4007 and an MK1V-135 (Sidac) are used for protection. The forward voltage drop across the 1N4007, during normal operation, will not affect the parametric characteristics of the MC3419-1 since it is "inside" a feedback circuit. If the MJE270 is used, the MK1V-135 should be replaced with a lower voltage Sidac or MoSorb transient suppressor.

An optocoupled transistor circuit is used for ring trip detection on long lines. It samples only the ac and dc ringing signal current and uses a simple one pole filter to eliminate the low level ac signal. Under worst case conditions this circuit will ring trip in 1½ to 4 cycles. In systems serving only short loops (<700 Ω), if R_{G1} and R_{G2} are 620 Ω or greater, the optotransistor circuit is not needed, the Hook Status Output will perform ring trip on a Zero Crossing. The Ring Enable input and the Hook Status Output interface with standard CMOS and TTL logic.

The op amp in this circuit is an integral part of the following codecs, filters or combos:

MC3417/8 — MC145414
MC14404/6/7 — MC14413/4
MC14401/2/3/5

For further applications information such as:

— 24 volt PBX circuit
— 2-wire differential to 2-wire unbalanced SLIC
— Constant current battery feed
— Per line ringing cadencing circuit
— Message waiting lamp
— Transfer button detection
— etc.

Please contact your local Motorola sales office.

3

LONG LINES OFF-PREMISE LINES

Specifications

R_F	— 200 Ω	R_O	— 600 Ω	Off-Hook	— <2500 Ω
I_L(max)	— 60 mA	R_X Gain	— 0 dB 200–3400 Hz	On-Hook	— >10 kΩ
R_L(max)	— 1900 Ω	T_X Gain	— 0 dB 200–3400 Hz	Protection	— 1000 V
				Ringer Equivalent	— 5

V_{Logic}	—	+5.0 V
V_{EE}	—	−42 to −56 Volts
$V_{Ringing}$	—	(40 V to 120 V_{RMS}) + V_{EE}

Parts List

MPSA56	R_R	—	9.09 k	1%	Matched
2N3905	R_T	—	9.09 k	1%	if desired
2N6558	R_{PT}	—	47 Ω	5%	
MPSA42	R_{PR}	—	75 Ω	5%	
MJE271	R_{G1}	—	620 Ω	5%	
1N4007	R_{G2}	—	100 Ω	5%	
MK1V135	R_{E1}	—	91 Ω	5%	
1N4007	R_{E2}	—	3.0 k	5%	
1N4007	R_{RT}	—	20 k	5%	
1N5303	R_C	—	24 k	5%	
1N4004	R_H	—	127 k	1–3%	
MC3419-1	R_{HSO}	—	10 k	5%	

MOC3030	R_{TX1}	—	12.1 k	1%	
4N25	R_{TS2}	—	5.76 k	1%	
	R_{RX}	—	28.7 k	1%	
	R_B	—	28.0 k	1%	
	R_{VTX}	—	28.6 k	1%	
	C_T		0.004 μF		
	C_R	—	0.004 μF		
	C_C	—	0.001 μF		
	C_{RX}	—	1.0 μF/20 V		
	C_{TX}	—	2.0 μF/40 V		
	C_{RT}	—	20 μF/5.0 V		
	C_{QB}	—	10 μF/60 V		

SHORT LINES ON-PREMISE LINES

Specifications

R_F	—	500 Ω	R_X Gain	—	−5.0 dB
R_L(max)	—	700 Ω	T_X Gain	—	0 dB
Ring Trip	—	<50 ms	V_{Logic}	—	+5.0 Volts
Ringer Equivalent	—	2.5	V_{EE}	—	−20 to −56 Volts
R_O	—	600 Ω	$V_{Ringing}$	—	(40 V to 70 V_{RMS}) + V_{EE}

Parts List

MJE271	R_R	—	19.6 k	1%	
MJE270	R_T	—	19.6 k	1%	
MPSA56	R_{G1}	—	620 Ω	5%	
2N3905	R_{G2}	—	620 Ω	5%	
1N4007	R_{E1}	—	91 Ω	5%	
1N4007	R_{E2}	—	3.0 k	5%	
MC3419C-1	R_H	—	330 k	5%	

MOC3030	R_{HSO}	—	10 k	5%	
	R_{TX1}	—	19.6 k	1%	
C_T — 0.004 μF	R_{TX2}	—	42.2 k	1%	
C_R — 0.004 μF	R_{RX}	—	69.8 k	1%	
C_C — 0.004 μF	R_B	—	301 k	1%	
C_{RX} — 0.1 μF	R_{VTX}	—	127 k	1%	
C_{TX} — 0.5 μF	R_C	—	56 k	5%	

MOTOROLA

MC6172
(Formerly MC6862)

2400 bps DIGITAL MODULATOR

The MC6172 is a MOS subsystem designed to be integrated into a wide range of equipment utilizing serial data communication.

The modulator provides the necessary modulation and control functions to implement a serial data communication link over a voice grade channel, utilizing differential phase shift keying (DKSP) at bit rates of 1200 or 2400 bps. Phase options are provided for both the U.S. and international markets. The MC6172 can be implemented into a wide range of data handling systems, including stand-alone modems, data storage devices, remote data commuication terminals, and I/O interfaces for counters.

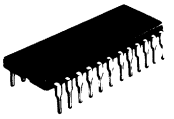
N-channel silicon-gate technology permits the MC6172 to operate using a single voltage supply and be fully TTL compatible.

The modulator is compatible with the MC6173 demodulator to provide medium-speed data communications capability.

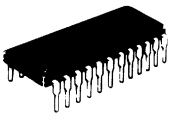
- Clear-to-Send Delay Options
- 511-Bit CCITT Test Pattern
- Terminal Interfaces are TTL Compatible
- Compatible Functions for 201B/C Data Sets
- CCITT and U.S. Phase Options
- 1200/2400 bps Operation
- Answer-Back Tone
- The MC6173 Is the Companion Demodulator
- Application Note Available – AN-870

MOS
(N-CHANNEL, SILICON-GATE)

2400 bps MODULATOR

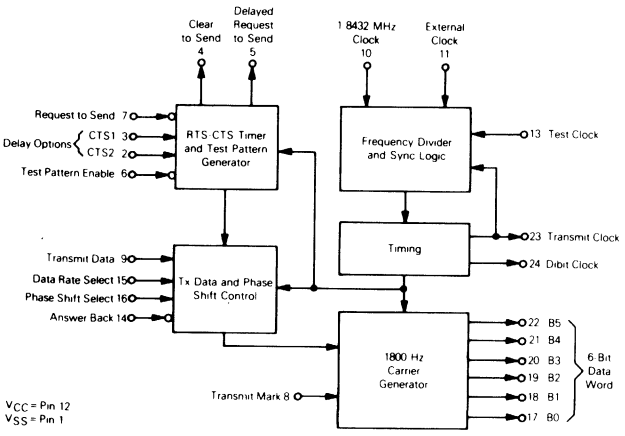


L SUFFIX
CERDIP PACKAGE
CASE 623

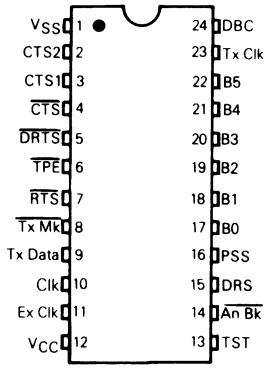


P SUFFIX
PLASTIC PACKAGE
CASE 709

BLOCK DIAGRAM



PIN ASSIGNMENT



DS9842R1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_A	T_L to T_H 0 to 70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance Plastic Package Cerdip Package	θ_{JA}	 120 65	°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}).

POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

Where:

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{PORT}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts − Chip Internal Power

P_{PORT} = Port Power Dissipation, Watts − User Determined

For most applications $P_{PORT} \ll P_{INT}$ and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P_D and T_J (if P_{PORT} is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

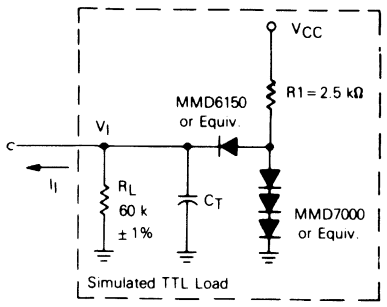
DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0 ±0.25 Vdc, V_{SS} = 0, $T_A = T_L$ to T_H, all outputs loaded as shown in Figure 1 unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage	V_{IH}	V_{SS} + 2.0	–	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}	–	V_{SS} + 0.8	V
Input Current ($V_{in} = V_{SS}$) CTS1, CTS2, PSS, DRS, $\overline{An\ Bk}$, and $\overline{Tx\ MK}$ / $\overline{RTS}$ and $\overline{TPE}$	I_{in}	– –	– –	−0.2 −1.6	mA
Input Leakage Current (V_{in} = 5.25 V, $V_{CC} = V_{SS}$)	I_{IL}	–	–	2.5	μA
Output High Voltage (I_{OH} = −0.04 mA, Load A) (I_{OH} = 0.0 mA, Load B)	 V_{OH1} V_{OH2}	 V_{SS} + 2.4 V_{CC} − 0.5 V	 – –	 V_{CC} V_{CC}	V
Output Low Voltage (I_{OL} = 1.6 mA, Load A)	V_{OL}	V_{SS}	–	V_{SS} + 0.4	V
Input Capacitance (f = 0.1 MHz, T_A = 25°C)	C_{in}	–	5.0	–	pF
Internal Power Dissipation (Measured at $T_A = T_L$) (All inputs at V_{SS} except Pin 13 = 57.6 kHz and ALL outputs open)	P_{int}	–	210	315	mW
Input Transition Times, All Inputs Except 1.8432 MHz Input (From 10% to 90% points)	t_r, t_f	–	–	1.0*	μs
Input Transition Times, 1.8432 MHz Input (From 0.8 V to 2.0 V)	t_r, t_f	–	–	40	ns
Input Clock Duty Cycle, 1.8432 MHz Input (Measured at 1.5 V level)	D.C.	30	–	70	%
Tx Data Setup Time (Figure 2)	t_{su}	35	–	–	μs
Tx Data Hold Time (Figure 2)	t_h	35	–	–	μs
Output Transition Times	t_r, t_f	–	–	5.0	μs

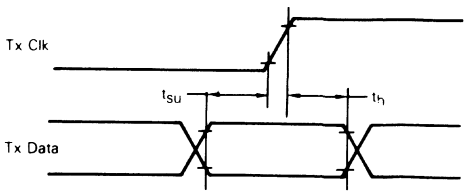
*Maximum Input Transition Times are ≤0.1 × Pulse Width or the specified maximum of 1.0 μs, whichever is smaller.

FIGURE 1 – OUTPUT TEST LOAD



C_T = 20 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

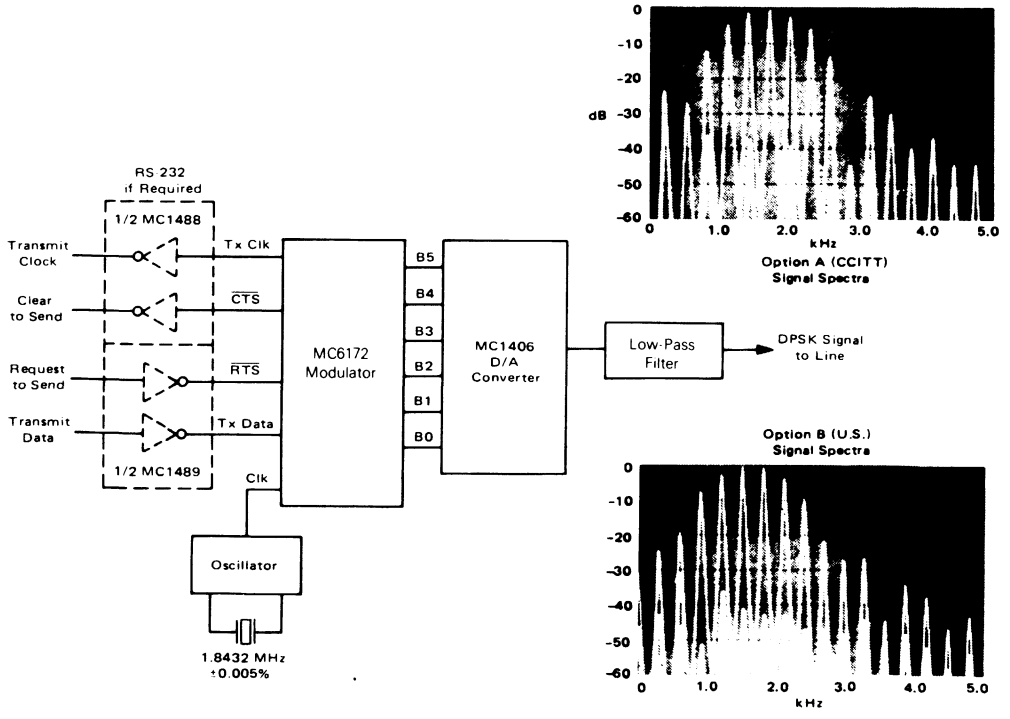
FIGURE 2 – TRANSMIT DATA SETUP AND HOLD TIME



Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

3

FIGURE 3 – 2400 bps MODULATOR INTERFACE

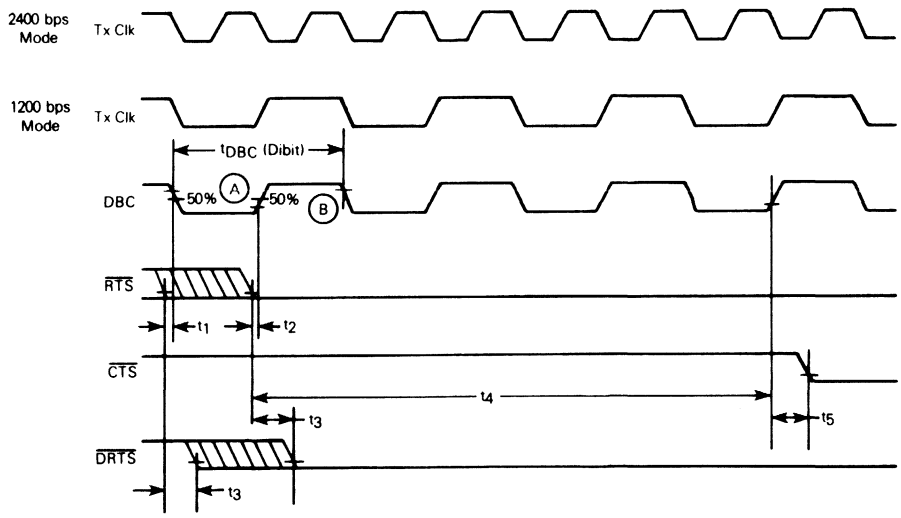


DELAY TIMINGS (See Figures 4 and 5)

Characteristic	Symbol	Min	Typ	Max	Unit
$\overline{RTS}$ to DBC Delay	t_1	–	–	8	μs
DBC to $\overline{RTS}$ Delay	t_2	45	–	–	μs
$\overline{RTS}$-$\overline{DRTS}$ Delay	t_3	–	–	35	μs
$\overline{RTS}$-$\overline{CTS}$ Delay					
CTS1 = 0, CTS2 = 1	t_4*	0	–	35	μs
CTS1 = 1, CTS2 = 0		8.55	–	9.35	ms
CTS1 = 1, CTS2 = 1		24.9	–	26.4	ms
CTS1 = 0, CTS2 = 0		147.0	–	154.0	ms
$\overline{CTS}$-DBC Delay					
CTS1 = 1, CTS2 = 0	t_5	–	–	35	μs
CTS1 = 1, CTS2 = 1		–	–	35	
CTS1 = 0, CTS2 = 0		–	–	35	
$\overline{RTS}$ to $\overline{CTS}$ Low	t_6	–	–	1.60	ms
$\overline{RTS}$ Min Delay	t_7	–	–	1.67	ms
DBC to $\overline{DRTS}$ Delay	t_8	–	–	35	μs
DBC Cycle Time	t_{DBC}	833.28	833.33	833.37	μs

*The reference frequency tolerance is not included.

FIGURE 4 – $\overline{RTS}$-$\overline{CTS}$ AND $\overline{RTS}$-$\overline{DRTS}$ DELAYS



$\overline{RTS}$-$\overline{CTS}$ delay options are selected by the CTS1 and CTS2 inputs, and are stated as time delay interval t_4. An $\overline{RTS}$ input signal synchronized about point A will synchronize $\overline{CTS}$ with the positive transition of DBC (Dibit Clock). Delay t_4 is measured with respect to the negative transition of $\overline{RTS}$.

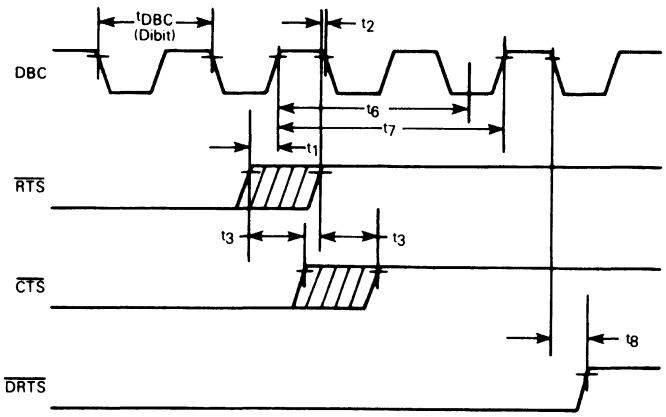
$\overline{RTS}$ signals synchronized with the positive transition of DBC (point B), will result in the same $\overline{CTS}$ delay (t_4). For this case the negative transition of $\overline{CTS}$ is synchronized with the negative transition of DBC with delay t_4 measured with respect to the negative transition of $\overline{RTS}$.

$\overline{DRTS}$ will go low within t_3 of the negative transition of $\overline{RTS}$. With the exception of the no-delay option, $\overline{CTS}$ will go low within t_5 of the positive transition of DBC, following the t_4 delay selected. This applies when $\overline{RTS}$ is synchronized to Point A as shown.

If $\overline{RTS}$ goes high and remains high ≥ 20 μs within time interval t_4, a reset of the internal $\overline{RTS}$-$\overline{CTS}$ timer function will occur. If $\overline{RTS}$ goes high for less than 20 μs, the circuit may or may not respond to this momentary loss of the $\overline{RTS}$ signal.

Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

FIGURE 5 – LOSS OF $\overline{RTS}$ TO $\overline{DRTS}$ DELAY



A positive transition of $\overline{RTS}$ after $\overline{CTS}$ has become active can result in different functional characteristics of the $\overline{CTS}$ and $\overline{DRTS}$ output signals, depending on the time duration that $\overline{RTS}$ remains inactive.

Under all conditions, $\overline{CTS}$ will go high within t_3 following a positive transition of $\overline{RTS}$. If $\overline{RTS}$ goes high in the shaded region shown (i.e., synchronized to the positive transition of DBC) and remains high beyond the time interval defined as t_7, then $\overline{DRTS}$ will go high within t_8 of the next negative transition of DBC. If $\overline{RTS}$ were to go low after t_7, the $\overline{RTS}$-$\overline{CTS}$ delay times given in Figure 4 will result.

If $\overline{RTS}$ goes high in the shaded region shown, and then returns low within time interval t_6, the negative transition of $\overline{CTS}$ will follow within 35 μs, and $\overline{DRTS}$ will remain in the active or low state. Under these conditions, the normal $\overline{RTS}$-$\overline{CTS}$ delay times are not encountered when $\overline{RTS}$ is reactivated. If $\overline{RTS}$ goes low for less than 20 μs, the circuit may or may not respond

NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

DEVICE OPERATION

GENERAL

Figure 3 shows the modulator and its intra-connections. The data to be transmitted is presented in synchronous serial format to the modulator for conversion to DPSK signals used in transmission. The modulator output is digital; therefore, a D/A converter and a filter transform the signal to an analog form.

The control functions provide four different Clear-to-Send delay options. An Answer-Back tone is available for automatic answering applications. The modulator has a built-in 511-bit pseudorandom pattern generator for use in system diagnostic tests.

INPUT/OUTPUT FUNCTIONS

Request to Send ($\overline{RTS}$)

The $\overline{RTS}$ signal from the data terminal controls transmission from the modulator. A low level on $\overline{RTS}$ activates the modulator data output. A constant mark, for synchronization, is sent during the $\overline{RTS}$ to $\overline{CTS}$ delay interval. Termination of the transmission is accomplished by taking $\overline{RTS}$ high (see Figures 4 and 5).

Delayed Request to Send ($\overline{DRTS}$)

This output can be used to control transmission as specified by the Transmit Mark control input. $\overline{DRTS}$ follows the negative transition of $\overline{RTS}$, and goes negative within t_3 of the negative transition of $\overline{RTS}$ (Figure 4). The delay from a positive transition of $\overline{RTS}$ to a positive transition of $\overline{DRTS}$ is shown in Figure 5. The $\overline{DRTS}$ delay allows data within the modulator to be transmitted before transmission is inhibited.

Clear to Send ($\overline{CTS}$)

$\overline{CTS}$ follows $\overline{RTS}$ to both the logic 0 and logic 1 levels. The delay from a negative transition of $\overline{RTS}$ to a negative $\overline{CTS}$ transition is selectable by external strapping of CTS1 and CTS2. The delay from a positive transition of $\overline{RTS}$ to a positive $\overline{CTS}$ transition is less than t_4.

$\overline{CTS}$ will go low within t_5 after the positive transition of the Dibit Clock (see Figure 4) except when the non-delay option is selected. For the no-delay option, $\overline{CTS}$ follows $\overline{RTS}$ within t_5.

$\overline{RTS}$-$\overline{CTS}$ Delay Options (CTS1, CTS2)

The $\overline{RTS}$-$\overline{CTS}$ delays are selectable according to the following strapping options

$\overline{RTS}$-$\overline{CTS}$ Delay	CTS1	CTS2
0.0 + 0.035 ms, − 0.0 ms	0	1
8.55 to 9.35 ms	1	0
24.90 to 26.4 ms	1	1
147.0 to 154.0 ms	0	0

Transmit Mark (Tx Mk)

The Transmit Mark control allows the system designer to select whether the Delayed Request to Send activitates and deactivates the transmission on the modulator chip or off the chip in the output amplifier.

When Tx Mk is high, transmission is controlled on the modulator chip, and occurs from the chip only when $\overline{DRTS}$ or Answer Back is in the logic 0 state (see Figure 6).

When Tx Mk is low, transmission is controlled off the modulator chip. In this mode, the modulator chip transmits marks at all times except when data or an Answer-Back tone is being transmitted (see Figure 6).

Test Pattern Enable ($\overline{TPE}$)

A 511-bit test pattern generator is contained on the modulator chip. This pattern is in accord with CCITT specification V52.

The 511-bit test pattern is activated by applying a logic 0 to $\overline{TPE}$. A mark (logic 1) condition on the Transmit Data input with $\overline{TPE}$ activated (logic 0) causes the test pattern to appear at the data output. A space (logic 0) condition on Tx Data with $\overline{TPE}$ activated causes the test pattern data to appear inverted at the data output.

Although the Motorola 2400 bps modulator contains a CCITT 511 test pattern generator it does not incorporate the 511 data randomizer or scrambler.

Random data applied to Tx Data with TPE activated causes the test pattern data to be scrambled (exclusive NORed) with the data, and the result appears at the data output.

The MC6173 demodulator does contain a built-in data descrambler, which is enabled by $\overline{TPE}$ input going active. To scramble data using the modulator, the circuit in Figure 7 must precede the Tx Data input of the modulator. Tx Data is added to the scrambler output pattern. Then the data is delayed by a full data bit before being transmitted by the modem. This assures a proper Transmit Data/Transmit Clock phase relationship.

If the data scrambler is to be an optional feature, then the transmit data multiplexer would also have to be built. This is selected by the Test Pattern Enable signal or any other signal that is found suitable.

The scrambling of data in the data comm environment is not done in an attempt to encrypt information in the normal sense of the word. Rather, the purpose of the scrambling of data is to guarantee that with respect to the modem carrier, there is always random data on the line with little chance for a long string of ones or zeros to exist. This is particularly important if an adaptive equalizer is being incorporated at the demodulator. The adaptive equalizer will require reasonably evenly distributed data to optimize its statistical response to the incoming signal. The normally used code is the CCITT 511 sequence which is exclusive ORed with data.

The test pattern generator can be enabled only when $\overline{CTS}$ and $\overline{RTS}$ are logic 0. If $\overline{TPE}$ is activated outside this time interval, the previously stated $\overline{RTS}$-$\overline{CTS}$ and $\overline{RTS}$-$\overline{DRTS}$ delays, shown in Figures 4 and 5, are not valid.

Data-Rate Select (DRS)

The modulator can transmit at either 2400 bps or 1200 bps. Both data rates utilize an 1800 Hz carrier signal and employ phase shifting at 1200 Hz. The 2400 bps rate is obtained by encoding two bits of data into each phase shift. The 2400 Hz rate is selected by applying a logic 1 to the Data-Rate Select lead. The 1200 Hz rate is selected by applying a logic 0 to DRS.

Phase-Shift Select (PSS)

Option A (CCITT) or Option B (U.S.) phase shift can be selected for 2400 bps operation. The input data format and phase shift relationship for these two options are as follows:

Data	PSS = 0 Option A*	PSS = 1 Option B
00	0°	+45°
01	+90°	+135°
11	+180°	+225°
10	+270°	+315°

*See example Figure 8.

FIGURE 6 — TRANSMIT MARK CONTROL

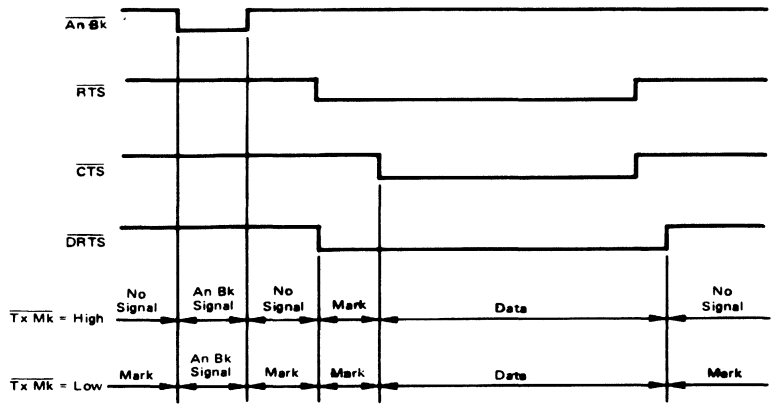


FIGURE 7 – MODULATOR CCITT 511 DATA SCRAMBLER

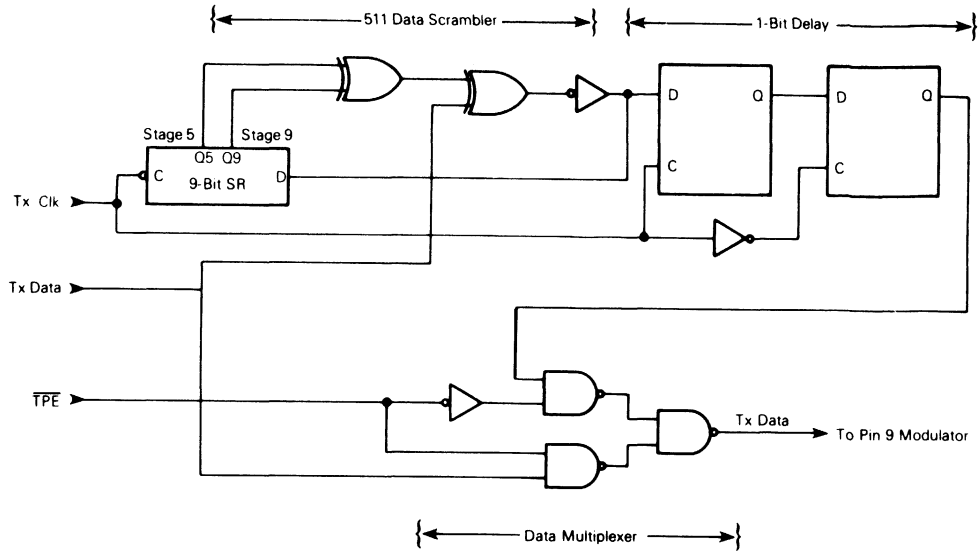
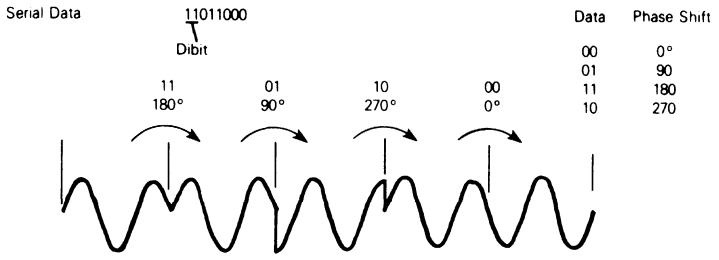


FIGURE 8 – EXAMPLE-CARRIER PHASE SHIFTS FOR OPTION A



For 1200 bps operation, Option C (CCITT) or Option D (U.S.) phase shift can be selected:

Data	PSS = 0 Option C	PSS = 1 Option D
0	+90°	+45°
1	+270°	+225°

Option C is selected by applying a logic 0 to the Phase Shift Select lead when the Data Rate Select lead is strapped for 1200 bps operation (logic 0). Option D is selected by applying a logic 1 to PSS with DRS at logic 0. The phase shifts shown are the difference in phase between the signal at the end of one dibit period and the new signal at the beginning of the next dibit.

Transmit Data (Tx Data)

Transmit Data is the serial binary information presented for DPSK modulation. A high level represents a mark. For timing, see Transmit Clock (Figure 4).

Transmit Clock (Tx Clk)

A 2400/1200 Hz Transmit Clock output is provided for the communication terminal. The Transmit Data signal is sampled on the positive transition of Transmit Clock. The Transmit Data to Transmit Clock setup and hold time requirements are shown in the Electrical Characteristics Table and in Figure 2.

Dibit Clock (DBC)

A 1200 Hz Dibit Clock identifies the modulation timing. This signal goes negative less than 100 μs prior to the start of dibit modulation.

External Clock (Ex Clk)

A 2400/1200 Hz clock signal applied to the External Clock lead causes Transmit Clock to be synchronized with Ex Clk. This input must have an accuracy within ±0.005%.

When no transitions occur on this input, the internal clock provides the 2400/1200 Hz transmit timing signal. Fast synchronization of Tx Clk to Ex Clk is not provided on the chip. *When Ex Clk is not used, it should be tied to either the logic 0 or logic 1 state.*

1.8432 MHz (Clk)

This input must be a square wave with rise and fall times of less than 40 ns and a 50 ±20% duty cycle. The clock accuracy must be written ±0.005%.

Answer Back ($\overline{\text{An Bk}}$)

A logic 0 level applied to Answer Back causes a 2025 Hz carrier to be generated on the modulator chip instead of a phase shifted 1800 Hz carrier. A logic 1 level applied to $\overline{\text{An Bk}}$ enables the modulator to generate the normal phase shifted 1800 Hz carrier signal, as shown in Figure 6. The time delay from a transition on $\overline{\text{An Bk}}$ to the appropriate signal at the modulator chip output is less than 2 ms.

Activation of $\overline{\text{An Bk}}$ (a logic 0) will disable all other operation modes including the $\overline{\text{Tx Mk}}$ function, and will reset $\overline{\text{CTS}}$ to an inactive state along with the $\overline{\text{RTX}}$-$\overline{\text{CTS}}$ internal timer. $\overline{\text{An Bk}}$ should therefore be activated only before initiating $\overline{\text{RTS}}$ or after loss of the $\overline{\text{DRTS}}$ output signal. The combination of a logic 0 on $\overline{\text{An Bk}}$ with a logic 0 on $\overline{\text{TPE}}$ is not used in normal system operation, and hence is used as a reset input during device test.

Digital Output (B0-B5)

These outputs are designed to interface with a 6-bit digital-to-analog converter. The resultant signal out of the D/A is the differential phase shift keyed signal quantized at a 14.4 kHz rate. A low-pass filter can then be used to smooth the data transitions. B0 is the least-significant bit, and the positive level the active state.

Test Clock (TST)

A test signal input is provided to decrease test time of the chip. *In normal operation this input must be strapped low.*

MOTOROLA

MC6173

2400 bps DIGITAL DEMODULATOR

MOS
(N-CHANNEL, SILICON-GATE)

2400 bps DEMODULATOR

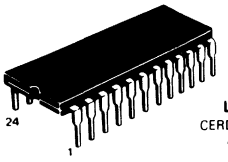
The MC6173 is a MOS subsystem designed to be integrated into a wide range of equipment utilizing serial data communication.

The demodulator provides the necessary demodulation and control functions to implement a serial data communication link over a voice grade channel, utilizing differential phase shift keying (DPSK) at bit rates of 1200 or 2400 bps. Phase options are provided for both the U.S. and international markets. The MC6173 can be implemented into a wide range of data handling systems, including stand-alone modems, data storage devices, remote data communication terminals, and I/O interfaces for counters.

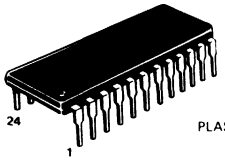
N-channel silicon gate technology permits the MC6173 to operate using a single voltage supply and be fully TTL compatible.

The demodulator is compatible with the M6800 microcomputer family, and provides medium-speed data communications capability.

- Compatible with MC6172 Modulator
- 511-Bit CCITT V.52 Test Pattern
- Terminal Interfaces Are TTL Compatible
- Compatible Functions for 201B/C and V.26 Data Sets
- CCITT and U.S. Phase Options
- 1200/2400 bps Operation

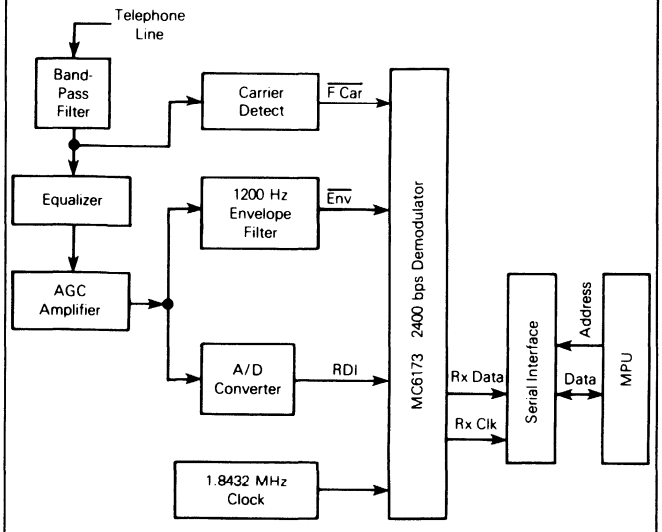


L SUFFIX
CERDIP PACKAGE
CASE 623

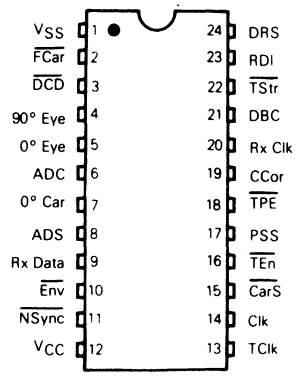


P SUFFIX
PLASTIC PACKAGE
CASE 709

FIGURE 1 – TYPICAL APPLICATIONS



PIN ASSIGNMENT



DS9869R1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Thermal Resistance	θ_{JA}	82.5	°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{SS}).

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 ±0.25 Vdc, V_{SS} = 0, $T_A = T_L$ to T_H all outputs loaded as shown in Figure 3 unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage	V_{IH}	V_{SS} + 2.0	–	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}	–	V_{SS} + 0.8	V
Input Current ($V_{in} = V_{IL}$) Pins 3, 11, 13, 15, 16, 17, 18, 22, 24	I_{IL}	–	–	−0.2	mA
Input Leakage Current (V_{in} = 5.25 Vdc, $V_{CC} = V_{SS}$) Pins 2, 10, 14, 23	I_{in}	–	–	2.5	µA
Output High Voltage (I_{OH} = −0.04 mA, Load A) (I_{OH} = 0.0 mA, Load B)	V_{OH1} V_{OH2}	V_{SS} + 2.4 V_{CC} − 0.5 V	– –	V_{CC} V_{CC}	V
Output Low Voltage (I_{OL} = 1.6 mA, Load A)	V_{OL}	V_{SS}	–	V_{SS} + 0.4	V
Input Capacitance (f = 0.1 MHz, T_A = 25°C)	C_{in}	–	5.0	–	pF
Internal Power Dissipation (measured at $T_A = T_L$) (All Inputs at V_{SS} except Pin 13 = 57.6 kHz and ALL Outputs Open)	P_{Int}	–		630	mW
Input Transition Times, 1.8432 MHz Input (From 0.8 V to 2.0 V)	t_r t_f	– –	– –	40 40	ns
Input Transition Times, All Inputs Except 1.8432 MHz Input (From 10% to 90% Points)	t_r, t_f	–	–	1.0*	µs
Output Transition Times (From 10% to 90% Points)	t_r, t_f	–	–	5.0	µs
Input Clock Duty Cycle, 1.8432 MHz Input (Measured at 1.5 V level)	D.C.	30	–	70	%
Data Setup Time	t_{DS}	770	–	–	ns
Rx Data Setup Time	t_{su}	35	–	–	µs
Data Hold Time	$t_{h(D)}$	0	–	–	ns
Rx Data Hold Time	t_h	35	–	–	µs
Data-Clamp Delay Time Option 1 Option 2 Option 3 Option 4	 t_{DCD1} t_{DCD2} t_{DCD3} t_{DCD4}	 5.7 4.135 20.795 104.135	 6 4.17 20.83 104.17	 6.3 4.205 20.865 104.205	 ns ms ms ms
A/D Clock to A/D Strobe Delay Time	t_{ADCD}	1.06	–	1.11	µs
Envelope-to-Dibit Clock Delay Time	t_{ED}	140	–	220	µs
Clock Frequency, ±0.005%	f_{Clk}	–	1.8432	–	MHz
A/D Clock Cycle Time (f_{Clk}/4)	t_{cyc}	–	2.17	–	µs
A/D Clock Pulse Width	$t_{w(ADC)}$	940	1000	1040	ns
A/D Strobe Pulse Width	$t_{w(ADS)}$	–	10.85	–	ns
New Sync Input Pulse Width	$t_{w(NSync)}$	0.84	–	–	ms

*Maximum input transition times are ≤ 0.1X pulse width or the specified maximum of 1.0 µs, whichever is smaller.

FIGURE 2 – DEMODULATOR BLOCK DIAGRAM

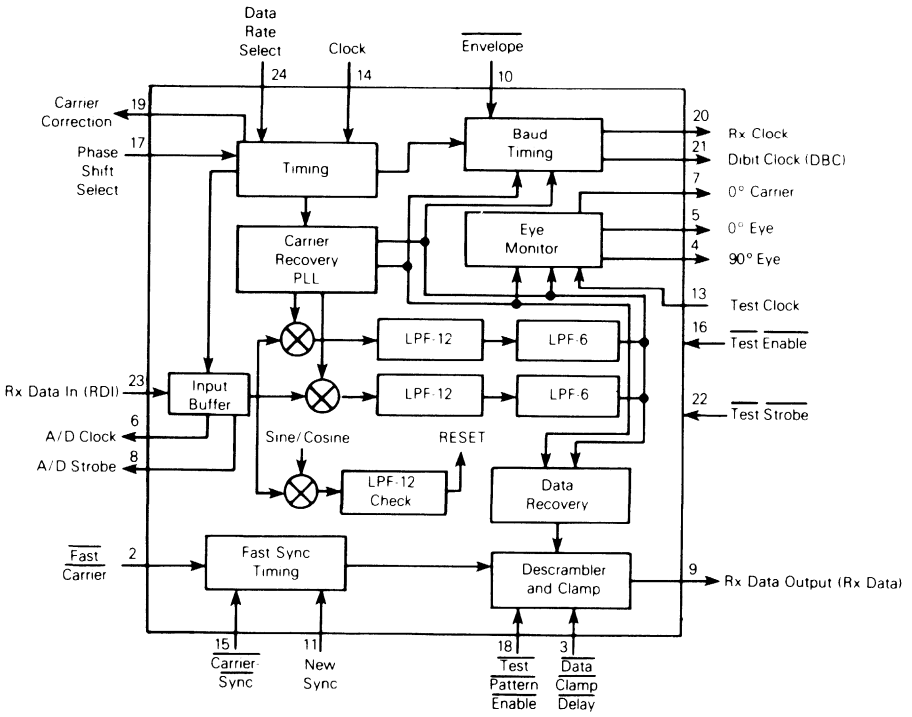
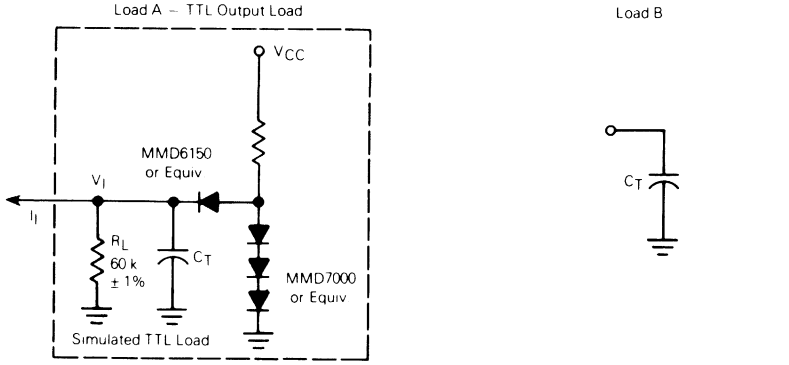


FIGURE 3 – OUTPUT TEST LOADS



C_T = 20 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances

GENERAL DESCRIPTION

The MC6173 Phase-Shift Key (PSK) Demodulator serves as an integral part of a system to recover synchronous data from an 1800 Hz PSK modulated carrier. Data rates of 1200 and 2400 bits-per-second are available. In the case of 1200 bps operation, the MC6173 detects phase shifts of 0 to 180 degrees to represent digital "0s" and "1s". When 2400 bps operations is desired, the MC6173 detects phase shifts of 0, 90, 180, and 270 (option A) or 45, 135, 225, and 315 (option B) degrees to represent two bits of data called dibits. These phase shifts decode to 00, 01, 10, and 11, respectively. In either data rate, the 1800 Hz carrier is modulated at a 1200 rate.

Figure 1 shows the MC6173 demodulator in a typical application. The band-pass filter, equalizer, analog-to-digital (A/D) converter, 1200 Hz envelope filter, AGC amplifier, and 1800 Hz carrier detector are external to the MC6173. The band-pass filter passes roughly 300 Hz to 3000 Hz eliminating noise, 60 Hz and 120 Hz pickup, and harmonics of 1800 Hz. The output of this filter is fed to the equalizer which adjusts phase versus amplitude such that a constant amplitude is maintained regardless of phase and is fed into the carrier detect circuit. The AGC amplifier provides a constant level signal regardless of the input level from the equalizer. The output of the AGC amplifier drives two basic sections of external circuitry, i.e., the A/D converter, and 1200 Hz envelope filter.

The A/D converter samples each 1200 Hz cycle or dibit 12 times. After each sample, digital data is clocked serially to the MC6173 receiver data input (RDI). The MC6173 generates the sampling clock for AD Strobe (ADS) and the serial clock (ADC) from the 1.8432 MHz internal oscillator.

The 1200 Hz envelope filter recovers the 1200 Hz component of the equalizer output during fast training and generates a 1200 Hz square wave. This square wave is connected to the envelope ($\overline{Env}$) input and is used for internal timing.

The carrier detect circuit is used to signal the fast carrier ($\overline{FCar}$) input that a carrier is present. Immediately after $\overline{FCar}$ has received a negative transition, the internal phase-lock loop temporarily widens its band width so that it can quickly adjust the internal timing of the MC6173 with respect to the 1200 Hz $\overline{Env}$ input (this is called fast Sync or fast training). The timing adjustments are made so that each dibit can be sampled at the most advantageous places.

The internal circuitry digests the dibit samples and produces the digital data (Rx Data) along with the receive data clock (Rx Clk). These two signals are used to drive a serial-to-parallel interface such as an MC6852 Synchronous Serial Interface Adapter.

PIN DESCRIPTION

FAST CARRIER ($\overline{FCar}$), Pin 2 – A negative transition on this input will force a period of approximately 8.3 ms of fast training for both baud and carrier timing.* Fast Sync or fast training allows for large corrections to be made in the internal timing of the demodulator. After the fast training period, the timing should be reasonably well adjusted. Small adjustments are made automatically to maintain proper phase relationships internally after the fast train period.

The $\overline{FCar}$ input, which normally comes from the carrier threshold detect circuits, must remain at a low level during the entire period of baud and carrier synchronization.

A positive level on the $\overline{FCar}$ input will disable the baud and carrier correction circuitry. Baud and carrier timing are then direct derivatives of the 1.8432 MHz clock as illustrated in Figure 4.

The first positive edge of the envelope ($\overline{Env}$) input will be totally asynchronous to the demodulator. This will be ± ½ cycle of the 2400 clock (± 208 μs). The nine following positive edges will introduce added tolerance equal to nine times the offset of $\overline{Env}$ from the absolute 1200 Hz (as defined by the 1.8432 MHz ± 0.005% clock). Thus . . .

$$\text{Max Fast Train Time} = 4.17 \text{ ms} + 9\, f_{\overline{Env}} + 0.21 \text{ ms}$$
$$= 4.38 \text{ ms} + 9/f_{\overline{Env}}$$
$$\text{Min Fast Train Time} = 4.17 \text{ ms} - 0.21 \text{ ms} + 9/f_{\overline{Env}}$$
$$= 3.96 \text{ ms} + 9/f_{\overline{Env}}$$

DATA-CLAMP DELAY ($\overline{DCD}$), Pin 3 – Data-clamp delay enables the selection of one of four delays during which Rx Data is held to a logic-high condition. This delay is measured from the negative edge of $\overline{FCar}$. The four options are available at one pin through the use of the internal multiplexing in the demodulator. Options 3 and 4 are available by demultiplexing the dibit clock as demonstrated in Figure 5. The available delay options are listed in Table 1, these times will be approximate due to their direct relationship to the $\overline{Env}$ input during the first 8.3 ms. Also, these times are further dependent upon carrier offset. The delays given in Table 1 assume no carrier offset and that $\overline{Env}$ is synchronous with the Tx Clk. Figure 4 is illustrative of the timing and sequencing of this circuit.

A scheme for programming the data-clamp delay is illustrated in Figure 5. The $\overline{DCD}$ input may either be a constant high or low level which will produce options 1 and 2. If the input "A" is exclusive ORed with the dibit clock options 3 and 4 are produced at the same input pin.

ENVELOPE ($\overline{Env}$), Pin 10 – The envelope input comes from the 1200 Hz envelope detection circuitry. Envelope detection will normally consist of a 1200 Hz filter and a voltage comparator to generate an approximate limited square wave. This is normally derived from a constant mark signal sent by the modulator for Sync acquisition purposes.

Each positive edge that is input to $\overline{Env}$ will reset both baud timing and the dibit clock to a logic "0". The optimum timing of the positive transition at the $\overline{Env}$ input will be t_{ED} prior to the falling edge of the dibit clock. Timing is illustrated in Figure 6.

$\overline{Env}$ will be effective in the training of baud timing and dibit clock only if $\overline{FCar}$ is in the active low state.

Minimum positive pulse width at the $\overline{Env}$ is ≥2.17 μs.

NEW-SYNC ($\overline{NSync}$), Pin 11 – This input port is normally controlled by the business machine. If $\overline{FCar}$ is at an active low, then an active low pulse in excess of 0.84 ms on the $\overline{NSync}$ lead will put the demodulator into the fast-Sync

*The postive transition of the 1200 Hz signal, present at the $\overline{Env}$ input, provides a divide-by-20 counter with every other clock. This will cause approximately 8.3 ms of fast training to the incoming signal at the demodulator.

FIGURE 4 – DEMODULATOR SYNC TIMING DIAGRAM

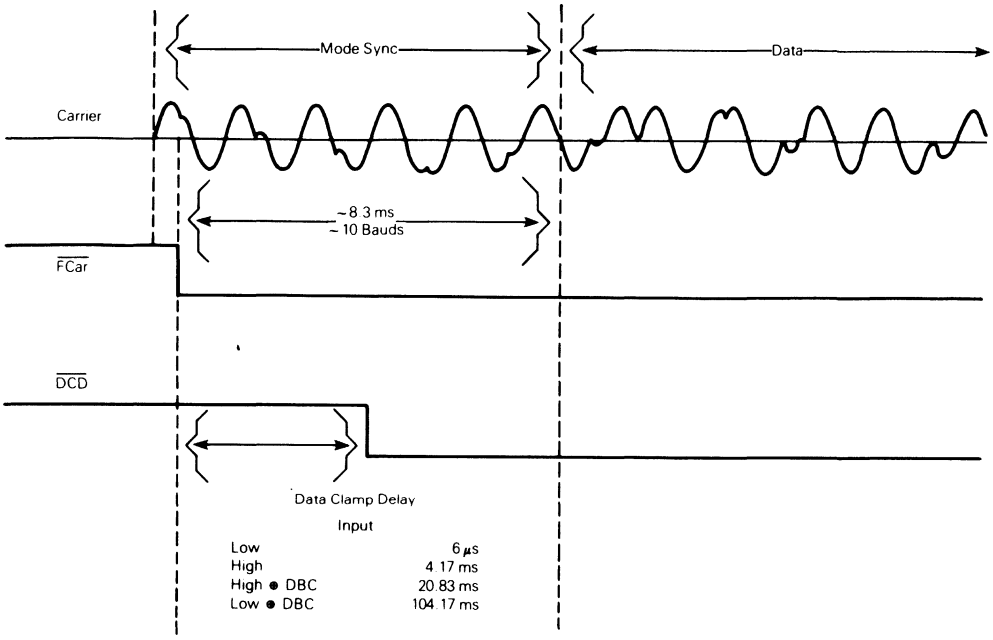


TABLE 1 – DATA-CLAMP DELAY OPTIONS

Option	A	C	$\overline{DCD}$	Data-Clamp Delay
1	1	0	0	6 μs
2	0	0	1	4.17 ms ± 35 μs
3	1	DBC	DBC	20.83 ms ± 35 μs
4	0	DBC	$\overline{DBC}$	104.17 ms ± 35 μs

FIGURE 5 – DATA-CLAMP DELAY DEMULTIPLEXER

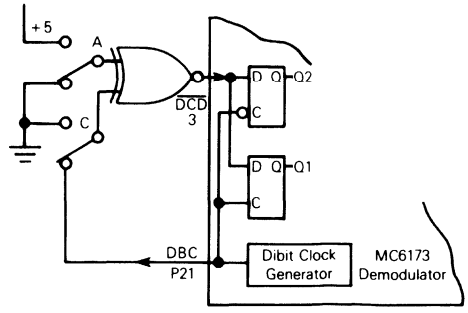
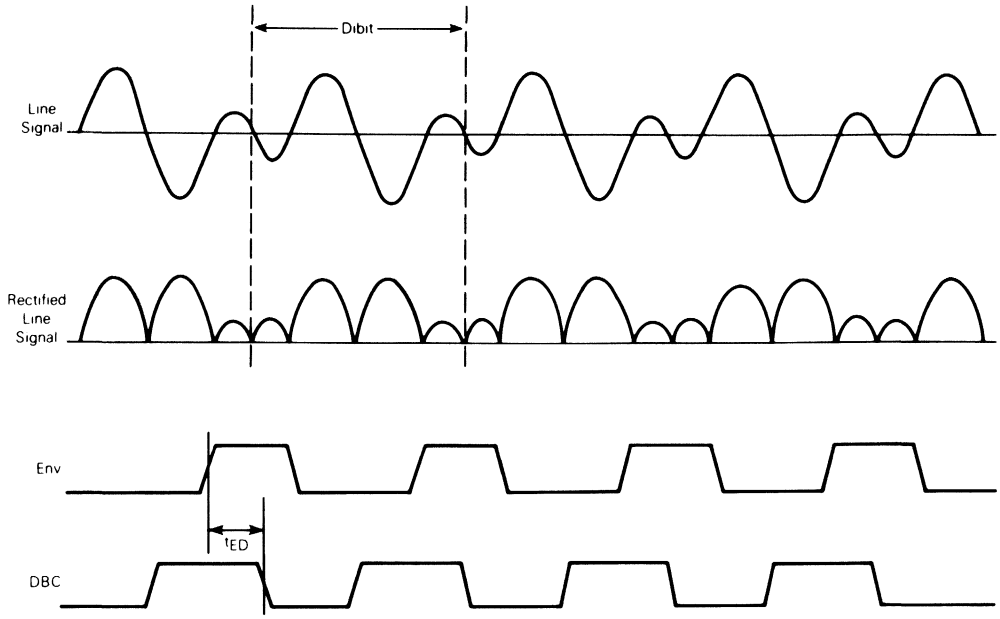


FIGURE 6 – ENVELOPE CLOCK TIMING DIAGRAM



or fast-train mode (these terms are synonymous).

Activation of $\overline{\text{NSync}}$ allows large corrections to be made to both baud and carrier timing similar to initial activation of the $\overline{\text{FCar}}$ lead. These corrections will be applied for approximately 8.3 ms. The receiver must complete the 8.3 ms period of fast Sync before another $\overline{\text{NSync}}$ is recognized.

$\overline{\text{CARRIER-SYNC}}$ ($\overline{\text{CarS}}$), Pin 15 – When $\overline{\text{CarS}}$ is taken to an active low, baud timing will be taken from the $\overline{\text{Env}}$ input. In addition, the slow carrier correction will be doubled in the 2400 baud mode as defined by the data-rate select (DRS) and phase-shift select (PSS) inputs. (This is not the same as the fast training that is incorporated when $\overline{\text{FCar}}$ or $\overline{\text{NSync}}$ are active, which is a changing of the bandwidth of the internal phase-lock loop [PLL]). This widening of the PLL band width will allow a faster search and lock on the 1800 Hz carrier. This Carrier-Sync mode will remain active as long as $\overline{\text{CarS}}$ is held in the active state. The normal application of this option would be to extend the training or Sync time under the mark input data condition that exceeds 8.3 ms.

If $\overline{\text{FCar}}$ is at a logic "1" inactive state, this input is ignored by the demodulator.

A/D CLOCK (ADC), Pin 6 – This output will allow, in a serial format, the six A/D data bits plus sign information to be synchronously clocked into the demodulator. (See Figure 8.)

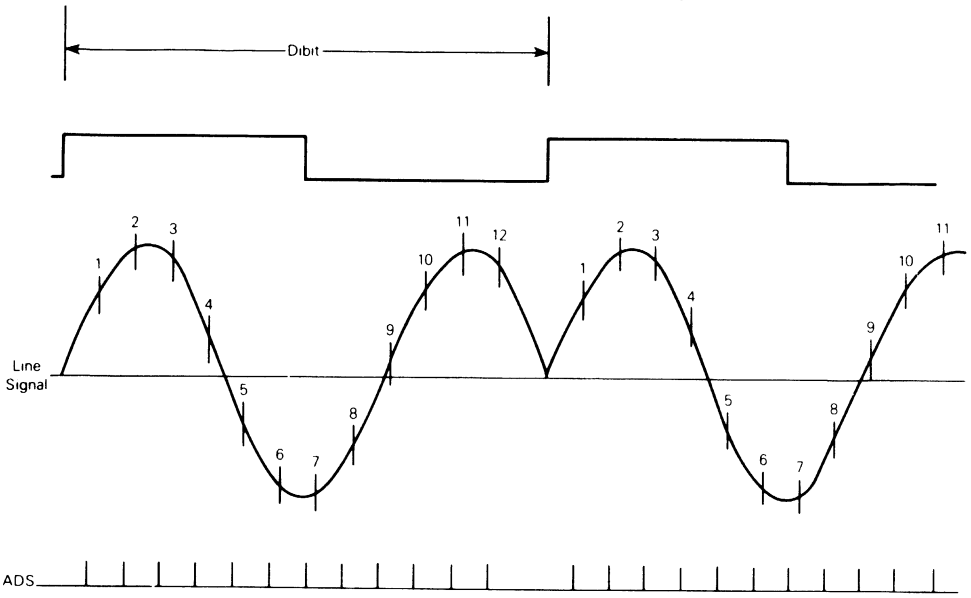
There are nine 1 μs positive pulses occuring at a 460 kHz rate. The first pulse, along with ADS, is used to begin the A/D conversion sequence. The next seven positive edges strobe data serially from the A/D converter to the demodulator input (RDI) enabling the demodulator to properly decode the A/D data.

This signal is also used to clock 0 and 90 degree eye data out of the demodulator. This is described in the Eye Pattern section. When $\overline{\text{TEn}}$ is low, ADC monitors check accumulator output (see $\overline{\text{TEn}}$).

A/D STROBE (ADS), Pin 8 – A positive going, approximately 11 μs, pulse is used as an enable signal for a sample and hold circuit prior to the A/D converter. The negative edge of this pulse is used to start the conversion process. Pulse rate of this signal is 14.4 kHz which allows each dibit to be sampled 12 times. (See Figure 7.) When $\overline{\text{TEn}}$ is low, ADS monitors zero crossings (see $\overline{\text{TEn}}$).

RECEIVER DATA INPUT (RDI), Pin 23 – The digital decode of the line signal magnitude, as sampled by the A/D, is input to the demodulator at this port. The data format is scaled binary. This sign bit occurs on the second A/D clock, followed by six magnitude bits which begin with the most-significant bit as shown in Figure 8. The data is strobed syn-

FIGURE 7 – ANALOG TO DIGITAL SAMPLE SCHEME



chronously with the positive edges of the ADC.

A logic one in the sign bit slot will represent a positive value. The magnitude of the six data bits increases from 000000 to 111111 with all ones always representing the most-positive value as illustrated below:

Sign	MSB					LSB	Value
1	1	1	1	1	1	1	+63
1	0	0	0	0	0	0	0
0	1	1	1	1	1	1	−0
0	0	0	0	0	0	0	−63

RECEIVE DATA OUTPUT (Rx Data), Pin 9 – This pin is the demodulator output for mark and space serial data. Data is synchronous with the receiver clock output with the positive going edge of the receiver clock occurring in the center of the data bit. A mark is represented by a logic high ("1") level except for the conditions described under PSS and $\overline{TPE}$.

The Rx Data output is inhibited in a logic-high level when $\overline{FCar}$ is in the inactive high state. The delay from the positive edge of $\overline{FCar}$ to the inhibiting of data is 2 μs.

RECEIVE CLOCK (Rx Clk), Pin 20 – The receive clock output provides the 2400 Hz ±0.005% timing signal to the business machine for sampling the demodulated received data marks and spaces (Rx Data). Receive clock is present at the demodulator chip output at all times, is not clamped to an inactive state when the carrier detected is not presented on $\overline{FCar}$, nor is Rx Clk clamped by any other combination of inputs to the demodulator.

Timing corrections to the receive clock, that are generated internally, are made following $\overline{FCar}$ going active. As described in $\overline{FCar}$, if $\overline{CarS}$ is held active the receive clock is continuously updated from dibit Sync.

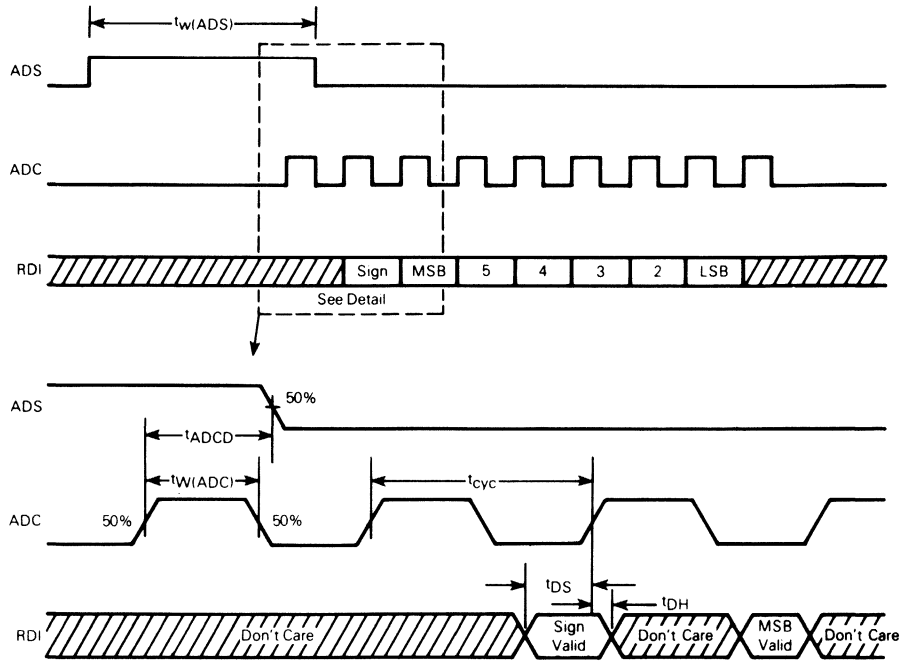
The positive transition of the Receive Clock, which occurs in the middle of the data bit, should be used to strobe data from the demodulator, under normal operating conditions. When $\overline{TPE}$ scrambler/descrambler is being incorporated, then the negative edge of the Rx Clk will occur in the center of the data bit.

Receive Clock will be 2400 bps or 1200 bps depending on the logic input at the DRS input. The Rx Clk edges described above apply to either 2400 bps or 1200 bps data rates.

Under $\overline{TPE}$ active, the Dibit relation to Rx Clk does not change. See Figure 9 for relative timing of Rx Clk, DBC and Rx Data.

Figure 10 depicts the requirements at the demodulator if the data scrambler is being incorporated. The exclusive Nor gating of $\overline{TPE}$ and Rx Clk would then maintain proper phasing of Rx Clk as it goes to the RS-232 driver. This circuit would be required since the positive edge of Receive Clock is a Data Communications Standard.

FIGURE 8 – ANALOG-TO-DIGITAL TIMING DIAGRAM



DATA RATE SELECT (DRS), Pin 24 – The following levels are valid for either phase-shift select:

Logic high equals 2400 bps,
Logic low equals 1200 bps.

PHASE-SHIFT SELECT (PSS), Pin 17 – Option A (CCITT) or option B (U.S.) phase shift can be selected for 2400 bps operation. The input data format and phase shift relationship for these two options are as follows:

Data	PSS = 0 Option A (Degrees)	PSS = 1 Option B (Degrees)
00	0	+ 45
01	+ 90	+ 135
11	+ 180	+ 225
10	+ 270	+ 315

For 1200 bps operation, option A (CCITT) or option B (U.S.) phase shift can be selected as follows:

Data	PSS = 0 Option A (Degrees)	PSS = 1 Option B (Degrees)
0	+ 90	+ 45
1	+ 270	+ 225

The phase shifts shown are the difference in phase between the signal at the end of one dibit period and the new signal at the beginning of the next dibit.

If the logic level inputs to PSS are EXORed with DBC (dibit clock) or $\overline{DBC}$, then the test-pattern enable option may be selected and produce the compliment of normal data at Rx Data as explained in the $\overline{TPE}$ description. (See Figure 11.)

$\overline{TEST\text{-}PATTERN\ ENABLE}$ ($\overline{TPE}$), Pin 18 – Incorporated in the demodulator is the 511-bit test pattern shift register that is in accord with CCITT specification V52. This is the pattern that is generated by feedback from the 5th and 9th stages of a 9-bit shift register.

When the $\overline{TPE}$ input is allowed to be pulled up internally, there is normal data flow through the receiver. When the $\overline{TPE}$ input is pulled low, the incoming data is passed through this self-synchronous decoder which will produce the inverse of the 511-bit CCITT V52 pattern.

$\overline{TPE}$ works in coordination with PSS. If PSS is directly pulled high or low to represent option A or option B, then the presence of the 511-test pattern at the (RDI) input and $\overline{TPE}$ active will result in logic "1" condition at Rx Data output. If the DBC option is being utilized at the PSS input and $\overline{TPE}$ is active while the 511-bit test pattern is being received, the receiver data output will equal a logic "0". These options (Figure 11) are summarized in Table 2.

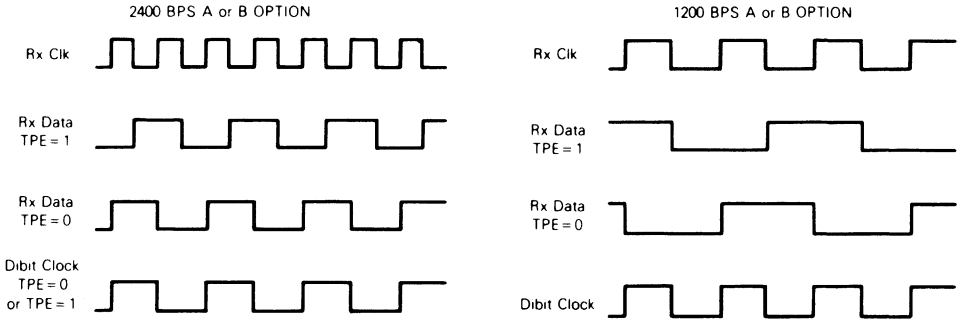
This assumes the modulator is sending the 511-bit test pattern with Rx Data being either a constant mark (logic "1") or space (logic "0"). If a logic "0" is received in options 1 or 2 or a logic "1" is received in options 3 or 4, then a transmission error has occurred. The number of errors-per-unit time is a measure of the transmission line quality.

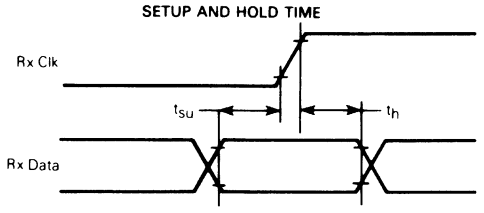
A feature of the above type of pattern detector is that it will be self-synchronizing. It should be pointed out that there will be at least two error counts each time an error is detected.

If the $\overline{TPE}$ input is in the active state, it is important to note that the Rx Clk phase changes. The necessary circuit to regain proper phase is shown in Figure 10.

A scheme for programming the phase-shift select is illustrated in Figure 11. The PSS input may either be a constant high or low level which will produce options 1 and 2. If the input "A" is exclusive ORed with the dibit clock, options 3 and 4 are produced at the same input pin.

FIGURE 9 – CLOCK TIMING DIAGRAM





Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

FIGURE 10 – DEMODULATOR DATA SCRAMBLER RECEIVE CLOCK PHASE CORRECTION REQUIREMENTS

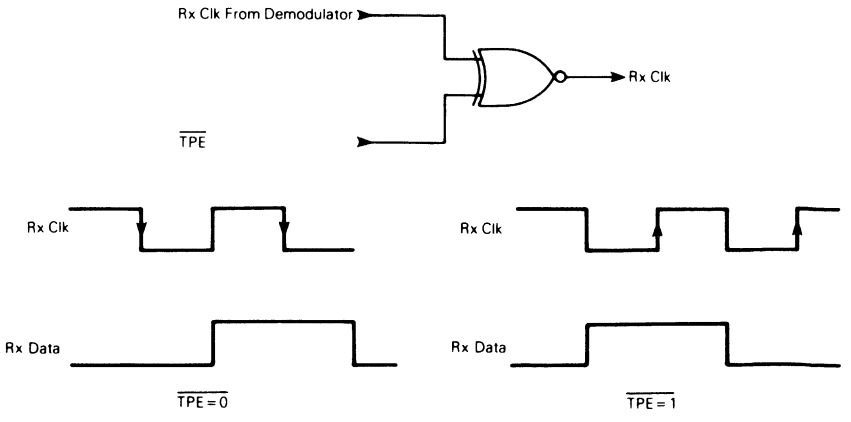


FIGURE 11 – PHASE-SHIFT SELECT DEMULTIPLEXER FOR TEST PATTERN ENABLE

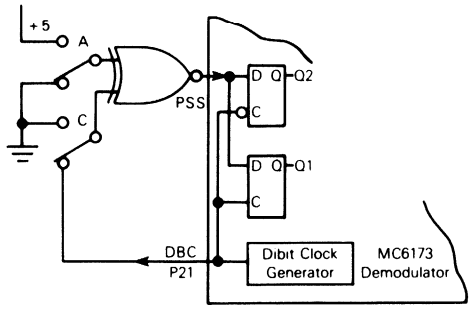


TABLE 2 – TEST PATTERN ENABLE OPTIONS

Option	$\overline{TPE}$	A	C	Phase Option	PSS	Output State
1	0	1	0	A	0	Rx Data Output = 1
2	0	0	0	B	1	Rx Data Output = 1
3	0	1	DBC	A	DBC	Rx Data Output = 0
4	0	0	DBC	B	$\overline{DBC}$	Rx Data Output = 0

CLOCK (Clk), Pin 14 – A 1.8432 MHz signal input ±0.005% is required at this port. The clock requirements are the same as the modulator clock specifications. See Figure 12 for a suggested clock circuit.

The receive clock is generated by dividing down the 1.8432 MHz. Since receive clock accuracy must be at least ±0.005%, the clock source must be of the same accuracy.

TEST-CLOCK (TClk), Pin 13 – This input is used for production testing of the demodulator device. In normal operation this pin should be left open which will enable the internal pullup resistor.

Pin 5	0 Degree Eye
Pin 4	90 Degree Eye
Pin 7	0 Degree Carrier
Pin 19	Carrier Correction

These test outputs are explained in the test enable ($\overline{TEN}$) description below.

$\overline{TEST}$ $\overline{ENABLE}$ ($\overline{TEn}$), Pin 16; 0° Eye, Pin 5; 90° Eye, Pin 4; 0° Car, Pin 7; CCor, Pin 19 – These pins allow the monitoring of ten internal points within the demodulator. A low level on $\overline{TEn}$ is normally associated with testing of the demodulator such as in a production test environment or incoming testing. Activation of $\overline{TEn}$ affects internal timing.

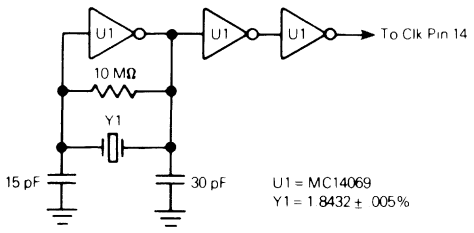
TABLE 3 – INTERNAL MONITORS

Output	$\overline{TEn}$	Function
ADS (Pin 8)	H	See Description Under ADS (Pin 8)
	L	Monitors Zero Crossings
ADC (Pin 6)	H	See Description Under ADC (Pin 6)
	L	Monitors Check Accumulator Output
0 Degree Eye (Pin 5)	H	Monitors 0 Degree Eye 2s Complement Information from 6 Tap Filter
	L	Monitors 0 Degree Eye 2s Complement Information from 12 Tap Filter
90 Degree Eye (Pin 4)	H	Monitors 90 Degree Eye 2s Complement Information from 12 Tap Filter
0°Car (Pin 7)	H	Monitors 0 Degree Carrier
	L	Monitors Check Accumulator Compare Errors
CCor (Pin 19)	H	Monitors Carrier Correction Enable
	L	Monitors Carrier Correction Direction

DIBIT CLOCK (DBC), Pin 21 – This output is a 1200 Hz clock which is derived from incoming data envelope and provides a dibit reference. This signal is representative of "data derived timing." When studying the quality of the demodulated signal, through the use of eye patterns, this output is necessary for proper synchronization of the oscilloscope.

$\overline{TEST}$ $\overline{STROBE}$ ($\overline{TStr}$), Pin 22 – This input is used to facilitate testing of the demodulator during the manufacturing process. It should be left unconnected which will result in

FIGURE 12 – OSCILLATOR CONFIGURATION



the internal pullup resistor causing the high level on this pin.
V_{SS} Pin 1 = The most negative supply, typically ground.
V_{CC} Pin 12 = The most positive supply, typically 5 volts.

DATA SCRAMBLER

The scrambling of data in the data communication environment is not done in an attempt to encrypt information in the normal sense of the word. Rather, the purpose of the scrambling of data is to guarantee that, with respect to the modem carrier, there is always random data on the line with little chance for a long string of "1s" or "0s" to exist. This is particularly important if an adaptive equalizer is being incorporated in the modem as the adaptive equalizer will require reasonably evenly distributed data to optimize its statistical response to the incoming signal. The normally used code is the CCITT 511 sequence which is EXORed with data.

The Motorola 2400 bps modulator contains a CCITT 511-bit test-pattern generator. It does not, however, incorporate the 511 data randomizer or scrambler. To scramble data using the MC6172 modulator, the circuit in Figure 10 must precede the Tx Data input of the modulator. Tx Data is added to the scrambler output pattern; then, the data is delayed by a full data bit before being transmitted by the modem. This assures a proper transmit-data/transmit-clock phase relationship. If the data scrambler is to be an optional feature, then the transmit-data multiplexer would also have to be built. This is selected by the test-pattern enable signal or any other signal that is found suitable.

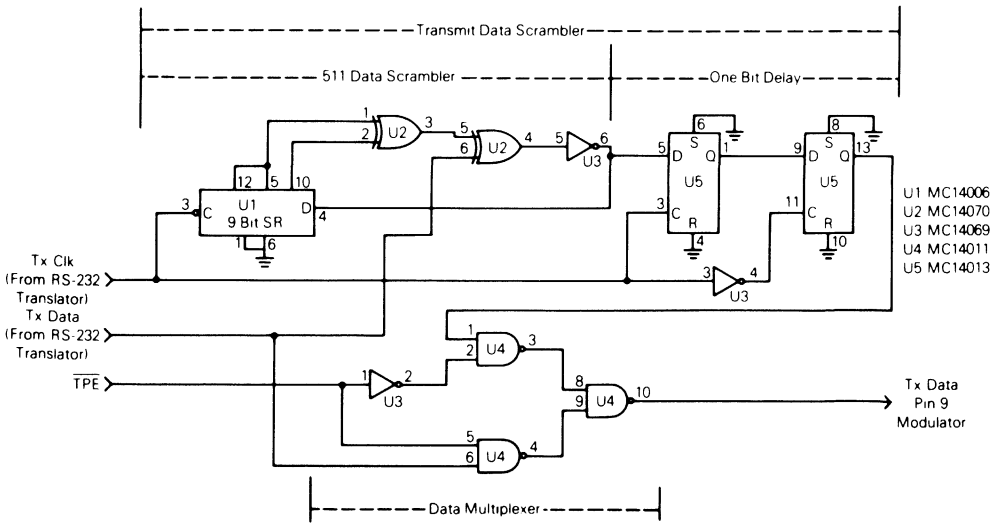
The demodulator does contain a built-in data descrambler which is enabled by the $\overline{TPE}$ input going active. The receive phasing, with respect to data, changes when $\overline{TPE}$ goes active. The exclusive NOR gating of $\overline{TPE}$ and Rx Clk, as shown in Figure 10 will maintain proper phase of Rx Clk. This circuit is required since the clocking of data on a positive edge is a data communications standard.

EYE PATTERN

When performing an evaluation of an 2400 bps modem, one common point of comparison is the quality of the eye patterns produced by the demodulator. The eye pattern may also be used as an indicator of the incoming signal with respect to level and line perturbations. Eye patterns are for test and evaluation only and are not used in the demodulation of the incoming signal.

Timing information in the Motorola 2400 bps demodulator is derived directly from the demodulated data signal. This is referred to as data derived timing. The advantage of data

FIGURE 13 – MODULATOR CCITT 511 DATA SCRAMBLER



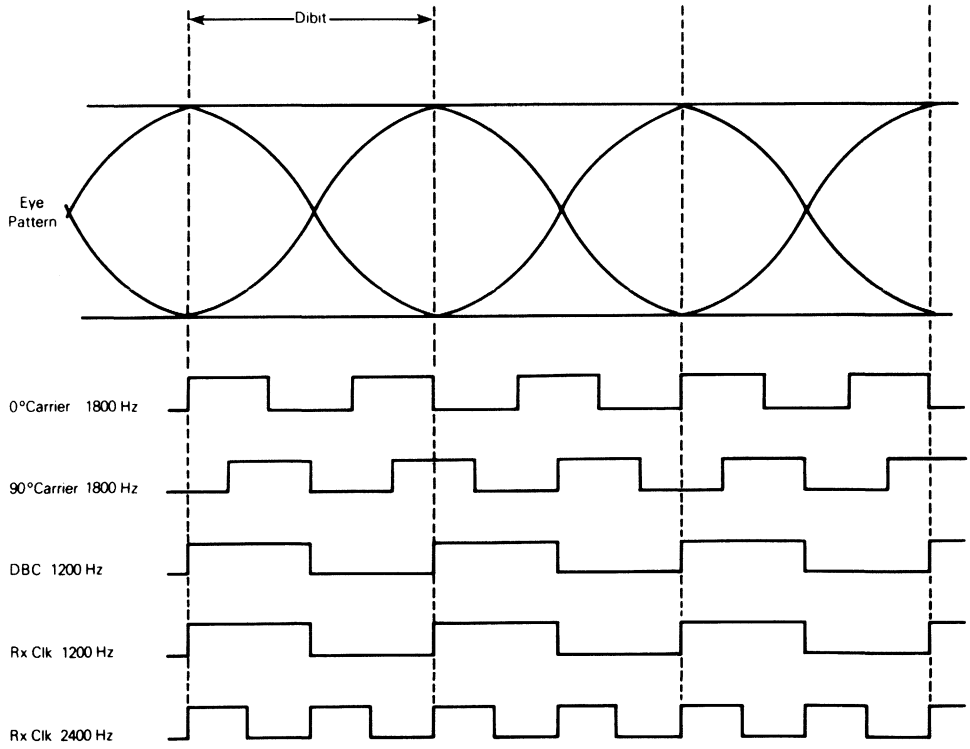
derived time is that it allows data to be sampled at optimum times. The demodulated signals, in differential phase-shift keying, take the form of "eye patterns" as shown in Figure 14. The demodulator, in optimizing its performance for minimum error rates, strobes data at the point of maximum eye opening. The demodulator constantly examines the eye opening to assure that the data sample is being taken at exactly the optimum point. As a result of constantly adjusting timing control, correct sampling is maintained. This technique provides improvements in reception that are significant, especially in a poor communications media environment.

The circuit in Figure 16 is required to observe the eye patterns. This circuit was built using Motorola CMOS devices. The 0 and 90 degree eye data is strobed from pins 4 and 5, respectively, into the shift register by the A/D clock. The A/D strobe then latches the data sample into the "D" type storage devices. The output of the storage devices taken across the scaled resistors will then represent the appropriate value of the sample taken. To properly observe the actual eye patterns, it is necessary to Sync on dibit clock while observing the 0 to 90 degree eye data. Overlaying the two patterns produces a two-level digital-eye pattern from which the quality of the incoming signal may be judged.

Figures 15 thru 17 show a typical receive/demodulator and transmit/modulator circuit, respectively. The transmit filter illustrated in Figure 17 limits the bandwidth of the signal to those frequencies allowed on a telephone line. The receive filter and equalizer in Figure 15 clean up and normalize the incoming signal for the A/D network, 1200 Hz envelope detector, and 1800 Hz carrier detector.

3

FIGURE 14 – EYE PATTERN



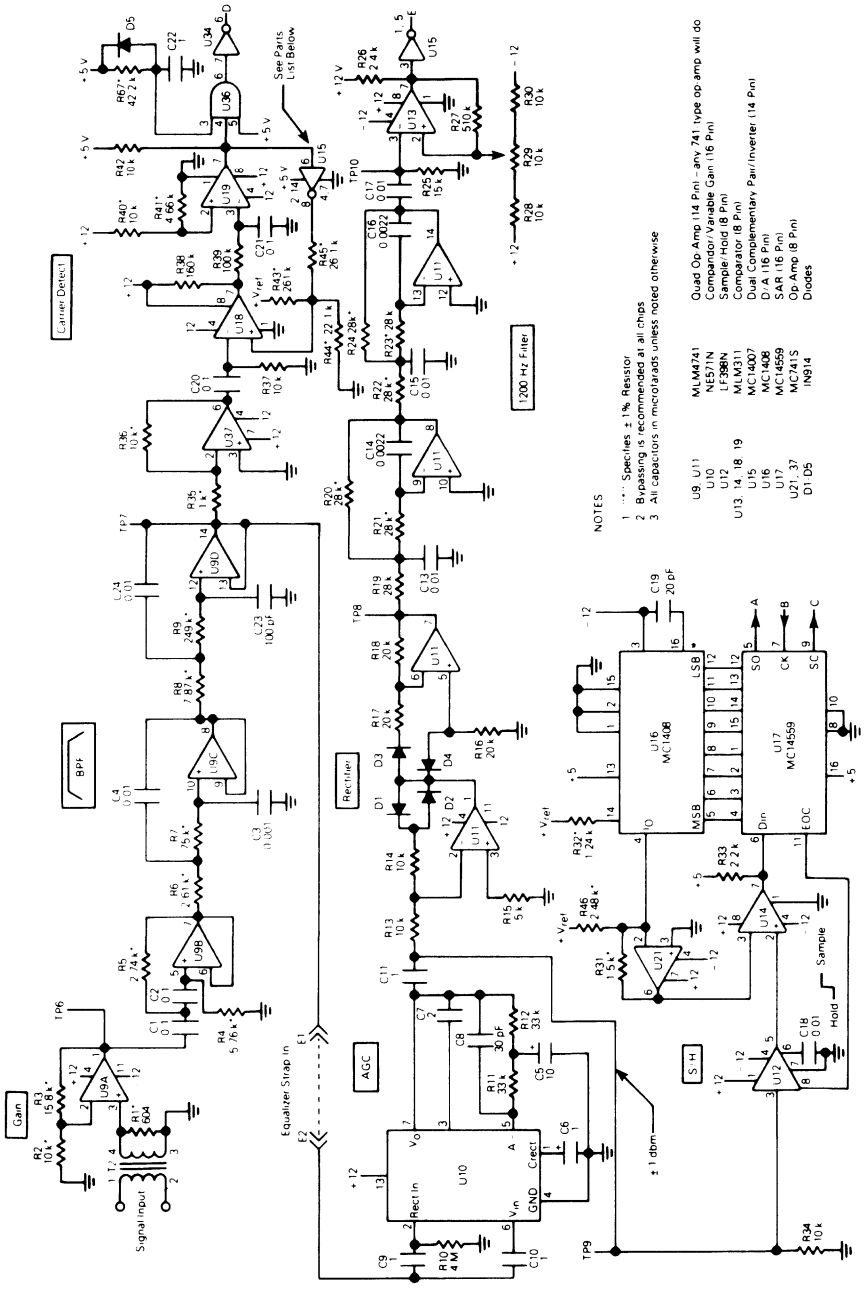


FIGURE 15 — 2400 BPS DPSK DEMODULATOR SYSTEM

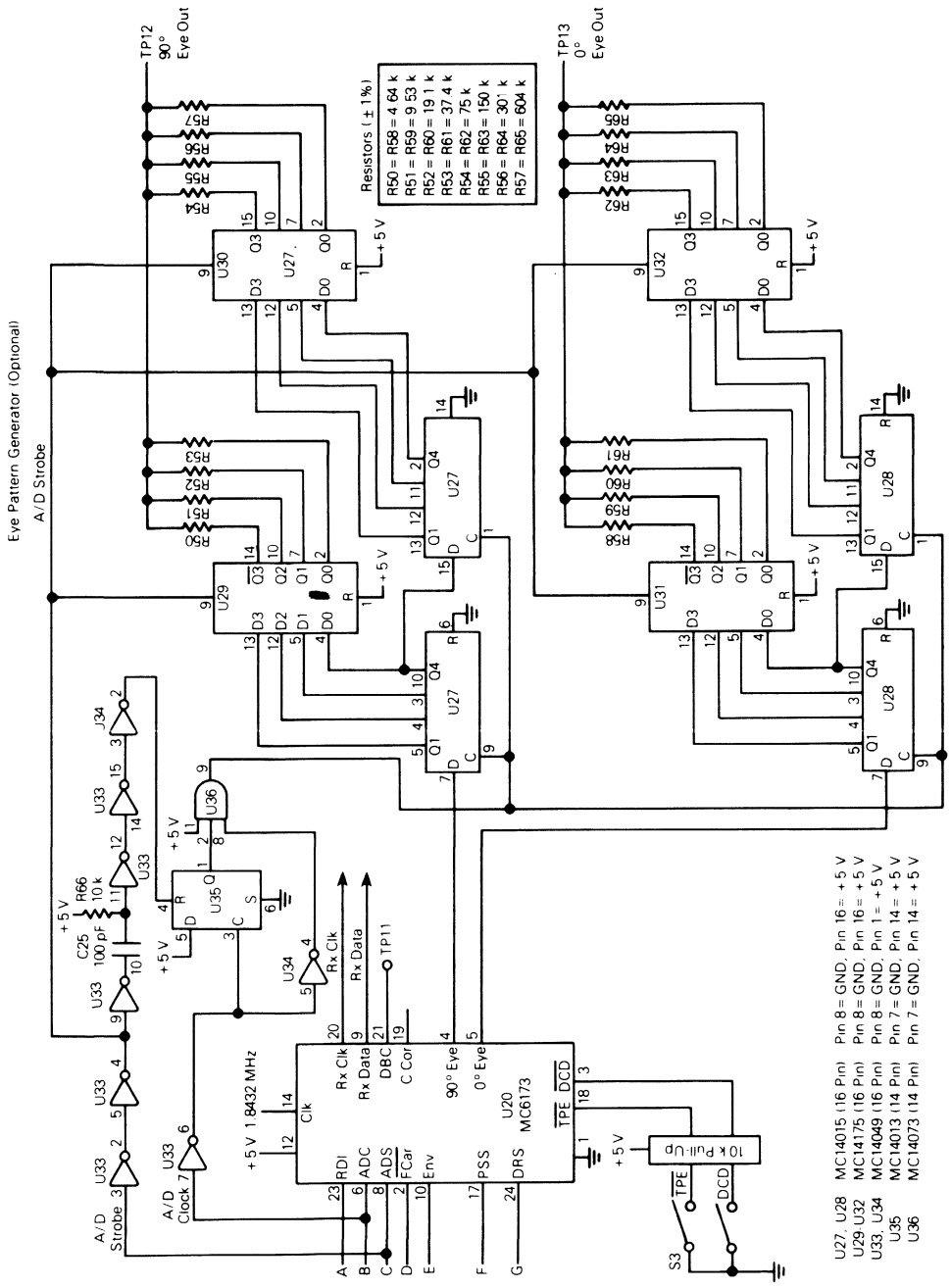


FIGURE 16 – 2400 BPS DPSK DEMODULATOR SYSTEM

3

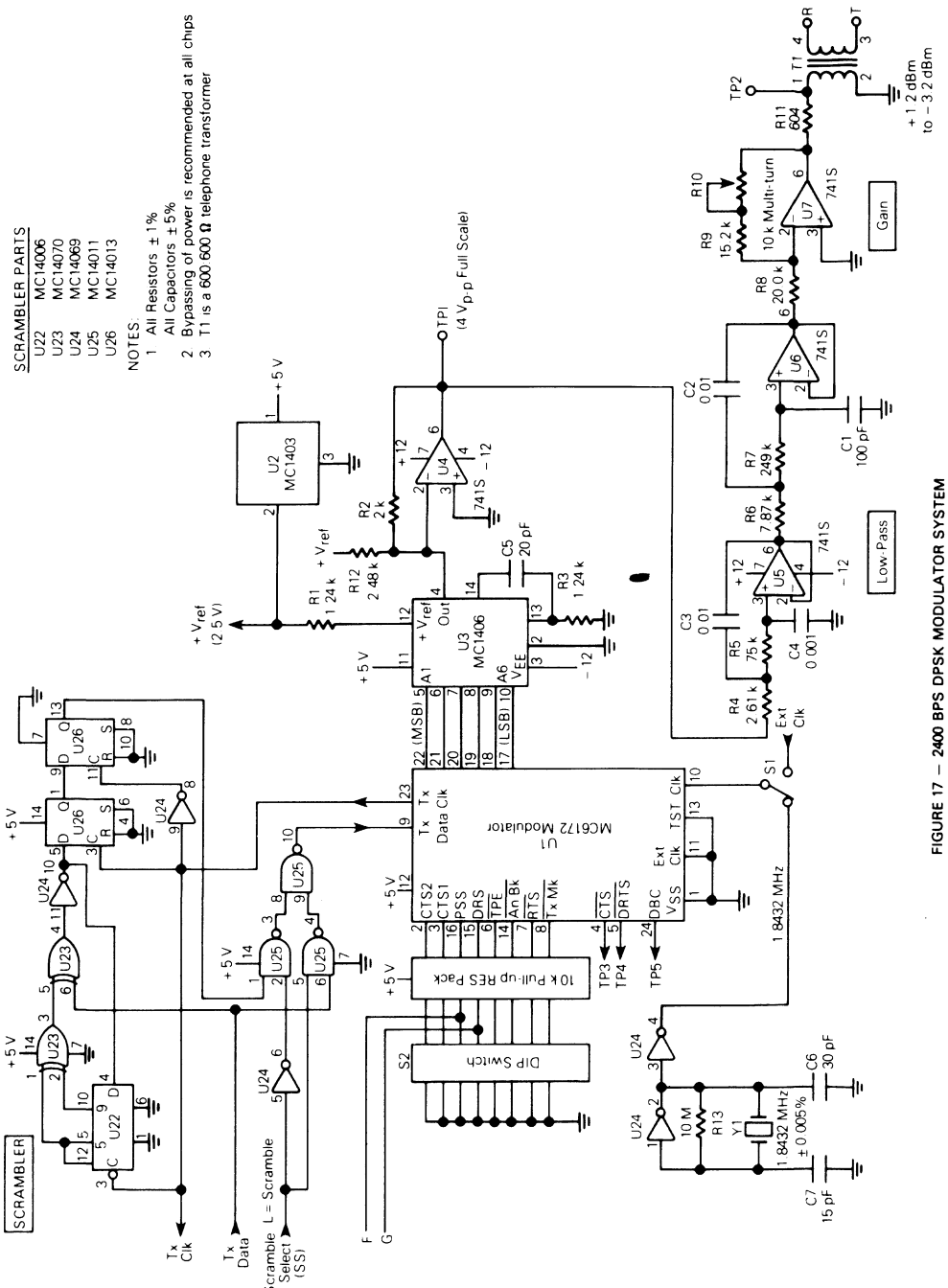


FIGURE 17 — 2400 BPS DPSK MODULATOR SYSTEM

MOTOROLA

MC14408
MC14409

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

BINARY TO PHONE PULSE CONVERTER SUBSYSTEM

3

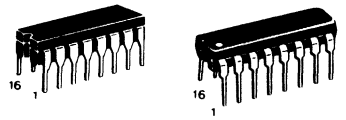
BINARY TO PHONE PULSE CONVERTER SUBSYSTEM

The MC14408 and the MC14409 are devices designed to convert a four bit binary input code to a number of serial output pulses corresponding to the value of the input code.

The devices can be used in telephone pulse dialing applications when combined with their companion device, the MC14419 (2-of-8 keypad-to-binary code converter). The devices have been partitioned to allow convenient addition of RAM memory and controls for repertoire dialing applications.

The MC14408 and MC14409 perform identical functions with the exception of the signal output at the DRO (Dial Rotating Output). In the MC14408, DRO remains high during continuous outpulsing of all digits and in the MC14409 DRO is low between each digit pulse burst.

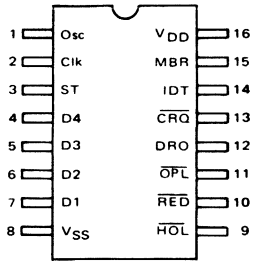
- On-Chip Oscillator
- Diode Protection on All Inputs
- Dialing of Numbers Up to 16 Digits Long
- Memory Storage (FIFO) and Re-Dialing (single pin) of Last Telephone Number
- Hold Interrupt Control for Additional Interdigit Delays (such as a Wait for Intermediate Dial Tones)
- Selectable Dialing Rate (10 pps or 20 pps)
- Selectable Interdigit Time (300 or 800 ms @ 10 pps; 150 or 400 ms @ 20 pps)
- Selectable Make-Break Ratio (61% or 67%)
- Buffered Outputs Compatible with Discrete Transistor Driver Interface, One Low-power Schottky TTL Load or Two Low-power TTL Loads Over the Rated Temperature Range.
- Low Power Dissipation – I_{DD} (operating with oscillator) = 470 μA typ @ V_{DD} = 5.0 Vdc, f_{Osc} = 16 kHz, C_L = 50 pF



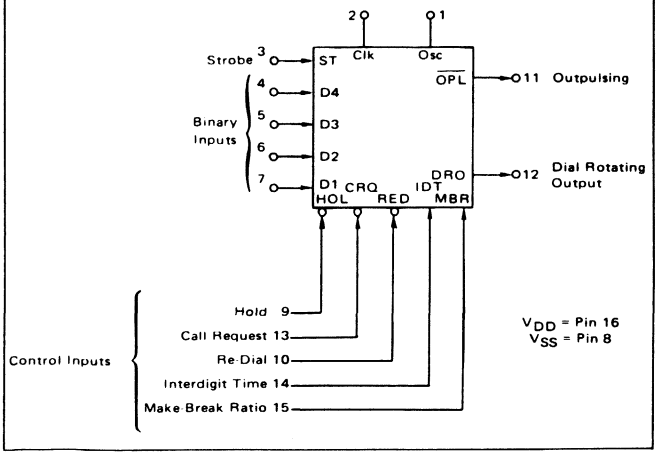
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

DS9426R1

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +6.0	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	-40°C Min	-40°C Max	25°C Min	25°C Typ	25°C Max	+85°C Min	+85°C Max	Unit
Supply Voltage	V_{DD}	–	3.0	6.0	3.0	5.0	6.0	3.0	6.0	Vdc
Output Voltage "0" Level	V_{out}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
"1" Level		5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
Noise Immunity										
($\Delta V_{out} \leq$ 0.5 Vdc)	V_{NL}	5.0	1.5	–	1.5	2.25	–	1.4	–	Vdc
($\Delta V_{out} \leq$ 0.5 Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
Output Drive Current	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.0	–	-0.80	-1.7	–	-0.60	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.20	–	-0.16	-0.36	–	-0.12	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
Input Current	I_{in}	6.0	–	0.3	–	±0.00001	±0.30	–	1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	12	–	5.0	12	–	12	pF
Operating Supply Current	I_{DD}	3	–	250	–	160	200	–	200	μAdc
f_{cl} = 16 kHz (operating		5	–	700	–	470	550	–	550	
with Osc)		6	–	1250	–	740	1000	–	1000	

FIGURE 1 – TIMING DIAGRAM – DATA AND STROBE INPUTS

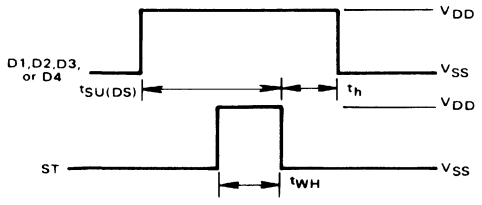
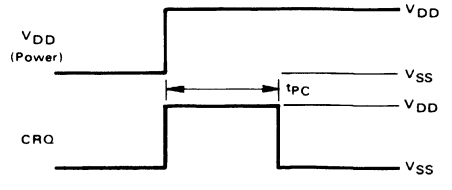


FIGURE 2 – TIMING DIAGRAM – CALL REQUEST



If power is turned off after each call, CRQ must stay high after power is applied (for a duration of t_{PC}) to ensure no spurious outpulsing. For this use the redial function is invalid.

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

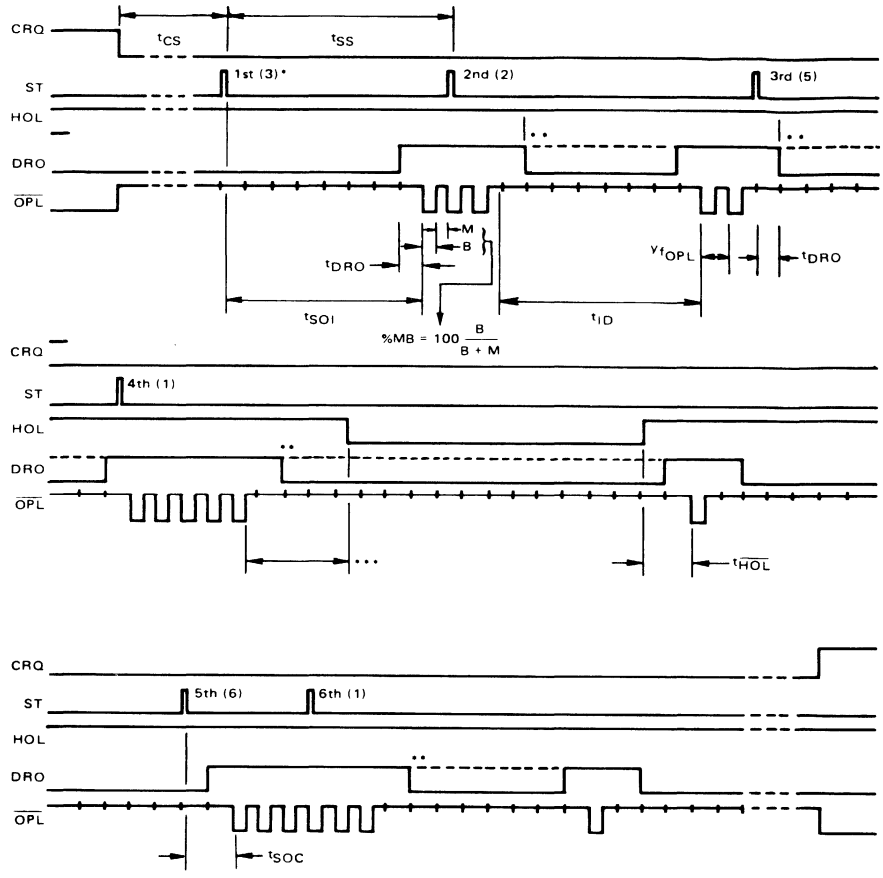
Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time** t_{TLH} = (3.0 ns/pF) C_L + 30 ns	t_{TLH}	5.0	–	180	400	ns
Output Fall Time** t_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	–	100	200	ns
Power Up to Call Request Pause	t_{PC}	3 to 6	48/f_{cl}*	–	–	ms
Call Request to First Strobe Pulse	t_{CS}	3 to 6	48/f_{cl}*	–	–	ms
Strobe to Strobe Separation Time	t_{SS}	3 to 6	48/f_{cl}*	–	–	ms
Strobe Pulse Width	t_{WH}	3 to 6	1.0	–	–	μs
Strobe to Data Hold Time	t_h	3 to 5	–	150	400	ns
Clock Frequency***	f_{cl}	3 to 6	12.5	16	100	kHz
Percent Break to Make Ratio	%MB	3 to 6				%
(MBR = 0)			–	61	–	
(MBR = 1)			–	67	–	
Outpulsing Rate (f_{OPL} = *f_{cl}/1.6)	f_{OPL}	3 to 6				pps
f_{cl} = 16 kHz			–	10	–	
f_{cl} = 32 kHz			–	20	–	
Interdigit Time	t_{ID}	3 to 6				ms
t_{ID} = (5 x IDT + 3)/f_{OPL}						
IDT = 0						
f_{OPL} = 10 pps			–	300	–	
f_{OPL} = 20 pps			–	150	–	
IDT = 1						
f_{OPL} = 10 pps			–	800	–	
f_{OPL} = 20 pps			–	400	–	
Strobe to Output Time	t_{SOI}	3 to 6				ms
Initial Outpulsing Stream						
IDT = 0						
f_{OPL} = 10 pps			300	–	400	
f_{OPL} = 20 pps			150	–	200	
IDT = 1						
f_{OPL} = 10 pps			800	–	900	
f_{OPL} = 20 pps			400	–	450	
Continued Outpulsing Stream	t_{SOC}	3 to 6				ms
IDT = 0 or 1						
f_{OPL} = 10 pps			100	–	200	
f_{OPL} = 20 pps			50	–	100	
Hold to Outpulse Time	t_{HOL}	3 to 6				ms
IDT = 0 or 1						
f_{OPL} = 10 pps			100	–	200	
f_{OPL} = 20 pps			50	–	100	
Dial Rotating Overlap Time	t_{DRO}	3 to 6				ms
f_{OPL} = 10 pps			–	100	–	
f_{OPL} = 20 pps			–	50	–	
Data to Strobe Setup Time (f_{cl} = 16 kHz)	$t_{SU(DS)}$	3 to 6	1.5	–	–	μs
Re-dial Pulse Width (f_{cl} = 16 kHz)	–	3 to 6	500	200	–	ns

*f_{cl} in kHz

**The formula given is for the typical characteristics only.

*** Minimum clock pulse width = 1.0 μs.

FIGURE 3 – PHONE DIALER SYSTEM TIMING DIAGRAM



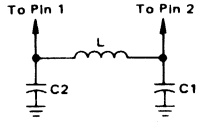
Notes:

(*) 1st, 2nd, 3rd, etc., denotes Strobe pulse sequence – i.e., which digit in the phone number is being dialed. The number in parentheses denotes the numerical value of the digit being dialed. The examples define the various voltage – level and timing requirements, not a complete phone number.

(**) For the MC14408 the DRO signal will remain high provided digits remain in the memory, or a digit for continuing outpulsing is strobed in before the anticipated falling edge of the most significant digit in the memory. (i.e., [200 % MB] ms after the most significant outpulsing edge). The time from Strobe to DRO can be 0 to 100 ms.

(***) For the HOL signal to hold a next digit (e.g. the 4th, etc.,) the HOL falling edge must not appear after [t_{ID}·%MB + 100] ms the last outpulsing edge of the previous digit.

FIGURE 4 – COMPONENT SELECTION FOR OSCILLATOR/CLOCK FREQUENCY



$f_{cl} = \frac{7.118}{\sqrt{LC}}$ where f_{cl} in kHz, L in mH,
C = C1 = C2 in μF

$\%f_{cl} = -0.5\,[\%C + \%L] \pm 3.0$ where $\%f_{cl}$, %C, %L are the frequency capacitor, and inductor tolerances in percent. The ±3.0% accounts for supply voltage and ambient temperature variations.

EXAMPLE

L	%L	C=C1=C2	%C	f_{cl}	$\%f_{cl}$	OUTPULSING RATE $f_{OPL} = f_{cl}/1.6$
5.0 mH	±5.0	0.04 μF	±5.0	≈16 kHz	±8.0	≈10 pps
5.0 mH	±5.0	0.01 μF	±5.0	≈32 kHz	±8.0	≈20 pps

3

FIGURE 5 – TRUTH TABLE

INPUTS							OUTPUTS	
$\overline{CRO}$	D4 D3 D2 D1	ST	$\overline{RED}$	$\overline{HOL}$	IDT	MBR	$\overline{OPL}$	DRO †
1	X X X X	X	X	X	X	X	0	0
0	X X X X	0	1	1	X	X	1 (Steady State)	0 (Steady State)
0	X X X X (nth Digit)	⊓	1	1	X	X	Number of pulses (1,) of nth digit = binary combination of D4, D3, D2, D1 *	1 During outpulsing 0 Otherwise
0	X X X X	0	⊓	1	X	X	Digits of number in memory re sent	1 During outpulsing 0 Otherwise
0	X X X X	X	1	0	X	X	1 { After conclusion of digit being outpulsed	0 { After conclusion of digit being outpulsed
X	X X X X	X	X	X	0 1	X	300 ms Interdigit time 800 ms Interdigit time } f_{cl} 16 kHz	
X	X X X X	X	X	X	X	0 1	61% (≈1.6 1) Make-Break Ratio 67% (≈2 1) Make-Break Ratio	

X = Don't Care

* With the exception of 0000 which will give 10 pulses.

† Refer to timing diagram Figure 3.

DEVICE OPERATION

OSCILLATOR (Osc, Pin 1)

This pin is an input to the internal oscillator and feedback connection for the L-C π-network. An external clock signal, if desired can be applied to Osc.

CLOCK (Clk, Pin 2)

This pin is an output from the internal oscillator and feedback connection for the L-C π-network and provides the system clock for the MC14419 bounce eliminator circuitry.

STROBE INPUT (ST, Pin 3)

This Strobe input, when high (ST = V_{DD}), signifies that the data at the D1, D2, D3, and D4 inputs is valid, and enters the 4-bit number into the internal FIFO (First-In, First-Out) memory for subsequent outpulsing. The first strobe pulse after a call is requested (CRQ = low) clears the memory of any previous number and enters the first digit of the new number. Successive strobe pulses will store up to a maximum of 16 digits in the internal FIFO memory, which ignores all digits entered in excess of that amount until a new call is requested.

DATA INPUTS (D4, D3, D2, D1, Pins 4, 5, 6, 7)

These pins are the Data inputs to the internal memory. A binary coded digit number entered will result in an equivalent number of pulses at the $\overline{OPL}$ (outpulsing) output, except for the code 0000, which will outpulse 10 pulses.

NEGATIVE POWER SUPPLY (V_{SS}, Pin 8)

This pin is the negative power supply connection. Normally this pin is system ground.

HOLD (HOL, Pin 9)

When taken low (HOL = V_{SS}), the Hold input disables the outpulsing at the completion of the digit being outpulsed. When taken high, outpulsing resumes. This feature can be used in multi-dial-tone phone systems to provide longer interdigit pauses when necessary.

RE-DIAL (RED, Pin 10)

The Re-Dial input, when taken low (RED = V_{SS}) automatically outpulses the digits entered into memory after the last time a call was requested.

OUTPULSING ($\overline{OPL}$, Pin 11)

The Outpulsing output sends out bursts of pulses equivalent to the digits of the telephone number stored in the memory. The duty cycle and interdigit time of the digit pulse bursts are controlled, respectively by the MBR (Pin 15) and IDT (Pin 14).

DIAL ROTATING OUTPUT (DRO, Pin 12)

The Dial Rotating (also known as "Off Normal") Output provides a signal which indicates that digit pulse bursts are being sent. In the MC14409, DRO goes high (V_{DD}) at the beginning of the first digit pulse burst and goes low (V_{SS}) between succeeding consecutive digit pulse bursts. In the MC14408, however, DRO goes high at the beginning of the first digit pulse burst and remains high until the last digit pulse burst of the telephone number has been sent (see Timing Diagram, Figure 3).

CALL REQUEST (CRQ, Pin 13)

The Call Request input when taken low (CRQ = V_{SS}) resets internal counters and prepares the internal logic to either accept new digit inputs to be dialed, or to re-dial (see RED, Pin 10) the digits stored in the memory.

INTERDIGIT TIME (IDT, Pin 14)

The Interdigit Timing input determines the length of time between consecutive digit pulse bursts. See the Interdigit Time (t_{ID}) in the switching characteristics for the length of time.

MAKE-BREAK RATIO (MBR, Pin 15)

The Make-to-Break Ratio input controls the duty cycle of the digit pulse bursts at the $\overline{OPL}$ output. For MBR = V_{DD}, duty cycle = 67% low, 33% high; and for MBR = V_{SS}, duty cycle = 61% low, 39% high.

POSITIVE POWER SUPPLY (V_{DD}, Pin 16)

This pin is the package positive power supply pin.

FIGURE 6 – KEYPAD TO PULSE DIALER FLOW DIAGRAM

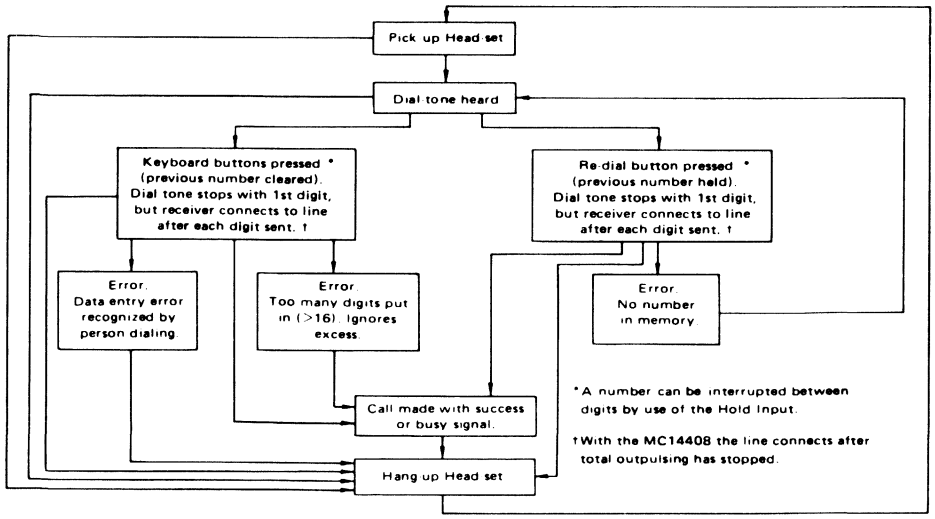


FIGURE 7 – PHONE DIALER SYSTEM

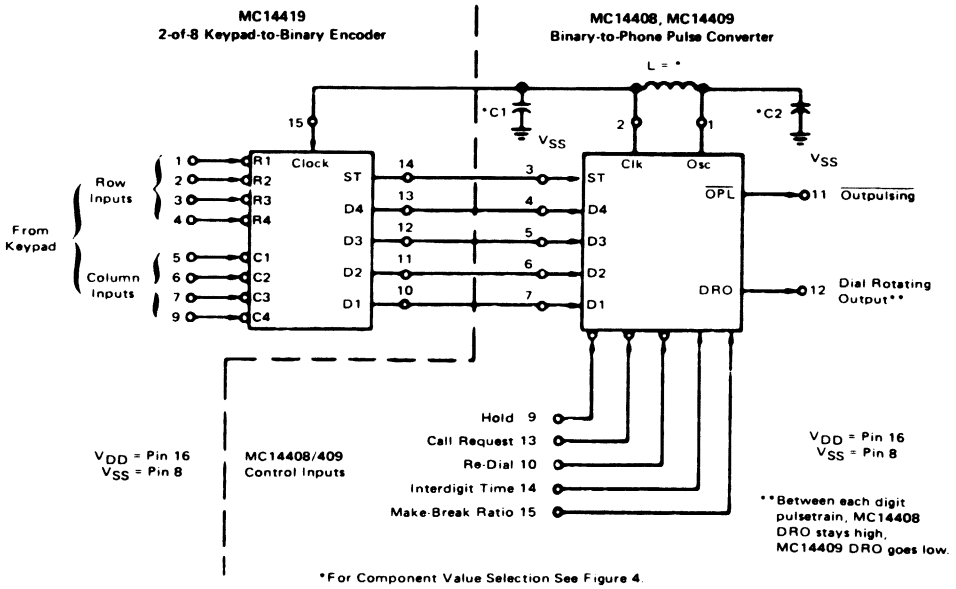


FIGURE 8 – STANDARD K-500 TELEPHONE

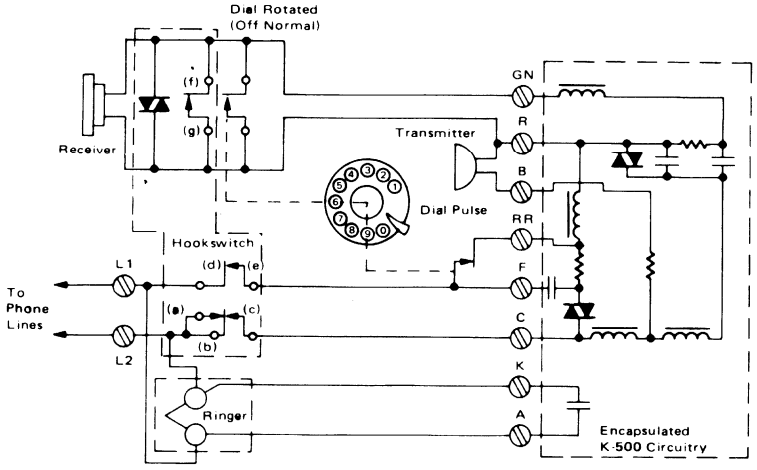
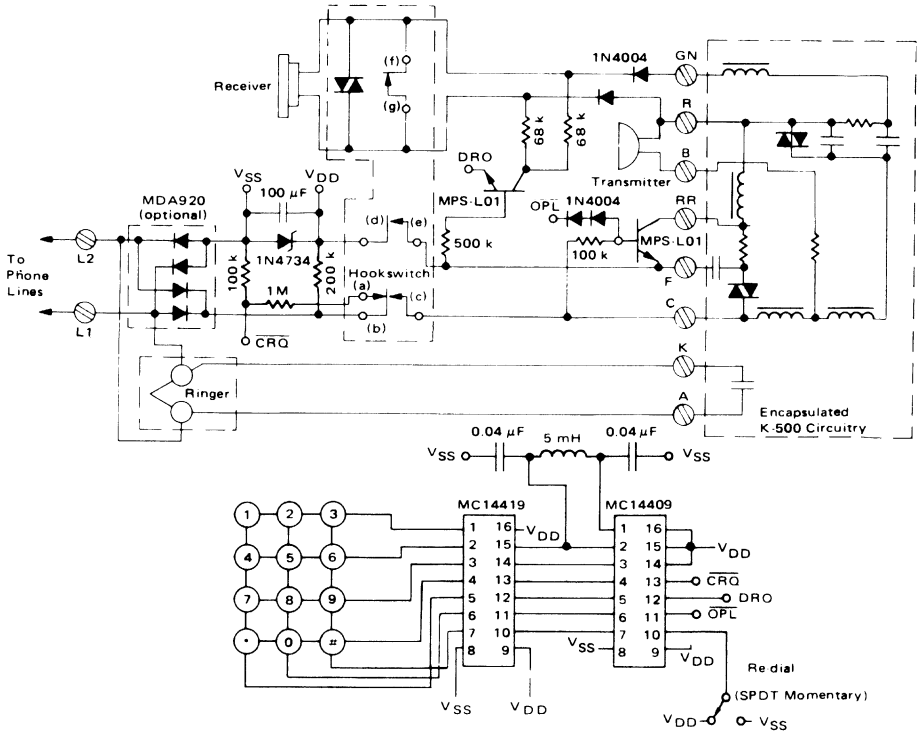


FIGURE 9 – MODIFIED K-500 TELEPHONE



MOTOROLA

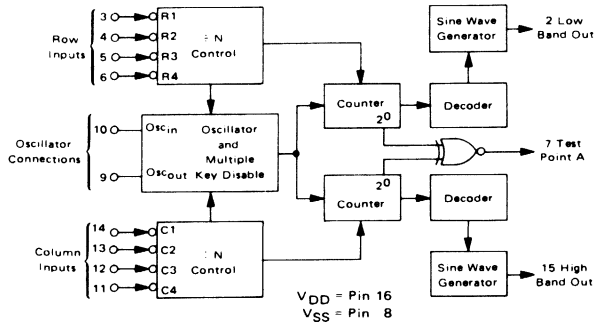
MC14410

2-OF-8 TONE ENCODER

The MC14410 2-of-8 tone encoder is constructed with complementary MOS enhancement mode devices. It is designed to accept digital inputs in a 2-of-8 code format and to digitally synthesize the high and low band sine waves specified by telephone tone dialing systems. The inputs are normally originated from a 4 x 4 matrix keypad, which generates 4 row and 4 column input signals in a 2-of-8 code format (1 row and 1 column are simultaneously connected to V_{SS}). The master clocking for the MC14410 is achieved from a crystal controlled oscillator which is included on the chip. Internal clocks, which operate the logic, are enabled only by one or more row and column signals being activated simultaneously. The two sine wave outputs have NPN bipolar structures on the same substrate which allows for low output impedance and large source currents. Applications of this device include telephone tone dialing, radio and mobile telephones, process control, point-of-sale terminals, and credit card verification terminals.

- Diode Protection on All Inputs
- Noise Immunity = 45% of V_{DD} Typical
- Supply Voltage Range = 4.4 Vdc to 6.0 Vdc
- On-Chip Oscillator (Crystal or External Clock Source may be applied to Pin 10)
- On-Chip Pull-Up Resistors on Row and Column Inputs
- Designed with Multiple Key Lockout (Eliminates Need for Mechanical Lockout in Keypad)
- Two Sine Wave Generators On-Chip
- Frequency Accuracy ±0.2%
- Low Harmonic Distortion
- Single Tone Capability
- Fast Oscillator Turn-On and Turn-Off Times

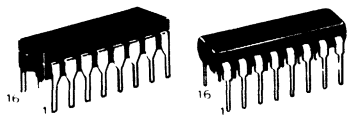
BLOCK DIAGRAM



CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

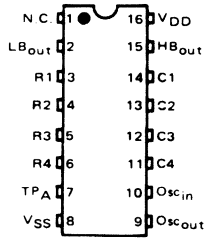
2-OF-8 TONE ENCODER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. A destructive high-current mode may occur if V_{in} and V_{out} are not constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Due to the sourcing capability of this circuit, damage can occur to the device if V_{DD} is applied, and the outputs are shorted to V_{SS} and are at a peak sinewave voltage.

DS9867

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +6.0	Vdc
Input Voltage, All Inputs	V_{in}	V_{SS} -0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	-40°C Min	-40°C Max	25°C Min	25°C Typ	25°C Max	+85°C Min	+85°C Max	Unit
Supply Voltage	V_{DD}	–	4.4	6.0	4.4	5.0	6.0	4.4	6.0	Vdc
Output Voltage "0" Level Pins 7 and 9	V_{out}	5.0	–	0.05		0	0.05	–	0.05	Vdc
"1" Level		5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
Input Voltage (V_O = 4.5 or 0.5 Vdc) "0" Level	V_{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
(V_O = 0.5 or 4.5 Vdc) "1" Level	V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source Pin 7	I_{OH}	5.0	-0.05	–	-0.05	-0.4	–	-0.04	–	mAdc
Pin 9			-0.23	–	-0.20	-1.7		-0.16	–	
(V_{OL} = 0.4 Vdc) Sink Pin 7	I_{OL}	5.0	0.05		0.05	0.20	–	0.04	–	mAdc
Pin 9			0.23	–	0.20	0.78	–	0.16	–	
Input Pull-Up Resistor Source Current (V_{in} = 0 Vdc) Pins 3-6, 11-14	I_{IL}	6.0	–	140	–	30	100	–	80	μAdc
Input Capacitance (V_{in} = 0 Vdc)	C_{in}	–	–		–	5.0	–	–	–	pF
Quiescent Current	I_Q	4.4		0.48		0.2	0.4	–	0.33	mAdc
		6.0		1.3	–	0.55	1.1	–	0.9	
Total Supply Current (Dynamic plus Quiescent)	I_T	4.4		1.7	–	0.7	1.4	–	1.15	mAdc
(R_L = 15 kΩ, f = 1 MHz)		6.0	–	3.5		1.45	2.9	–	2.4	
Low Band Output Voltage Swing Pin 2 Only (R_L = 100 k)	V_{Lpp}	4.4	400	600	500	600	700	550	750	mVpp
		6.0	800	1000	900	1000	1100	950	1150	
High Band Output Voltage Swing Pin 15 Only (R_L = 100 k)	V_{Hpp}	4.4	600	900	700	850	1000	800	1100	mVpp
		6.0	1000	1400	1100	1350	1500	1200	1600	
Low Band–High Band Voltage Differential	ΔV	5.0		–		2.5	–	–	–	dB
Low Band–High Band Pin 2,15 Output Impedance AC only	z_o	–	–	–	–	80	–	–	–	Ω
Low Band–High Band Pin 2,15 2nd thru 14th Harmonics (R_L = 15 kΩ)	V_{2H}-V_{14H}	4.4 to 6.0	–	-20	–	-30	-25	–	-25	dB
Maximum Clock Pulse Frequency	f_{cl}	4.4	–	–	–	1.0	–	1.1	–	MHz
Turn-on Time (Power on to oscillation)	t_{on}	5.0	–	–	–	8.0	–	–	–	ms

TABLE 1 – FUNCTIONAL TRUTH TABLE

ACTIVE LOW INPUTS		OUTPUTS	
Activated Row Lines	Activated Column Lines	Low Band Pin 2	High Band Pin 15
None	X**	dc level	dc level
X**	None	dc level	dc level
One	One	f_L*	f_H*
Two or more	One	dc level	f_H*
One	Two or more	f_L*	dc level
Two or more	Two or more	dc level	dc level

*See Table 2
**X = Don't care

TABLE 2 – OUTPUT FREQUENCY TABLE

Input Line Activated (low)	Frequency Generated**	
	f_L (Hz)	f_H (Hz)
R1	697	
R2	770	
R3	852	
R4	941	
C1		1209
C2		1336
C3		1477
C4		1633

**All frequencies are accurate to +0.2% (crystal tolerance not included).

FIGURE 1 – TYPICAL SINE WAVE OUTPUT
(Pins 2 or 15, No External Filtering)

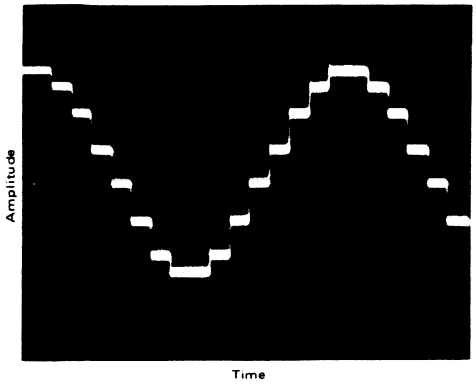


FIGURE 2 – TYPICAL FREQUENCY SPECTRUM
(Pins 2 or 15, No External Filtering)

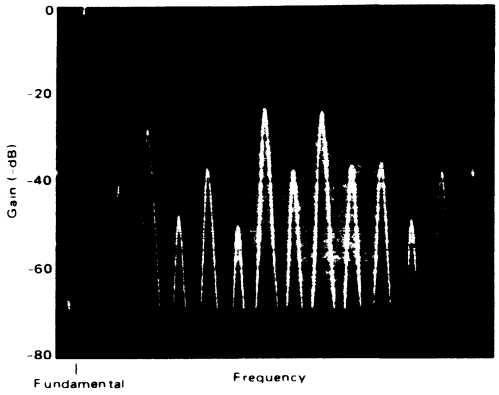


FIGURE 3 – TYPICAL CRYSTAL CIRCUIT

R_f = 15 MΩ ± 10%

CRYSTAL SPECIFICATION

Crystal Mode	Parallel
Frequency	1 MHz ± 0.1%
R_S	540Ω typ
C_0	7.0 pF typ
Temperature Range	-40°C to +85°C
Test Level	1 mW
Test Set	TS-330/TSM or Equivalent

*Recommended Crystals: CTS KNIGHT

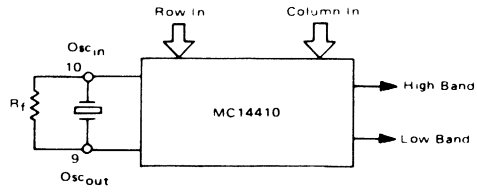


FIGURE 4 – TYPICAL TELEPHONE INTERFACE APPLICATION

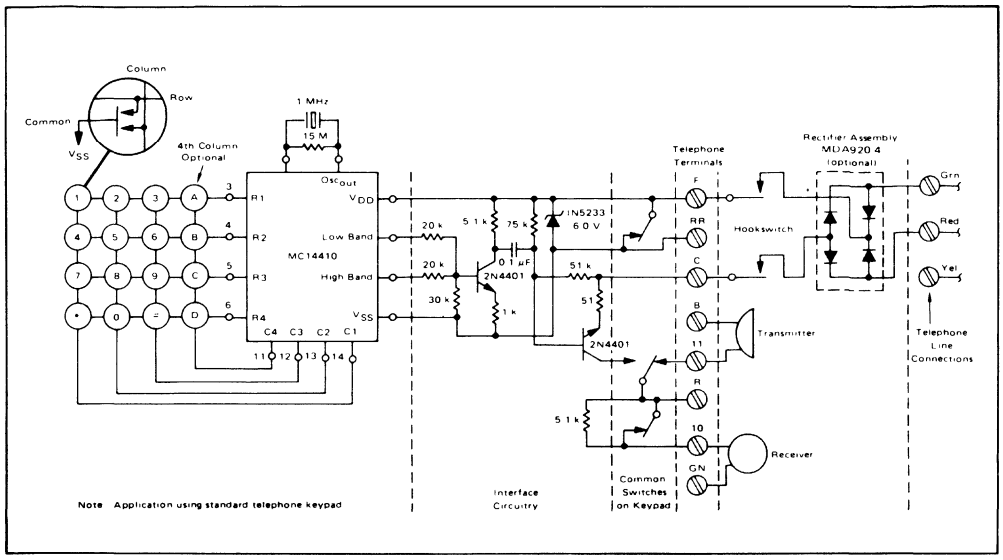


FIGURE 5 – LOW LEVEL OUTPUT TONE GENERATOR APPLICATION

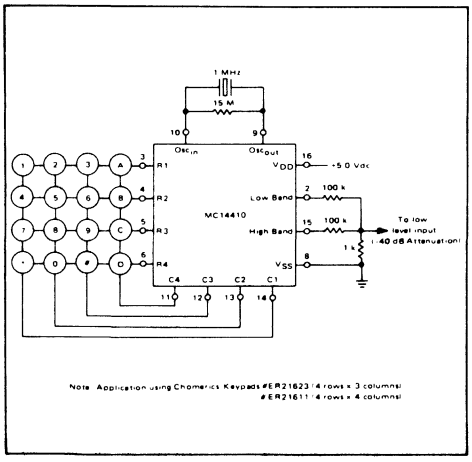
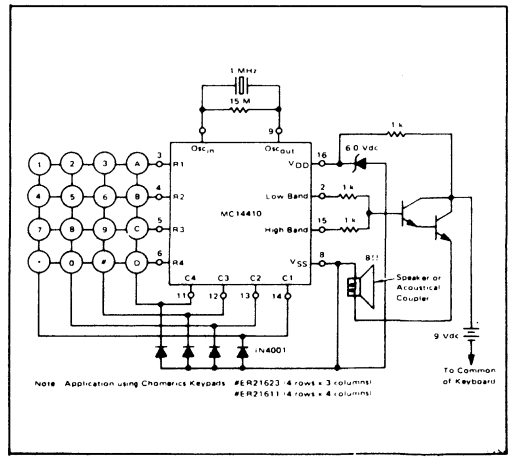


FIGURE 6 – BATTERY POWERED OPERATION (Driving Audio Speaker)



MOTOROLA

MC14411

BIT RATE GENERATOR

The MC14411 bit rate generator is constructed with complementary MOS enhancement mode devices. It utilizes a frequency divider network to provide a wide range of output frequencies.

A crystal controlled oscillator is the clock source for the network. A two-bit address is provided to select one of four multiple output clock rates.

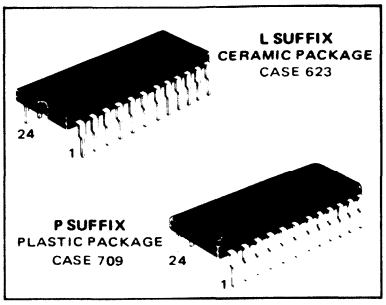
Applications include a selectable frequency source for equipment in the data communications market, such as teleprinters, printers, CRT terminals, and microprocessor systems.

- Single 5.0 Vdc (±5%) Power Supply
- Internal Oscillator Crystal Controlled for Stability (1.8432 MHz)
- Sixteen Different Output Clock Rates
- 50% Output Duty Cycle
- Programmable Time Bases for One of Four Multiple Output Rates
- Buffered Outputs Compatible with Low Power TTL
- Noise Immunity = 45% of V_{DD} Typical
- Diode Protection on All Inputs
- External Clock May be Applied to Pin 21
- Internal Pullup Resistor on Reset Input

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

BIT RATE GENERATOR

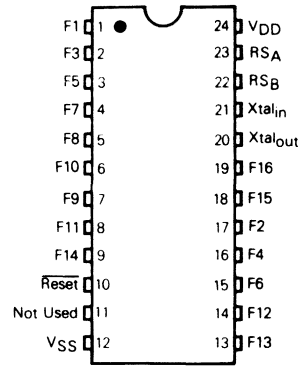


3

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 12.)

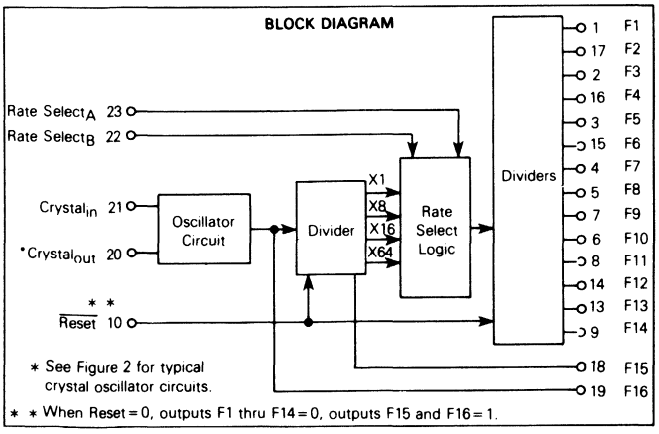
Rating	Symbol	Value	Unit
DC Supply Voltage Range	V_{DD}	5.25 to −0.5	V
Input Voltage, All Inputs	V_{in}	V_{DD} + 0.5 to V_{SS} − 0.5	V
DC Current Drain per Pin	I	10	mA
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

PIN ASSIGNMENT



V_{DD} = Pin 24
V_{SS} = Pin 12

BLOCK DIAGRAM



* See Figure 2 for typical crystal oscillator circuits.

* * When Reset = 0, outputs F1 thru F14 = 0, outputs F15 and F16 = 1.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

DS9386R2

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	−40°C Min	−40°C Max	25°C Min	25°C Typ	25°C Max	+85°C Min	+85°C Max	Unit
Supply Voltage	V_{DD}	–	4.75	5.25	4.75	5.0	5.25	4.75	5.25	V
Output Voltage "0" Level	V_{out}	5.0	–	0.05	–	0	0.05	–	0.05	V
"1" Level		5.0	4.95	–	4.95	5.0	–	4.95	–	V
Input Voltage (V_O = 4.5 or 0.5 V)	V_{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	V
(V_O = 0.5 or 4.5 Vdc)	V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	V
Output Drive Current (V_{OH} = 2.5 V) Source	I_{OH}	5.0	−0.23	–	−0.20	−1.7	–	−0.16	–	mA
(V_{OL} = 0.4 V) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mA
Input Current Pins 21, 22, 23	I_{in}	–	–	±0.1	–	±0.00001	±0.1	–	±1.0	μA
Pin 10		5.0	–	–	−1.5	–	−7.5	–	–	μA
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation	P_Q	5.0	–	2.5	–	0.015	2.5	–	15	mW
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	P_D = (7.5 mW/MHz) f + P_Q							mW
Output Rise Time** t_r = (3.0 ns/pF) C_L + 25 ns	t_{TLH}	5.0	–	–	–	70	200	–	–	ns
Output Fall Time** t_f = (1.5 ns/pF) C_L + 47 ns	t_{THL}	5.0	–	–	–	70	200	–	–	ns
Input Clock Frequency	f_{CL}	5.0	–	1.85	–	–	1.85	–	1.85	MHz
Clock Pulse Width	$t_{W(C)}$	–	200	–	200	–	–	200	–	ns
Reset Pulse Width	$t_{W(R)}$	–	500	–	500	–	–	500	–	ns

†For dissipation at different external capacitance (C_L) refer to corresponding formula:
$P_T(C_L) = P_D + 2.6 \times 10^{-3}(C_L - 15\ pF)\ V_{DD}^2 f$
where: P_T, P_D in mW, C_L in pF, V_{DD} in Vdc, and f in MHz.
**The formula given is for the typical characteristics only.

TABLE 1 — OUTPUT CLOCK RATES

Rate Select B	Rate Select A	Rate
0	0	X1
0	1	X8
1	0	X16
1	1	X64

Output Number	Output Rates (Hz) X64	X16	X8	X1
F1	614.4 k	153.6 k	76.8 k	9600
F2	460.8 k	115.2 k	57.6 k	7200
F3	307.2 k	76.8 k	38.4 k	4800
F4	230.4 k	57.6 k	28.8 k	3600
F5	153.6 k	38.4 k	19.2 k	2400
F6	115.2 k	28.8 k	14.4 k	1800
F7	76.8 k	19.2 k	9600	1200
F8	38.4 k	9600	4800	600
F9	19.2 k	4800	2400	300
F10	12.8 k	3200	1600	200
F11	9600	2400	1200	150
F12	8613.2	2153.3	1076.6	134.5
F13	7035.5	1758.8	879.4	109.9
F14	4800	1200	600	75
F15	921.6 k	921.6 k	921.6 k	921.6 k
F16*	1.843 M	1.843 M	1.843 M	1.843 M

*F16 is buffered oscillator output.

FIGURE 1 – DYNAMIC SIGNAL WAVEFORMS

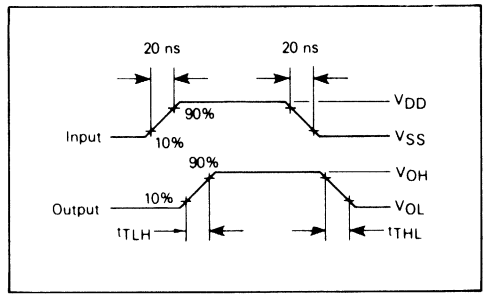
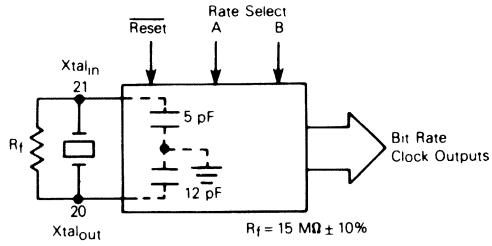


FIGURE 2 – TYPICAL CRYSTAL OSCILLATOR CIRCUIT



Crystal Specifications

Crystal Mode	Parallel
Frequency	1.8432 MHz ±0.05%@13 pF
R_S	540 Ω max
C_0	7.0 pF max
Temperature Range	0 to 70°C
Test Level	1 mW
Test Set	TS – 330/TSM or Equivalent

*Suggested Crystal Suppliers.
Tyco, CTS Knights

Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc., or others.

MOTOROLA

MC14412

CMOS LSI

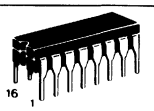
(LOW-POWER COMPLEMENTARY MOS)

UNIVERSAL LOW SPEED (0-600 bps) MODEM

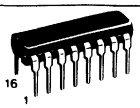
UNIVERSAL LOW SPEED MODEM (0-600 bps)

The MC14412 contains a complete FSK (Frequency-Shift Keying) modulator and demodulator compatible with both foreign (C.C.I.T.T. standards) and U.S.A. low speed (0 to 600 (bps) communication networks.

- On-Chip Crystal Oscillator with External Crystal
- Echo Suppressor Disable Tone Generator
- Originate and Answer Modes
- Simplex, Half-Duplex, and Full-Duplex Operation
- On-Chip Sine Wave Generator
- Modem Self Test Mode
- Single Supply:
  V_{DD} = 4.75 to 15 Vdc MC14412FP, MC14412 FL
  V_{DD} = 4.75 to 6.0 Vdc MC14412VP, MC14412VL
- Selectable Data Rates: 0-300, 0-600 bps
- Post Detection Filter
- TTL or CMOS Compatible Inputs and Outputs



L SUFFIX
CERAMIC PACKAGE
CASE 620



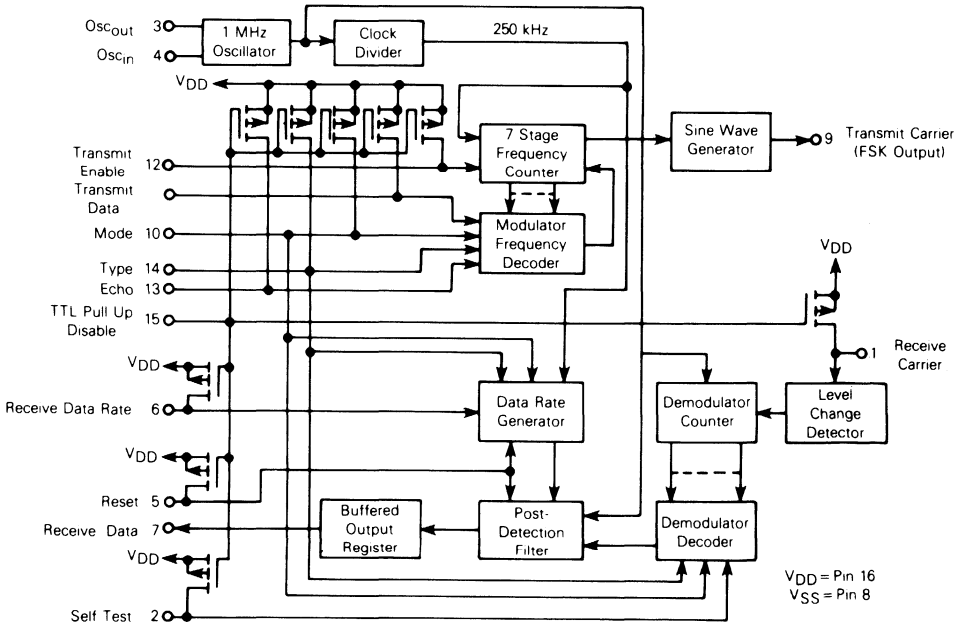
P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC144XX

Suffix	Denotes
L	Ceramic Package
P	Plastic Package
F	4.75 to 15 Vdc
V	4.75 to 6.0 Vdc

BLOCK DIAGRAM



DS9411R1

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}** Vdc	−40°C Min	−40°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit
Output Voltage Pin 7 Only		5.0	–	0.05	–	0	0.05	–	0.05	
"0" Level	V_{OL}	10	–	0.05	–	0	0.05	–	0.05	V
$V_{in} = V_{DD}$ or 0		15	–	0.05	–	0	0.05	–	0.05	
"1" Level		5.0	4.95	–	4.95	5.0	–	4.95	–	
$V_{in} = 0$ or V_{DD}	V_{OH}	10	9.95	–	9.95	10	–	9.95	–	V
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage*										
"0" Level										
(V_O = 4.5 or 0.5 V)	V_{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	V
(V_O = 9.0 or 1.0 V)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 V)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level										
Pin 15		5 to 15	V_{DD} − 0.75	–	V_{DD} − 0.8	V_{DD} − 2	–	V_{DD} − 0.85	–	
(V_O = 0.5 or 4.5 V)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 V)	V_{IH}	10	7.0	–	7.0	5.50	–	7.0	–	V
(V_O = 1.5 or 13.5 V)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current										
Pin 7 Only										
(V_{OH} = 2.5)	I_{OH}	5	−0.62	–	−0.5	−1.5	–	−0.35	–	mA
(V_{OH} = 9.5)		10	−0.62	–	−0.5	−1.0	–	−0.35	–	
(V_{OH} = 13.5)		15	−1.8	–	−1.5	−3.6	–	−1.1	–	
(V_{OL} = 0.4)		4.75	2.3	–	2.0	4.0	–	1.6	–	
(V_{OL} = 0.5)	I_{OL}	10	5.3	–	4.5	10	–	3.6	–	mA
(V_{OL} = 1.5)		15	15	–	13	35	–	10	–	
Input Current (Pin 15 = V_{DD})	I_{in}	–	–	–	–	±0.00001	±0.1	–	–	µA
Input Pull-Up Resistor Source Current (Pin 15 = V_{SS}, V_{in} = 2.4 Vdc) Pins 1, 2, 5, 6, 10, 11 12, 13, 14	I_P	5	285	–	250	460	–	205	–	µA
Input Capacitance	C_{in}	–	–	–	–	5.0	–	–	–	pF
Total Supply Current		5	–	4.5	–	1.1	4.0	–	3.5	
(Pin 15 = V_{DD})	I_T	10	–	13	–	4.0	12	–	11	mA
		15	–	27	–	8.0	25	–	23	
Modulator/Demodulator Frequency Accuracy (Excluding Crystal)	ACC	5 to 15	–	–	–	0.5	–	–	–	%
Transmit Carrier Output		5	–	–	−20	−25	–	–	–	
2nd Harmonic	V_{2H}	15	–	–	−25	−32	–	–	–	dB
Transmit Carrier Output		5	–	–	0.2	0.30	–	–	–	
Voltage (R_L = 100 kΩ)	V_{out}	10	–	–	0.5	0.85	–	–	–	V_{RMS}
(Pin 9)		15	–	–	1.0	1.5	–	–	–	
Maximum Receive		5	–	15	–	–	15	–	15	
Carrier Rise and Fall	t_r, t_f	10	–	5.0	–	–	5.0	–	5.0	µs
Times (Pin 1)		15	–	4.0	–	–	4.0	–	4.0	
Maximum Oscillator Frequency	f_{max}	5	–	–	1.2	5	–	–	–	MHz
Minimum Clock Pulse Width	t_w	5	–	–	–	50	350	–	–	ns

*DC Noise Immunity (V_{IL}, V_{IH}) is defined as the maximum voltage change from an ideal "0" or "1" input level, that the circuit will withstand before accepting an erroneous input.

**Note: Only 5-Volt specifications apply to MC14412VP devices.

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

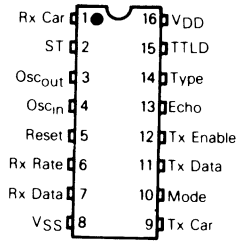
Rating	Symbol	Value	Unit
DC Supply Voltages MC14412FP, FL MC14412VP, VL	V_{DD}	−0.5 to 15 −0.5 to 6.0	V
Input Voltages, All Inputs	V_{in}	V_{DD} + 0.5 to V_{SS} − 0.5	V
DC Current Drain per Pin (except Pin 8, 7)	I	10	mA
DC Current Drain (Pin 8, 7)	I	35	mA
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

3

PIN ASSIGNMENT



DEVICE OPERATION

GENERAL

Figure 1 shows the modem in a system application. The data to be transmitted is presented in serial format to the modulator for conversion to FSK signals for transmission over the telephone network. The modulator output is buffered/amplified before driving the 600 ohm telephone line.

The FSK signal from the remote modem is received via the telephone line and filtered to remove extraneous signals such as the local Transmit Carrier. This filtering can be either a bandpass which passes only the desired band of frequencies or a notch which rejects the known interfering signal. The desired signal is then limited to preserve the axis crossings and fed to the demodulator where the data is recovered from the received FSK carrier.

INPUT/OUTPUT FUNCTIONS

Figure 2 shows the I/O interface for the MC14412 low-speed modem. The following is a description of each individual signal.

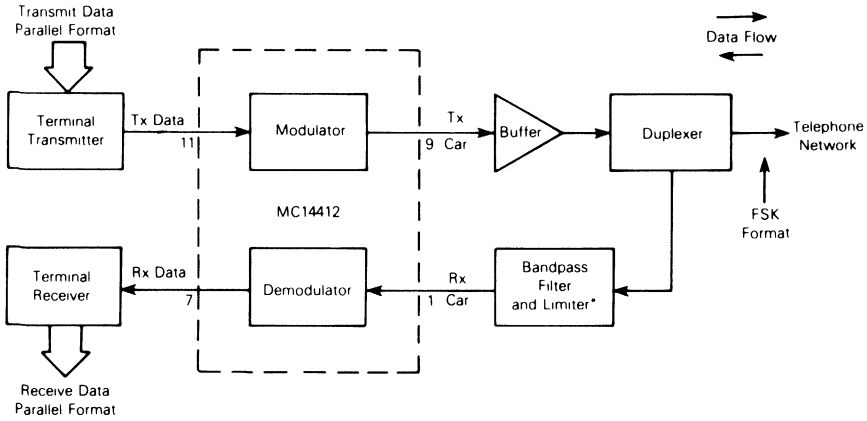
TYPE (Pin 14)

The Type input selects either the U.S. or C.C.I.T.T. operational frequencies for both transmitting and receiving data. When the Type input = "1", the U.S. standard is selected and when the Type input = "0", the C.C.I.T.T. standard is selected.

TRANSMIT DATA (Tx Data, Pin 11)

Transmit Data is the binary information input. Data entered for transmission is modulated using FSK techniques. When operating in the U.S. standard (Type = "1") a logic "1" input level represents a Mark or when operating in the CCITT standard (Type = "0") a logic "1" input level represents a Mark.

FIGURE 1 – TYPICAL LOW-SPEED MODEM APPLICATION



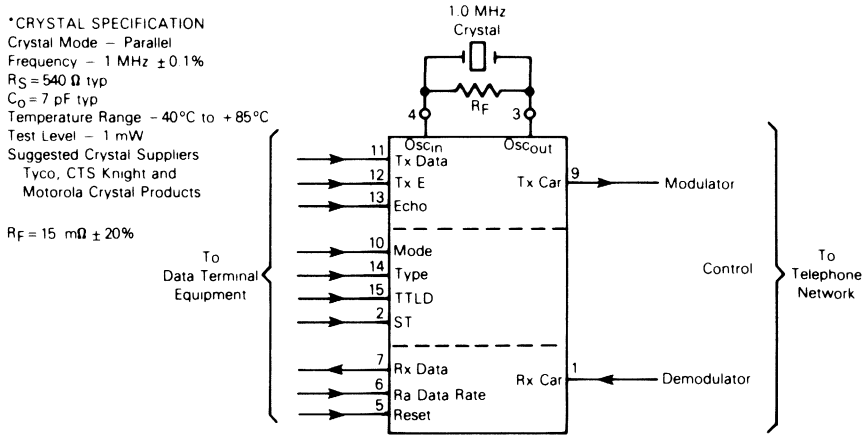
Since the modulator and demodulator sections of the MC14412 are functionally equivalent to those of the MC6860, additional application information can be obtained from the following Motorola publications

AN-731 Low-speed Modem Fundamentals

AN-747 Low-speed Modem System Design Using the MC6860

EB-49 Application Performance of the MC6860 MODEM.

FIGURE 2 – MC14412 INPUT/OUTPUT SIGNALS



TRANSMIT CARRIER (Tx Car, Pin 9)

The Transmit Carrier is a digital-synthesized sine wave derived from a 1.0 MHz oscillator reference. The Tx CAR has an AC output impedance of 5 kΩ typical. The frequency characteristics are as follows:

United States Standard
Type = "1"
Echo = "0"

Mode		Tx Data		Tx Car
Originate	"1"	Mark	"1"	1270 Hz
Originate	"1"	Space	"0"	1070 Hz
Answer	"0"	Mark	"1"	2225 Hz
Answer	"0"	Space	"0"	2025 Hz

C.C.I.T.T. Standard
Type = "0"
Echo = "0"

Mode		Tx Data		Tx Car
Channel	"1"	Mark	"1"	980 Hz
No. 1	"1"	Space	"0"	1180 Hz
Channel	"0"	Mark	"1"	1650 Hz
No. 2	"0"	Space	"0"	1850 Hz

Echo Suppressor Disable Tone
Type = "0"
Echo = "1"

Mode	Tx Data	Tx Car
Chan. No. 2 "0"	"1"	2100 Hz

TRANSMIT ENABLE (Tx Enable, Pin 12)

The Transmit Carrier output is enabled when the Tx Enable input = "1". No output tone can be transmitted when Tx Enable = "0".

MODE (Pin 10)

The Mode input selects the pair of transmitting and receive frequencies used during modulation and demodulation. When Mode = "1", the U.S. originate mode is selected (Type input = "1") or the C.C.I.T.T. Channel No. 1 (Type input = "0"). When mode = "0", the U.S. answer mode is selected (Type input = "1") or the C.C.I.T.T. Channel No. 2 (Type input = "0").

ECHO (Pin 13)

When the Echo input = "1" (Type = "0", Mode = "0", Tx Data = "1") the modulator will transmit a 2100 Hz tone for disabling line echo suppressors. During normal data transmission, this input should be low = "0".

RECEIVE DATA (Rx Data, Pin 7)

The Receive Data output is the digital data resulting from demodulating the Receive Carrier.

RECEIVE CARRIER (Rx Car, Pin 1)

The Receive Carrier is the FSK input to the demodulator. This input must have either a CMOS or TTL compatible logic level input (see TTL pull-up disable) at a duty cycle of 50% ± 2%, that is a square wave resulting from a signal limiter.

RECEIVE DATA RATE (Rx Rate, Pin 6)

The demodulator has been optimized for signal to noise performance at 300, and 600 bps.

Data Rate	Rx Rate
0-300 bps	"1"
0-600 bps	"0"

SELF TEST (ST, Pin 2)

When a high level (ST = "1") is placed on this input, the demodulator is switched to the modulator frequency and demodulates the transmitted FSK signal.

RESET (Pin 5)

This input is provided to decrease the test time of the chip. In normal operation, this input may be used to disable the demodulator (Reset = "1") – otherwise it should be tied low = "0". The reset pin does not reset Rx data pin 7.

CRYSTAL (Osc_{in}, Osc_{out}, Pin 4, Pin 3, respectively)

A 1.0 MHz crystal is required to utilize the on chip oscillator. A 1.0 MHz square wave clock can also be applied to the Osc_{in} input to satisfy the clock requirement (see Figure 2).

When utilizing the 1.0 MHz crystal, external parasitic capacitance, including crystal shunt capacitance, must be < 9 pF at the crystal input (pin 4). Pin 4 is capable of driving only one CMOS input.

TTL PULL-UP DISABLE (TTLD, Pin 15)

To improve TTL interface compatibility, all of the inputs to the MODEM have controllable P-Channel devices which act as pull-up resistors when TTLD input is low ("0"). When the input is taken high ("1") the pull-up is disabled, thus reducing power dissipation when interfacing with CMOS. Pin 15 should be taken high ("1") with V_{DD} greater than 6 volts.

FIGURE 3 – M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM

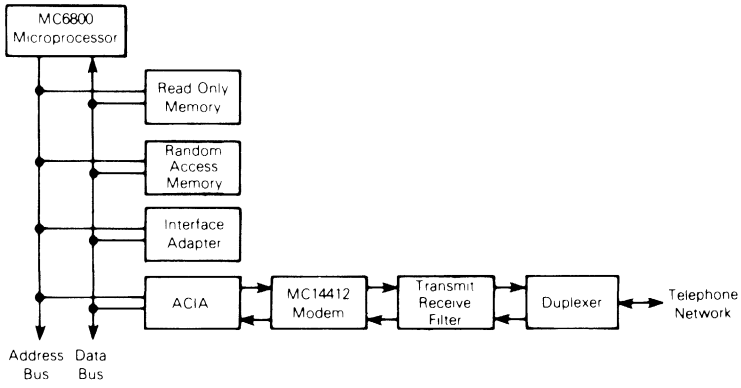


FIGURE 4 – TRANSMIT CARRIER SINEWAVE

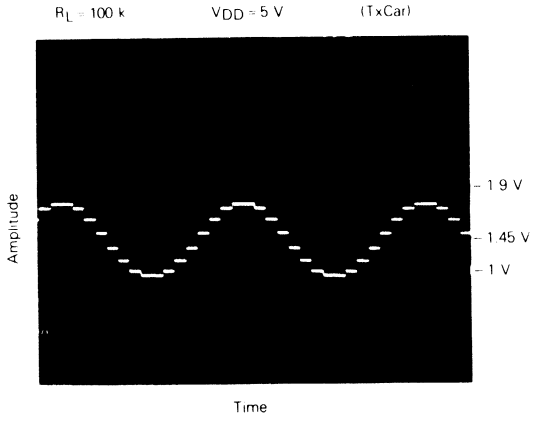
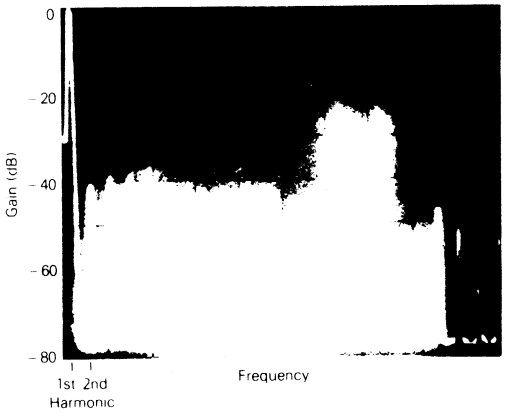


FIGURE 5 – TYPICAL TRANSMIT CARRIER FREQUENCY SPECTRUM



MOTOROLA

MC14413-1
MC14413-2
MC14414-1
MC14414-2

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

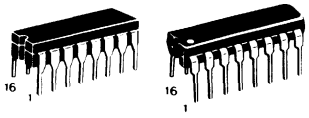
PULSE CODE MODULATION SAMPLED DATA FILTERS

3

PULSE CODE MODULATION SAMPLED DATA FILTERS

The MC14413-1, -2 and MC14414-1, -2 are sampled data, switched capacitor filter ICs intended to provide the band limiting and signal restoration filtering necessary in PCM Codec voice digitization systems. Both ICs are capable of operating from either a single or split power supply and can be powered-down when not in use. Included on both chips are two totally uncommitted op amps for use elsewhere in the systems as I to V converters, gain adjust buffers, etc.

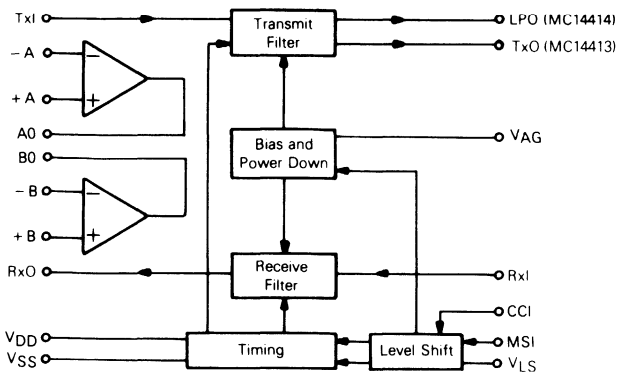
- Transmit Band-pass and Receive Low-pass (MC14413-1, -2)
- Transmit and Receive Low-pass (MC14414-1, -2)
- D3/D4 Specifications (MC14414-2/13-2)
- CCITT Specification (MC14414-1/13-1)
- Low Operating Power Consumption — 30 mW (Typical)
- Power Down Capability — 1 mW (Maximum)
- Single Supply Capability when Used with MC14404/6/7 Codecs
- ±5 to ±8 Volt Power Supply Ranges
- Receive Filter Compatible with 15% to 100% Duty Cycle PAM Inputs with Sinx/x Correction
- No Precision Components Required (MC14413-1, -2)
- TTL Compatible Inputs Using V_{LS} Pin
- Two Operational Amplifiers Available to Reduce System Component Count



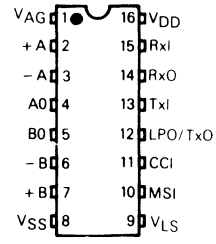
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

BLOCK DIAGRAM



PIN ASSIGNMENT



DS9833R2

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}-V_{SS}	−0.5 to 18	V
Input Voltage, All Pins	V_{in}	−0.5 to V_{DD} +0.5	V
DC Current Drain per Pin (Excluding V_{DD}, V_{SS})	I	10	mA
Operating Temperature Range	T_A	−40 to 85	°C
Storage Temperature Range	T_{stg}	−65 to 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}-V_{SS}	10	12	16	V
Convert Clock Frequency	CCI	50	128	400	kHz
Master Sync Frequency	MSI	–	8	32	kHz

DIGITAL ELECTRICAL CHARACTERISTICS (V_{SS} = 0 V)

Characteristic		Symbol	V_{DD} Vdc	0°C Min	0°C Max	25°C Min	25°C Typ	25°C Max	85°C Min	85°C Max	Unit
Operating Current		I_{DD}	12	–	5.0	–	2.0	4.3	–	5.0	mA
Power-Down Current (PDI = V_{SS})		I_{PD}	12	–	50	–	10	40	–	50	μA
Input Capacitance		C_{in}	12	–	–	–	5.0	7.5	–	–	pF
MODE CONTROL LOGIC LEVELS											
V_{LS} Power-Down Mode		V_{IH}	12 15	11.5 14.5	– –	11 14	11 13	– –	11.5 14.5	– –	V
V_{LS} TTL Mode		–	12 15	2 2	9.0 11.0	2.0 2.0	– –	9 12.0	2 2	9.0 11.0	V
V_{LS} CMOS Mode		V_{IL}	12 15	– –	0.8 0.8	– –	– –	0.8 0.8	– –	0.8 0.8	V
V_{AG} Power-Down Mode		V_{IH}	12 15	11.5 14.5	– –	11.5 14.5	10.5 13.5	– –	11.5 14.5	– –	V
V_{AG} Analog-Ground Mode		V_{IL}	12 15	– –	9.0 12.0	– –	– –	9.0 12.0	– –	9.0 12.0	V
CMOS LOGIC LEVELS ($V_{LS} = V_{SS}$)											
Input Current CCI		I_{in}	12	–	±1.0	–	±0.00001	±0.3	–	±1.0	μA
Input Current MSI (Internal Pulldown Resistors)	"1" Level "0" Level	I_{in}	12 12	– –	200 −1.0	– –	50 −0.00001	100 −0.3	– –	200 −1.0	μA
Input Voltage CCI, MSI	"0" Level	V_{IL}	12 15	– –	– –	– –	5.25 6.75	3.60 4.0	– –	– –	V
	"1" Level	V_{IH}	12 15	– –	– –	9.0 11.5	6.75 8.25	– –	– –	– –	V
TTL LOGIC LEVELS (V_{LS} = 6 V, V_{SS} = 0 V)											
Input Current CCI		I_{in}	12	–	±1.0	–	±0.00001	±0.3	–	±1.0	μA
Input Current MSI (Internal Pulldown Resistor)	"1" Level "0" Level	I_{in}	12 12	– –	200 −1.0	– –	30 −0.00001	– −0.3	– –	200 −1.0	μA
Input Voltage CCI, MSI	"0" Level "1" Level	V_{IL} V_{IH}	12 12	– –	– –	– V_{LS} + 2.0	– –	V_{LS} + 0.8 –	– –	– –	V

ANALOG ELECTRICAL CHARACTERISTICS (V_{DD} = 12 V)

Characteristic		Symbol	0°C		25°C			85°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Input Current	V_{AG}	I_{in}	–	±30	–	–	±10	–	±30	μA
Input Current	RxI, TxI	I_{in}	–	–	–	±0.00001	±1.0	–	±1.0	μA
AC Input Impedance (1 kHz)	RxI, TxI	Z_{in}	1.0	–	1.0	2.0	–	1.0	–	MΩ
Input Common Mode Voltage Range	TxI, RxI	V_{ICR}	–	–	1.5	–	10.5	–	–	V
Output Voltage Range	TxO, LPO, RxO									
(R_L = 20 kΩ to V_{AG})		V_{OR}	1.5	10.5	1.5	–	10.5	1.5	10.5	V
(R_L = 600 Ω to V_{AG})			2.0	9.3	2.0	–	9.3	2.0	9.3	
(R_L = 900 Ω to V_{AG})			1.5	10.5	1.5	–	10.5	1.5	10.5	
Small Signal Output Impedance (1 kHz)	TxO (MC14413)		–	–	–	50	–	–	–	
	LPO (MC14414)	Z_O	–	–	–	50	–	–	–	Ω
	RxO		–	–	–	50	–	–	–	
Output Current										
(V_O = 11 V)	TxO, LPO, RxO	I_{OH}	–5	–	–5	–6.0	–	–5	–	mA
(V_O = 1 V)	TxO, LPO, RxO	I_{OL}	5	–	5	7	–	5	–	

OP AMP PERFORMANCE ($V_{DD} - V_{SS}$ = 12 V)

Characteristic		0°C		25°C			85°C		Unit
		Min	Max	Min	Typ	Max	Min	Max	
Input Offset Voltage		–	±80	–	–	±70	–	±80	mV
Open Loop Gain	Z_L = 600 Ω + 200 pF to V_{AG}	–	–	–	45	–	–	–	dB
Input Bias Current		–	–	–	±0.1	–	–	–	μA
Output Voltage Range									
(R_L = 20 kΩ to V_{AG})		–	–	1.5	–	10.5	–	–	V
(R_L = 600 Ω to V_{AG})		–	–	2.0	–	9.3	–	–	
(R_L = 900 Ω to V_{AG})		–	–	1.5	–	10.5	–	–	
Output Current	V_{OH} 10.5	–	5.1	–	7.0	–	–	5.1	mA
	V_{OL} 0.5	–	–5.1	–	–7.0	–	–	–5.1	
Output Noise		–	0	–	–3	–	–	0	dBrnc0
Slew Rate		–	–	–	2	–	–	–	V/μs

RECEIVE FILTER SPECIFICATIONS

($V_{DD} - V_{SS}$ = 12 V, CCI = 128 kHz, MSI = 8 kHz, includes sinx/x correction, V_{in} = –10 dBm0, full scale = +3 dBm0, 7 V p-p)

Characteristic		0°C		25°C			85°C		Unit
		Min	Max	Min	Typ	Max	Min	Max	
Gain (1020 Hz)		–0.3	0.30	–	±0.2	–	–0.30	0.30	dB
Pass-band Ripple (50 Hz to 3000 Hz)	Relative to 1.02 kHz@0 dBm0	–0.15	+0.15	–	±0.08	–	–0.15	+0.15	dB
Out of Band Rejection Relative to 1.02 kHz@0 dBm0	MC14414/13-1	–	–0.9	–	–0.5	–0.9	–	–0.9	
3400 Hz	MC14414/13-2	–	–1.5	–	–0.8	–1.5	–	–1.5	dB
4000 Hz-4600 Hz		–14	–	–14.2	–15.5	–	–14	–	
4600 Hz-64 kHz		–28	–	–30	–33	–	–28	–	
Output Noise (RXI = V_{AG})	ref to 900 Ω	–	–	–	8	12	–	–	dBrnc0
Dynamic Range		–	–	81	83	–	–	–	dB
Absolute Delay Difference									
1150 to 2300 kHz Delay		–	22	–	12	22	–	22	μs
1000 to 2500 kHz Delay		–	35	–	25	35	–	35	
800 to 2700 kHz Delay		–	41	–	31	41	–	41	
Crosstalk 0 dBm@3 kHz		–	–	–	76	–	–	–	dB
Power Supply Rejection Ratio V_{DD} = 12 V + 0.1 Vrms@1 kHz		–	–	–	40	–	–	–	dB

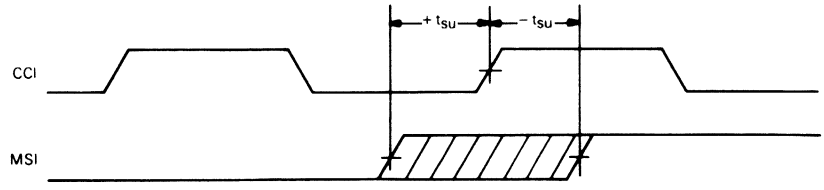
TRANSMIT FILTER SPECIFICATIONS ($V_{DD} - V_{SS}$ = 12 V, CC = 128 kHz, MSI = 8 kHz, V_{in} = − 10 dBm0, full scale = + 3 dBm0, 7 Vp-p)

Characteristic		0°C		25°C			85°C		Unit
		Min	Max	Min	Typ	Max	Min	Max	
Gain (1020 Hz)	MC14413-1, -2	− 0.3	+ 0.3	–	± 0.2	–	− 0.3	+ 0.3	dB
	MC14414-1, -2	− 0.25	0.25	–	± 0.15	–	− 0.25	0.25	
Pass-band Ripple (300 Hz to 3000 Hz)	Relative to 1.02 kHz@0 dBm0	− 0.15	0.15	–	± 0.08	–	− 0.15	0.15	dB
Rejection									dB
50 Hz (Relative to 1.02 kHz)	MC14413-1, -2 Only	− 24	–	− 26	− 28	–	− 24	–	
60 Hz	MC14413-1, -2 Only	− 22	–	− 22.7	− 25	–	− 22	–	
180 Hz		–	− 0.8	–	− 0.3	–	–	− 0.8	
3400 Hz	MC14414-1/13-1	–	− 0.8	–	− 0.5	− 0.8	–	− 0.8	
	MC14414-2/13-2	–	− 1.5	–	− 0.6	− 1.5	–	− 1.5	
4000 Hz-4600 Hz		− 14	–	− 14	− 15.5	–	− 14	–	
4600 Hz-64 kHz		− 32	–	− 32	− 33	–	− 32	–	
Output Noise (300 Hz-3400 Hz)	MC14413-1, -2	–	15	–	10	15	–	15	dBrnc0
	MC14414-1, -2	–	12	–	7	10	–	12	
Dynamic Range (7 V p-p Max)	MC14413-1, -2	–	–	78	84	–	–	–	dB
	MC14414-1, -2	–	–	81	87	–	–	–	
Absolute Delay Difference									µs
1150 to 2300 kHz Delay		–	22	–	12	22	–	22	
1000 to 2500 kHz Delay		–	35	–	25	35	–	35	
800 to 2700 kHz Delay		–	41	–	31	41	–	41	
Crosstalk	0 dBm@3 kHz RXO, TXO	–	–	–	76	–	–	–	dB
Power Supply Rejection Ratio	V_{DD} = 12 V + 0.1 V_{RMS}@1 kHz	–	–	–	40	–	–	–	dB

SWITCHING CHARACTERISTICS ($V_{DD} - V_{SS}$ = 10 V)

Characteristics		Symbol	0 to 70°C			Units
			Min	Typ	Max	
Input Rise Time Input Fall Time	CCI, MSI	t_{TLH} t_{THL}	–	–	4	µs
Pulse Width	CCI, MXI	t_{WH}	200	–	–	ns
Clock Pulse Frequency	CCI	f_{CL}	50	–	500	kHz
CCI Duty Cycle		–	40	–	60	%
Setup Time MSI Rising Edge to CCI Rising Edge (CCI = 128 kHz)*		t_{su}	− 3.0	–	+ 3.0	µs

*Specifications assume use of 50% duty cycle for clocks.



FUNCTIONAL DESCRIPTION OF PINS

Pin 1 — V_{AG} (Analog Ground)

This pin should be held at approximately (V_{DD}-V_{EE})/2. All analog inputs and outpus are referenced to this pin. If this pin is brought to within approximately 1.0 V of V_{DD}, the chip will be powered down.

Pin 2 — +A

Noninverting input of op-amp A.

Pin 3 — −A

Inverting input of op-amp A.

Pin 4 — A0

Output of uncommitted op-amp A.

Pin 5 — B0

Output of uncommitted op-amp B.

Pin 6 — −B

Inverting input of op-amp B.

Pin 7 — +B

Non-inverting input of op-amp B.

Pin 8 — V_{SS}

This is the most negative supply pin and digital ground for the package.

Pin 9 — V_{LS} (Logic Shift Voltage)

The voltage on this pin determines the logic compatibility for the CCI and MSI inputs. If V_{LS} is within 0.8 V of V_{SS}, the thresholds will be for CMOS operating between V_{DD} and V_{SS}. If V_{LS} is within 1.0 V of V_{DD}, the chip will power down. If V_{LS} is between $V_{DD}-2$ V and $V_{SS}+2$ V, the thresholds for logic inputs at CCI and MSI will be between $V_{LS}+0.8$ V and $V_{LS}+2.0$ V for TTL compatibility.

Pin 10 — MSI (Master Sync Input)

This pin should receive a low-to-high transition concurrent with each new PAM sample received at the receive filter input, ADI. A new transmit filter output sample will be presented 8 CCI clocks after this.

Pin 11 — CCI (Convert Clock Input)

Normally, a 128 kHz clock signal should be applied to this pin to operate both filters at fo = 3100 Hz. For other break frequencies use the following equation: fo = 0.02422 f clock.

Pin 12 — TxO (Transmit Band-pass Output — MC14413-1, -2)

This is the output of the transmit band-pass filter. It is 100% duty cycle PAM at 8 kHz.

Pin 12 — LPO (Transmit Low-pass Output — MC14414-1, -2)

This is the output of the transmit low-pass filter. It is 100% duty cycle PAM at CCI frequency, normally 128 kHz.

Pin 13 — TxI (Transmit Input)

This is the transmit-filter input.

Pin 14 — RxO (Receive Output)

This pin is the output of the receive filter. It is 100% duty cycle PAM at the same frequency as the CCI pin, normally 128 kHz.

Pin 15 — RxI (Receive Input)

This is the receive filter input. It will accept 15% to 100% duty cycle PAM at 8 kHz.

Pin 16 — V_{DD}

Nominally 12 volts.

NOTE: Both V_{AG} and V_{LS} are high-impedance inputs.

PCM FILTER DESCRIPTION

Transmit Filter Description

The transmit filter in both the MC14413-1, -2 and MC14414-1, -2 consists of a 5-pole elliptic low-pass section operating at a sampling rate of 128 kHz. This filter provides the band limiting necessary to prevent aliasing of the input signal in the codec. Since the transmit filter itself samples at a 128 kHz rate, its input (TxI) signal should be band limited to 124 kHz. If energy above 124 kHz could be present, a single-pole RC pre-filter should precede the transmit filter.

In addition to the low-pass section, the transmit filter of the MC14413-1, -2 incorporates a 3 pole Chebychev high-pass filter to provide 50/60 Hz and 15 Hz rejection. Although the MC14414-1, -2 does not include this filter, it can be externally realized using one of the on-board uncommitted op amps as an active filter. This is shown in Figure 9.

Both the MC14413-1, -2 and MC14414-1, -2 can be used in cascade to produce a sharper rolloff. This is especially useful in testing the MC14413-1, -2 since the 8 kHz PAM from the Tx filter will be sampled and sinx/x corrected by applying the Tx output to the RxI input and observing RxO.

Receive Filter Description

The receive filter sections of the MC14413-1, -2 and MC14414-1, -2 are identical and are 5-pole elliptic low-pass filters operating at a sampling rate of 128 kHz. These filters are used to smooth the PAM output of the PCM Codec. They are similar to the transmit low-pass sections with the exception that they include a 1/8 duty cycle 8 kHz pre-sampler on their inputs (RxI).

This circuitry resamples the codec's PAM output and thereby effecively eliminates the sinx/x distortion normally associated with 15% to 100% 8 kHz PAM pulse trains and eliminates the need to predistort the receive filter's pass-band characteristic.

In normal use as a codec's receive filter, MSI will be an 8 kHz signal. With the MC14407 codec family, the filter MSI is the same as the codec MSI. With other codecs, the MSI signal is receive sync.

The MC14414 may also be used in analog applications by disabling the sinx/x correction. If MSI and CCI are tied together, the receive filter has the same frequency response as the transmit filter and a gain of 18 dB.

Timing And Synchronization

Timing and synchronization of the MC14413-1, -2 and MC14414-1, -2 are provided by the CCI and MSI inputs. A 128 kHz signal should be applied to CCI. An 8 kHz signal, whose low-to-high transition coincides with a new output sample from the PCM codec, should be applied to MSI. The rising edges of theCCI and MSI signals should be skewed no more than 3.0 μs for proper operation.

Logic levels of these signals can be either TTL or CMOS compatible. Choice of logic level can be user determined by applying the appropriate voltage to the level shift control pin, V_{LS}.

Power Down

Both the MC14413-1, -2 and MC14414-1, -2 may be powered down in either of two ways: by bringing V_{AG} to within 0.5 V of V_{DD} or by bringing V_{LS} to within 0.5 V of V_{DD}.

If used on a single supply with the MC14406/7 PCM Codec, the filter IC will power down automatically when the codec does, since the codec raises its V_{AG} pin to V_{DD} in power down. When used in a split supply configuration, the circuit shown in Figure 7 may be utilized.

FIGURE 1 – RECEIVE FILTER TYPICAL AND GUARANTEED PERFORMANCE (MC14413-1, -2/MC14414-1, -2, SINX/X CORRECTION INCLUDED)

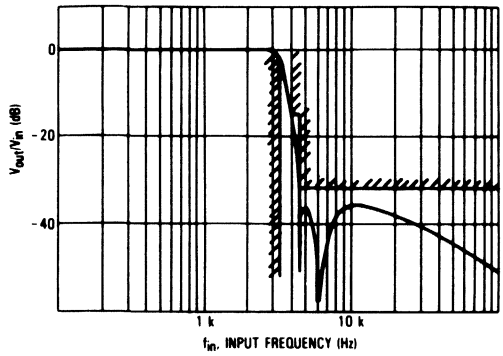


FIGURE 2 – RECEIVE FILTER TYPICAL AND GUARANTEED PASS-BAND PERFORMANCE (MC14413-1, -2/MC14414-1, -2)

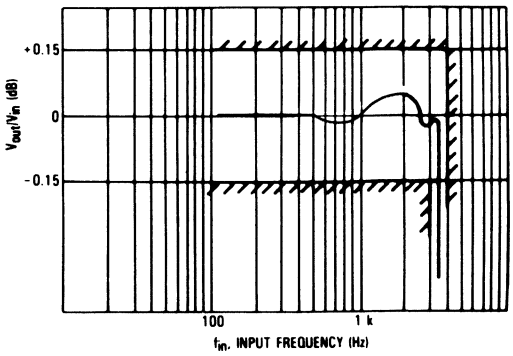


FIGURE 3 – TRANSMIT FILTER TYPICAL AND GUARANTEED PERFORMANCE (MC14413-1, -2 AND MC14414-1, -2 USING FIGURES 10 AND 11)

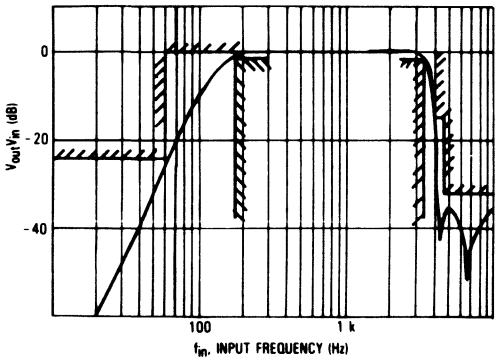


FIGURE 4 – TRANSMIT FILTER TYPICAL AND GUARANTEED PASS-BAND PERFORMANCE (MC14413-1, -2 AND MC14414-1, -2 USING FIGURES 10 AND 11)

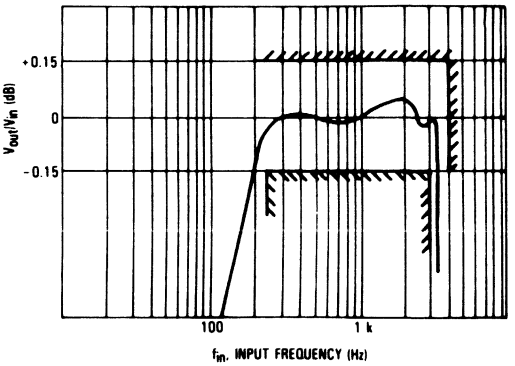


FIGURE 5 – TRANSMIT FILTER TYPICAL AND GUARANTEED PASS-BAND PERFORMANCE (MC14414-1, -2)

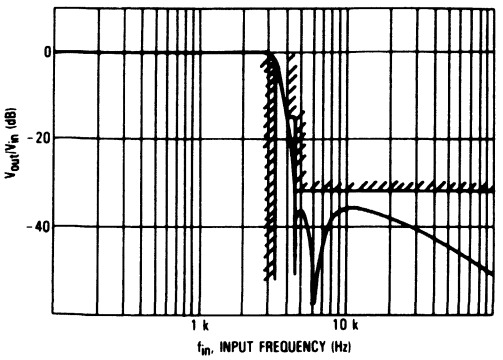


FIGURE 6 – TRANSMIT FILTER TYPICAL AND GUARANTEED PERFORMANCE (MC14414-1, -2)

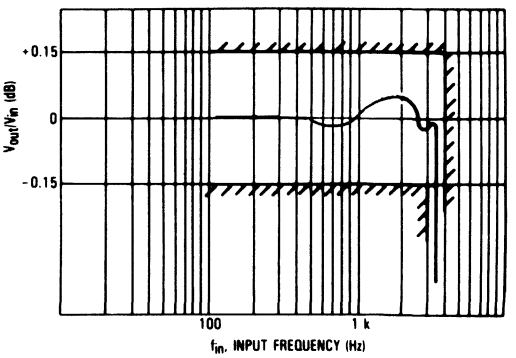


FIGURE 7 – TYPICAL CIRCUIT CONFIGURATION
USING THE MC14407 CODEC AND MC14413-1, -2 FILTER
(SPLIT SUPPLY)

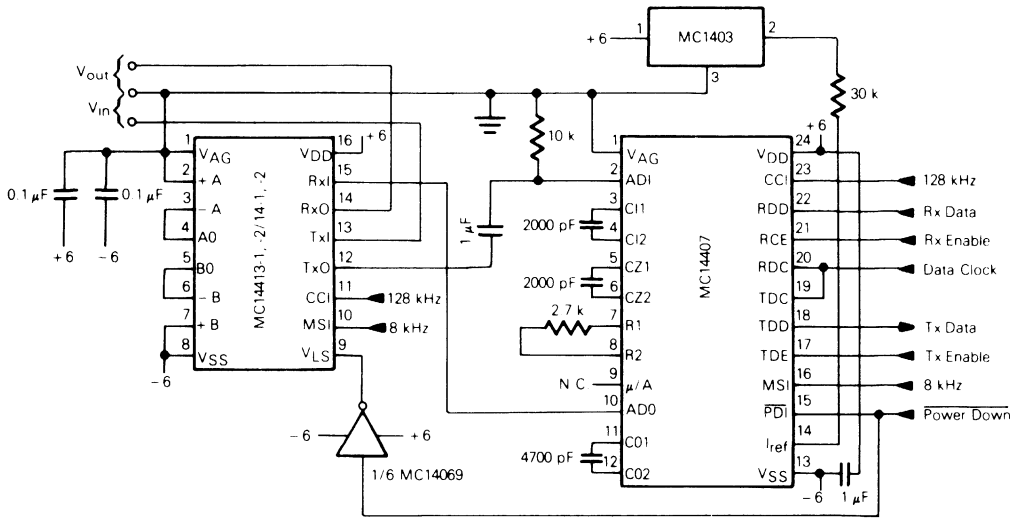
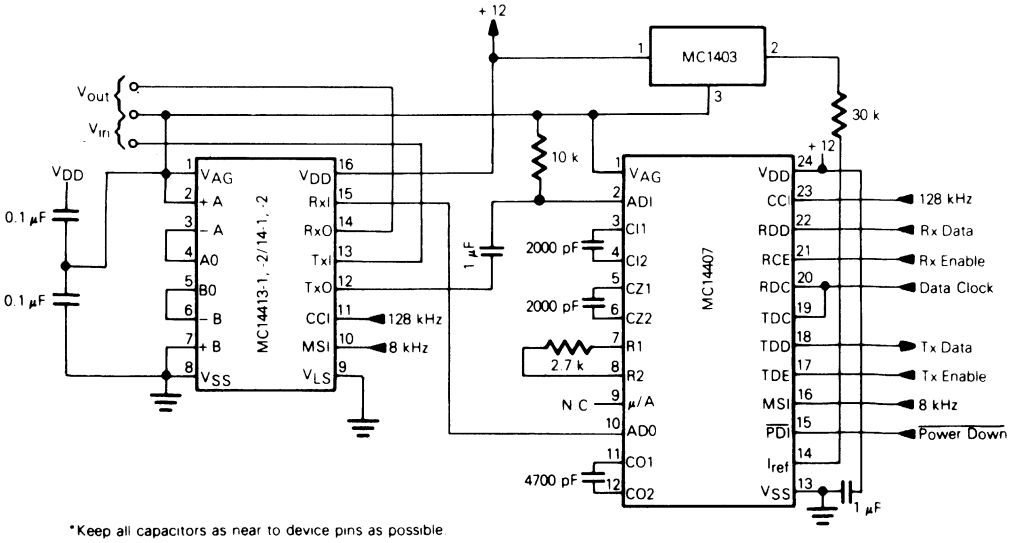


FIGURE 8 – TYPICAL CIRCUIT CONFIGURATION
USING THE MC14407 CODEC AND MC14413-1, -2 FILTER
(SINGLE SUPPLY)



*Keep all capacitors as near to device pins as possible

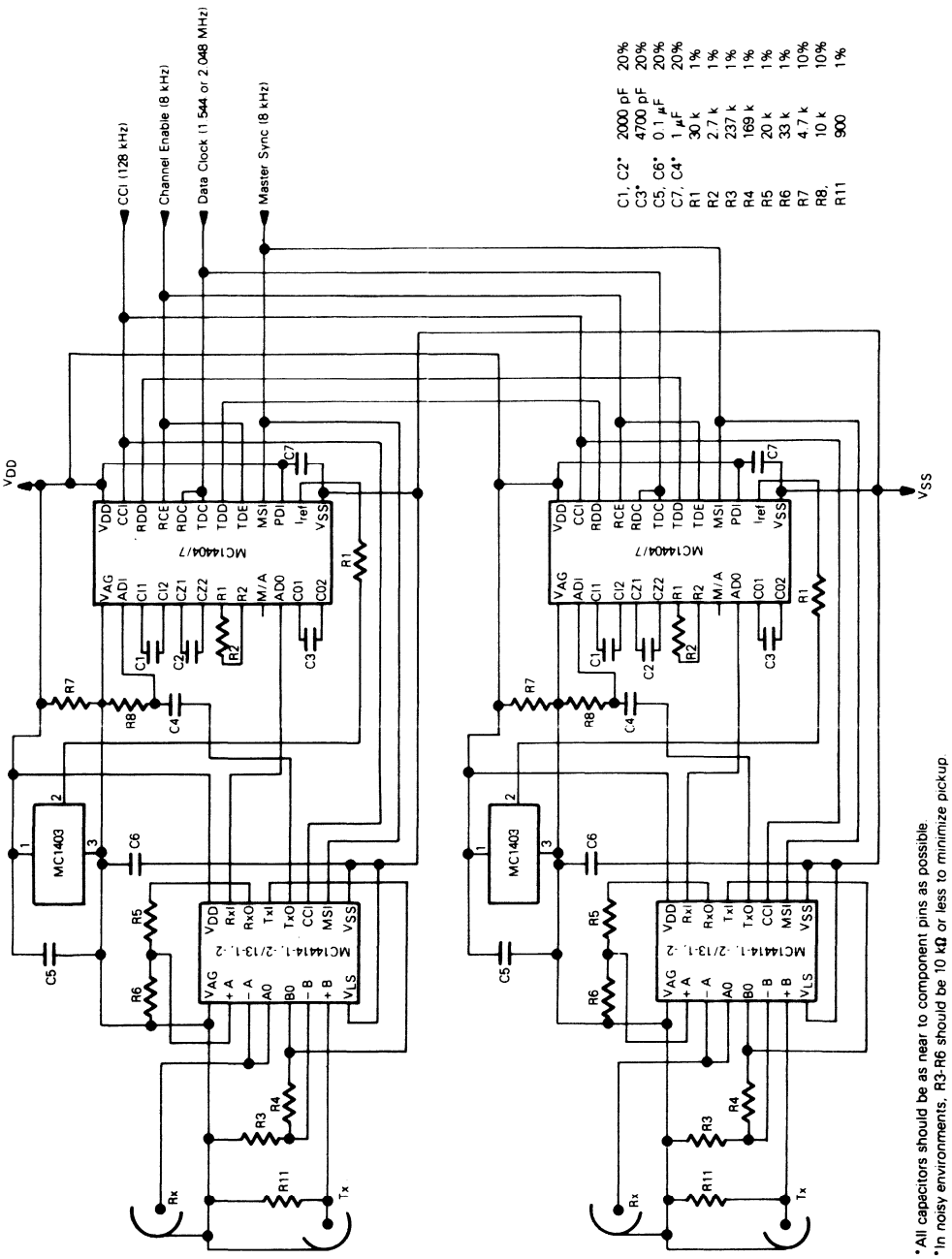


FIGURE 9 – MOTOROLA CODEC FILTER EVALUATION BOARD

*All capacitors should be as near to component pins as possible.
*In noisy environments, R3-R6 should be 10 kΩ or less to minimize pickup.

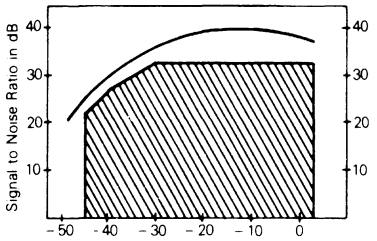
3

3

TYPICAL END-TO-END CHANNEL PERFORMANCE FOR MOTOROLA
MC14413-1, -2/14-1, -2-MC14404/7 CODEC AND FILTER

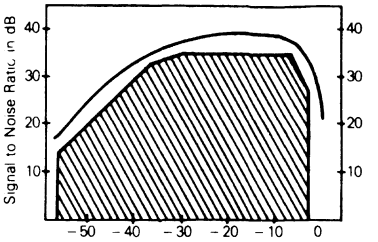
MC14407/13-2
SPECIFICATION BELL PUB 43801

QUANTIZING DISTORTION
SINUSOIDAL INPUT
C MESSAGE WEIGHTED

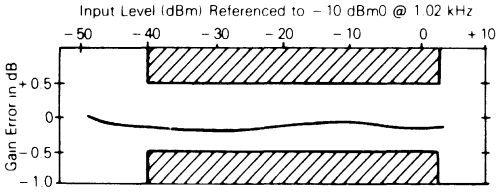


MC14404/13-1
SPECIFICATION CCITT G7.12

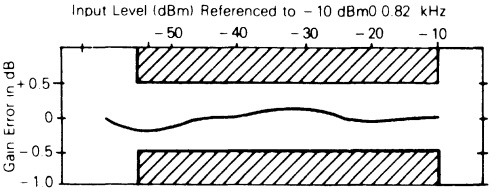
QUANTIZING DISTORTION
PSEUDO RANDOM NOISE
3 kHz FLAT WEIGHTING



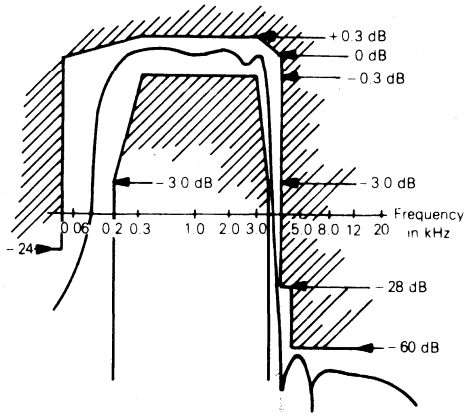
SINUSOIDAL GAIN TRACKING



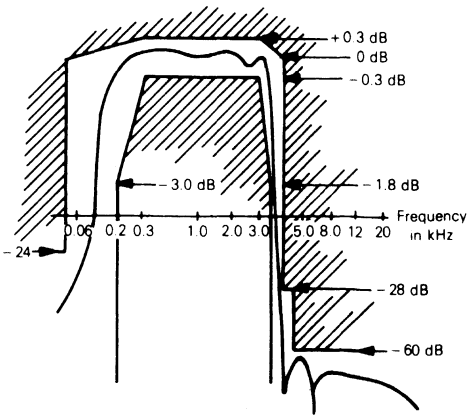
PSEUDO-RANDOM NOISE GAIN TRACKING



GAIN vs FREQUENCY, SINUSOIDAL



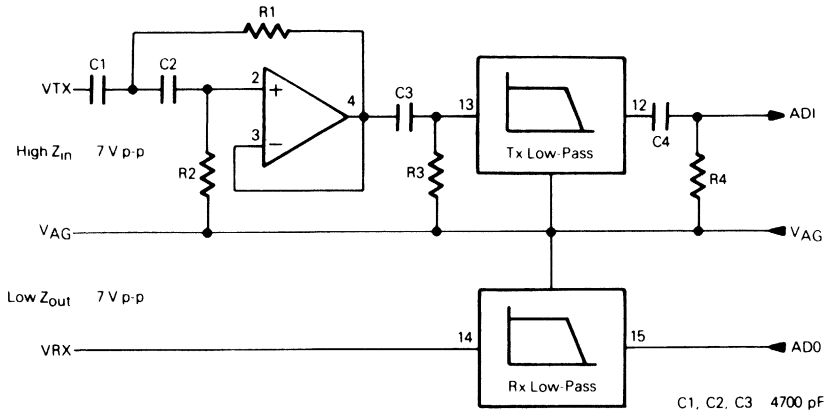
GAIN vs FREQUENCY, SINUSOIDAL



TYPICAL END-TO-END PERFORMANCE OF MOTOROLA CODEC AND FILTER
(All measurements made using HP3779B PCM Test Set)

Specification	Typical Performance of MC14407/4 Codec and MC14413 Filter	Bell System D4 Voice Frequency Requirements PUB 43801	CCITT G7.12 Voice Frequency Requirements
Channel Saturation	+3 dBm0	+3 dBm0	+3 dBm0
Gain Tracking with 1 kHz Tone			
+3 to −40 dBm0	±0.2 dB	≤ ±0.5 dB	≤ ±0.5 dB
−40 to −50 dBm0	±0.3 dB	≤ ±1.0 dB	≤ ±1.0 dB
−55 dBm0	±0.5 dB	≤ ±3.0 dB	≤ ±3.0 dB
Quantizing Distortion @ 1 kHz			
+3 to −30 dBm0	37 dB	≥ 33 dB	> 33 dB
−35 dBm0	34 dB	≥ 30 dB	≥ 30 dB
−40 dBm0	31 dB	≥ 27 dB	≥ 27 dB
−45 dBm0	25 dB	≥ 22 dB	≥ 22 dB
Idle Channel Noise with VTX = V_{AG}	16 dBrnc0	≤ 23 dBrnc0	≤ −65 dBm0P
Quiet Code Noise (all 1's at decoder (RDD) input)	10 dBrnc0	≤ 15 dBrnc0	≤ −75 dBm0P
Selective Response @ Multiplex of 8 kHz	−60 dBm0	See Frequency Response	≤ −50 dBm0
Frequency Response @ 0 dBm0 Input			
50 Hz Gain Relative to 1.02 kHz	−28 dB	−	≤ −24 dB
60 Hz Gain or 0.820 kHz	−24 dB	≤ −20 dB	−
200 to 300 Hz Ripple	±0.20 dB	≤ ±0.3 dB	≤ ±0.5 dB
3400 Hz Gain	−1.0 dB	≥ −3.0 dB	≥ −1.8 dB
4000 Hz Gain	−32 dB	≤ −28 dB	≤ −28 dB
≥ 4600 Hz Gain	< −62 dB	≤ −60 dB	≤ −60 dB
Single Frequency Spurious Response			
In Band with Input 1 kHz @ 0 dBm	≤ −44 dB	≤ −40 dB	≤ −40 dB
Out of Band with Input 0 to 12 kHz @ 0 dBm	≤ −32.5 dB	≤ −28 dB	≤ −25 dB
Differential Delay Distortion			
1150 to 2300	58 μs	≤ 60 μs	
1000 to 2500	72 μs	≤ 100 μs	
900 to 2700	91 μs	≤ 200 μs	

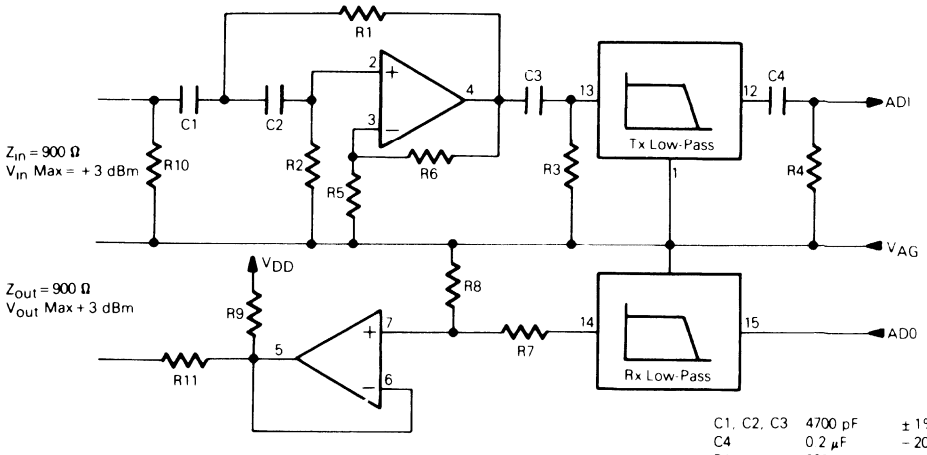
FIGURE 10 — FILTER SCHEMATIC FOR MC14414-1, -2 WITH 60 Hz REJECT FILTER



C1, C2, C3	4700 pF	±1%
C4	0.2 μF	−20% +80%
R1	112 kΩ ¼ W	1%
R2	620 kΩ ¼ W	1%
R3	223 kΩ ¼ W	1%
R4	100 kΩ ¼ W	10%

*In noisy environments, R1-R4 should be 10 kΩ or less to minimize pickup

FIGURE 11 – FILTER SCHEMATIC FOR MC14414-1, -2 WITH 60 Hz REJECTION AND 900 TERMINATION



C1, C2, C3	4700 pF	± 1%
C4	0 2 μF	– 20% + 80%
R1	236 kΩ ¼ W	1%
R2	294 kΩ ¼ W	1%
R3	223 kΩ ¼ W	1%
R4	100 kΩ ¼ W	10%
R5	200 kΩ ¼ W	1%
R6	169 kΩ ¼ W	1%
R7	24 kΩ ¼ W	1%
R8	33 kΩ ¼ W	1%
R9	1 8 kΩ ¼ W	10%
R10	900 Ω ¼ W	1%
R11	900 Ω ¼ W	1%

*In noisy environments, R1-R8 should be 10 kΩ or less

FIGURE 12 – TYPICAL 2-WIRE PORT INTERFACE USING MC14413

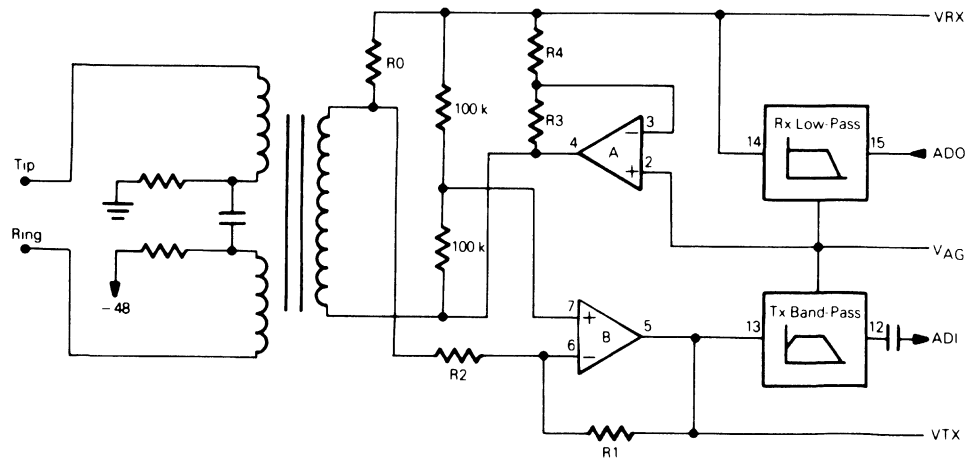
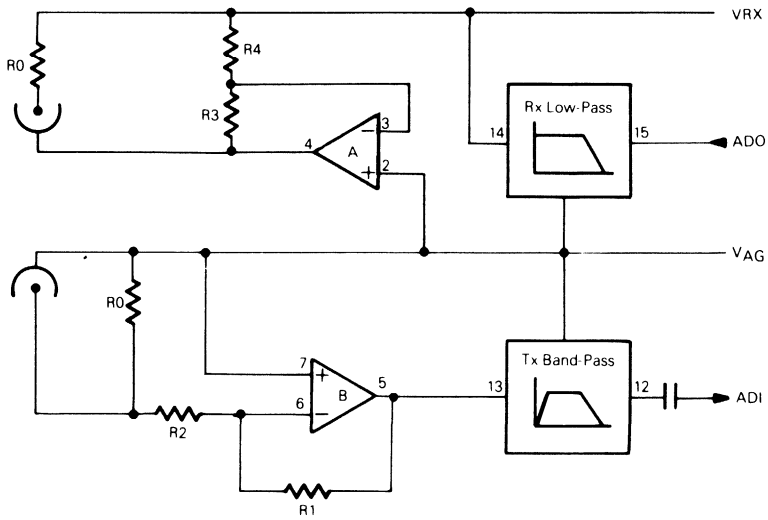


FIGURE 13 – TYPICAL 4-WIRE PORT INTERFACE USING MC14413



Full Scale Voltage at TxO (LPO) RxI	Port Impedance (RO)	Relative Level	R1	R2	R3	R4
5 V p-p	600	4.16 dBr	161 k	100 k	23.9 k	100 k
	900	2.4 dBr	198 k	150 k	51.8 k	100 k
6.2 V p-p, +9 dBm	600	6.00 dBr	100 k	100 k	Short	Open
	900	4.26 dBr	245 k	150 k	18.5	100 k
7.6 V p-p, +9 dBm	900	6.00 dBr	150 k	150 k	Short	Open

Interface to 2-wire or 4-wire ports using the MC14413-1, -2/14-1, -2 is shown in Figures 12 and 13, respectively. The table above shows some voltages typically used with the filter and the appropriate resistor values for cases in which the codec/filter OTLP is less than or equal to the 0 dBm level. If the codec/filter overload voltage is greater than required for 0 dBm levels in the load, the RxO output can be voltage divided by two resistors and the extra op amp used as a voltage follower.

FIGURE 14 – GENERATOR FOR 128 kHz IN SYSTEM USING 2.048 MHz CLOCK

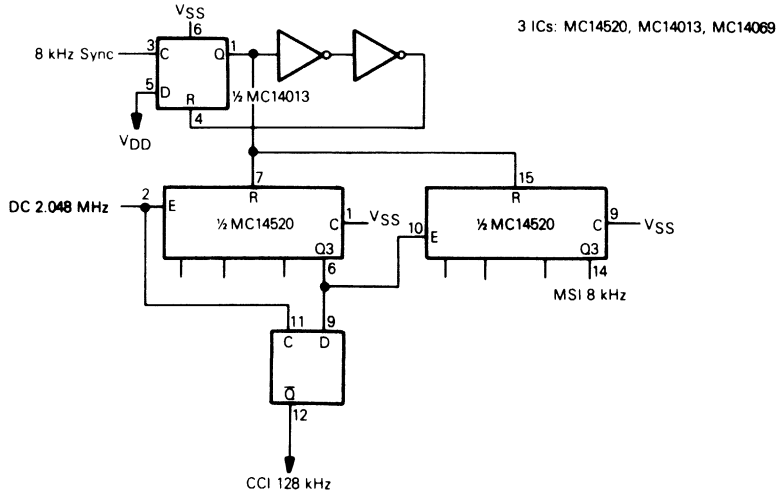


FIGURE 15 – 128 kHz FREQUENCY SYNTHESIZER USING 8 kHz INPUT

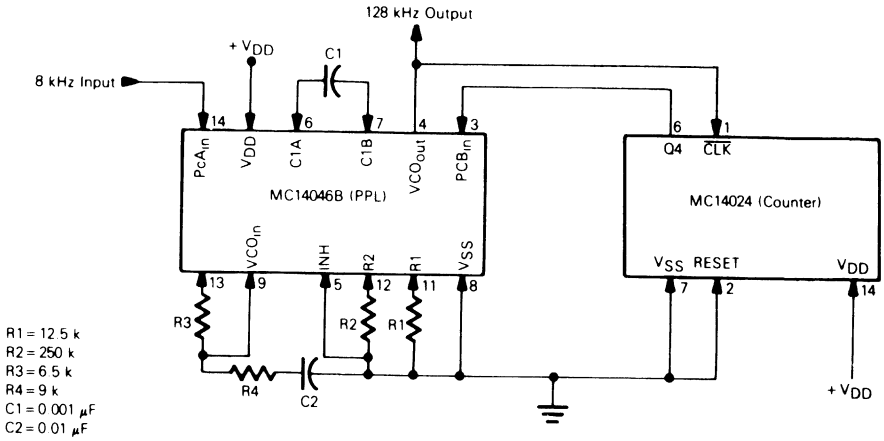


FIGURE 16 – GENERATION OF 128 kHz IN SYSTEM USING 1.544 MHz CLOCK

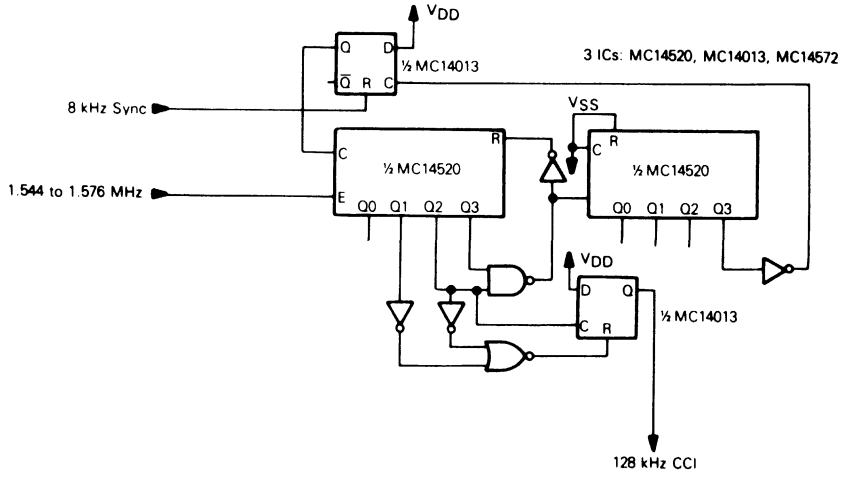
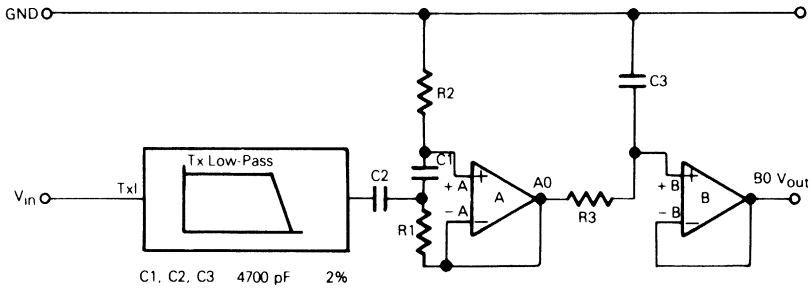


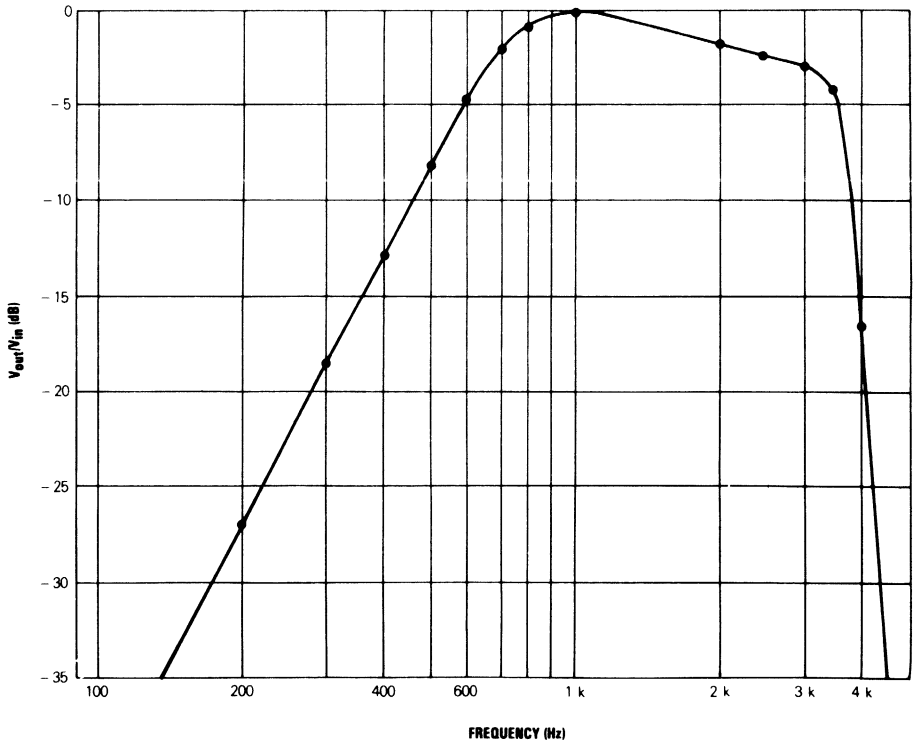
FIGURE 17 — TELEPHONY C-MESSAGE FILTER USING MC14414-1, -2 FILTER



C1, C2, C3	4700 pF	2%
R1	19.6 k	1%
R2	97.6 k	1%
R3	8.25 k	1%

V_{AG}, V_{LS} connected to GND
MSI, CCI connected to 134 kHz TTL clock
0.1 μF, V_{DD} to V_{AG} and V_{SS} to V_{AG}
Rx Filter can also be used and will provide 18 dB of input gain
V_{DD} = +5 V, V_{SS} = −5 V

NOTE: Op Amps A and B are the free op amps on the MC14414-1, -2 filter.



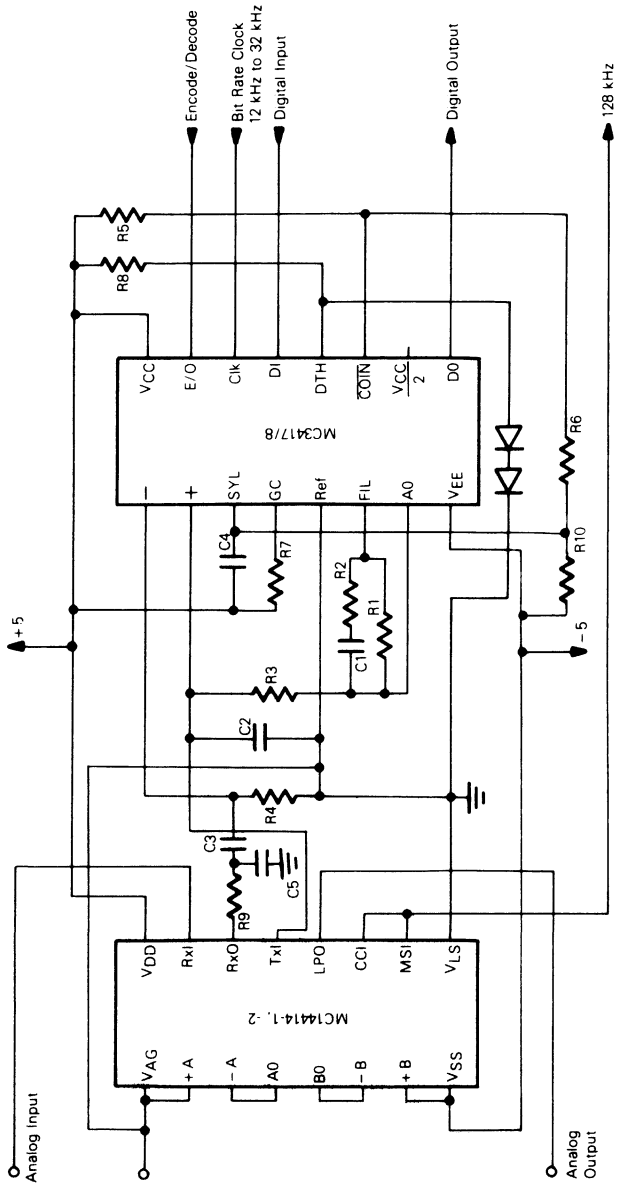


FIGURE 18 — DELTAMOD VOICE DIGITIZER USING MC3417 AND MC14414-1, -2

MOTOROLA

MC14416
MC14418

PER CHANNEL, ADDRESSABLE TIME SLOT ASSIGNER CIRCUITS (TSACs)

The MC14416 and MC14418 are per channel devices that allow variable codec time slot assignment to be programmed through a serial microprocessor port (0-63 time slots). Both devices have independent transmit and receive frame syncs and enables. They also include chip select and clear to send signals which simplify system design.

The MC14418 provides the additional addressing capability which allows a parallel bus back plane in the channel group. In addition, the MC14418 provides control bits which can be used for the power down, ring enable and ring trip functions on a line circuit.

The MC14416 provides the ability to multiplex off hook signals for a bank of TSACs.

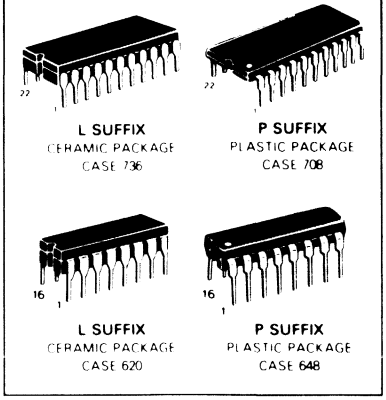
Both devices are fabricated using the CMOS technology for reliable low power performance. The MC14418 is the full featured device produced in a 22 pin package. The MC14416 without the addressing capability is offered in a 16 pin package.

- Low Power
- 5-Volt Interface on Microprocessor Port
- 5-16 Volt Output Logic Levels
- Independent Transmit and Receive Frame Syncs and Enables
- Up to 64 Time Slots Per Frame
- For Use With Up to 2.56 MHz Clocks
- Provides Power Down Control for Line Circuits
- Compatible with MC14400/01/02/03/05 and MK5116 Codecs
- Provides the Ring Enable and Ring Trip Functions (MC14418)
- Allows Use of a Parallel Backplane for Line Circuits Due to the Hard Wired Address Feature (MC14418)
- Off-Hook Multiplex Control (MC14416)
- CMOS Metal Gate for High Reliability

MOS LSI

(LOW-POWER COMPLEMENTARY MOS)

TSAC
TIME SLOT ASSIGNER
CIRCUITS



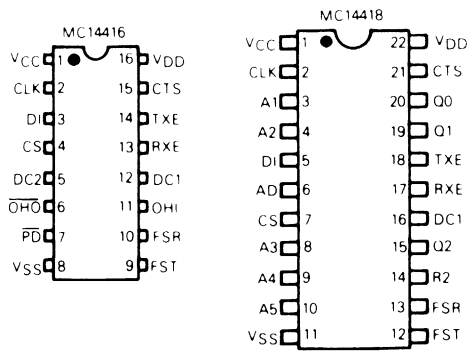
L SUFFIX
CERAMIC PACKAGE
CASE 736

P SUFFIX
PLASTIC PACKAGE
CASE 708

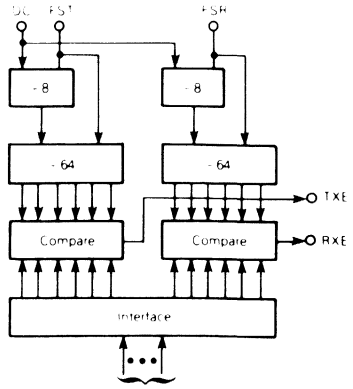
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENTS



BLOCK DIAGRAM



See Figures 3 and 4

DS9864R1

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	Vdc
Level Shift Voltage	V_{CC}	−0.5 to V_{DD}	Vdc
Input Voltage Inputs Referenced to V_{DD} to V_{CC}	 V_{in1} V_{in2}	 −0.5 to V_{DD} +0.5 −0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +165	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$)

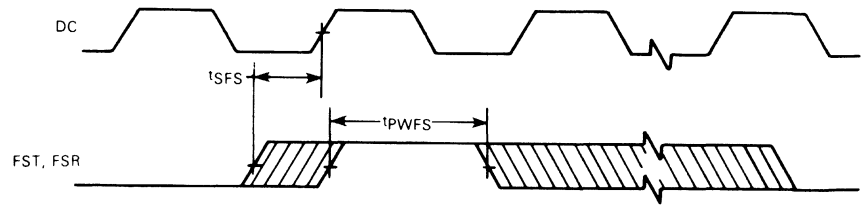
Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
DC Supply Voltage $V_{SS} = 0$ V	V_{DD}	–	4.5	12	16	V
DC Supply Voltage $V_{SS} = 0$ V	V_{CC}	–	4.5	5	V_{DD}	V
Output Current TXE, RXE, Q0, Q1, Q2, $\overline{P_D}$						
($V_{OL} = 0.4$ V)	I_{OL}	5	0.51	–	–	mAdc
($V_{OL} = 1.0$ V)		12	2.0	4.0	–	
($V_{OH} = 4.6$ V)	I_{OH}	5	−0.20	–	–	mAdc
($V_{OH} = 1.0$ V)		12	−2.0	−4.0	–	
Output Current CTS, OHO						
($V_{OL} = 0.8$ V)	I_{OL}	5	3.0	5.5	–	mAdc
($V_{OL} = 0.8$ V)		12	6.6	11.5	–	
($V_{OL} = 1.5$ V)		12	12.0	20.0	–	
($V_{OH} = 0.8$ V)	I_{OH}	5	−8	−20	−40	µAdc
($V_{OH} = 2.0$ V)		5	−6	−18	−40	
($V_{OH} = 0.8$ V)		12	−40	−100	−200	
($V_{OH} = 2.0$ V)		12	−35	−90	−200	
($V_{OH} = 10.5$ V)		12	−15	−30	−60	
Input Voltage (CMOS) "0" Level FST, FSR, R2, DC1, DC2, A1, A2	V_{IL}	5 12	– –	– –	1.0 2.4	Vdc
A3, A4, A5, OHI "1" Level	V_{IH}	5 12	4.0 9.6	– –	– –	Vdc
Input Current OHI (Active Pull Down)	I_{inH}	5 12	+1.5 +10	+4.0 +25	+15 +100	µAdc
Input Voltage (TTL) "0" Level CLK, CS, AD, DI	V_{IL}	5 12	– –	– –	0.8 0.8	Vdc
$V_{CC} = 5$ V "1" Level	V_{IH}	5 12	2.00 2.00	– –	– –	Vdc
Input Current	I_{in}	15	–	$\pm 10^{-5}$	±0.1	µAdc
Input Capacitance	C_{in}	–	–	5	7.5	pF
Total Supply Current (Outputs Unloaded) $V_{DD} = 12$ V DC1 at 2.048 MHz $V_{DD} = 5$ V	I_T	12 5	– –	3 2	6 4	mAdc
Total Supply Current (Power Down) MC14418 Only After CTS = V_{DD} CLK, CS, AD, DI Inputs ≤ 0.6 V	I_{PD}	–	–	–	0.1	mAdc

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C, unless otherwise noted)

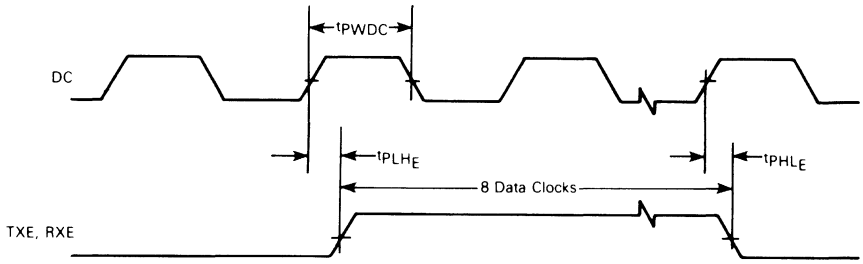
Characteristic	Symbol	Fig.	V_{DD}	Min	Typ	Max	Unit
Output Rise Time TXE, RXE, Q0, Q1, Q2, $\overline{P_D}$	t_r	–	5 12	– –	100 50	200 100	ns
Output Fall Time TXE, RXE, Q0, Q1, Q2, $\overline{P_D}$	t_f	–	5 12	– –	100 50	200 100	ns
Frame Sync Setup Time	t_{SFS}	1	5 12	−150 −75	– –	+150 +75	ns
Frame Sync Pulse Width	t_{PWFS}	1	5 12	200 100	– –	– –	ns
Propagation Delay – DC to TXE, RXE (Note 1) C_L = 20 pF	t_{PLHE}, t_{PHLE}	1	5 12	– –	130 80	180 125	ns
Data Clock Frequency	f_{DC}	–	5 12	– –	– –	2.048 2.6	MHz
Data Clock Pulse Width (at $f_{DC(MAX)}$)	t_{PWDC}	1	5 12	200 140	244 192	293 260	ns
Clock Frequency	f_{CLK}	–	5 12	00 00	– –	0.3 0.3	MHz
Clock Pulse Width (at $f_{CLK(MAX)}$)	t_{PWC}	2	5 12	0.5 0.5	– –	– –	µs
Address and Data Setup Time	t_{su}	2	5 12	300 300	– –	– –	ns
Address and Data Hold Time	t_h	2	5 12	200 200	– –	– –	ns
Propagation Delay DC1 to CTS	t_{PCL}	2	5 12	– –	– –	250 150	ns
DC1 or FST to CTS 10K Pullup or Equivalent	t_{PCH}	2	5 12	– –	– –	300 200	ns
Propagation Delay DC to PD	t_{PQ}	2	5 12	– –	– –	300 200	ns
DC to Q0-Q2	t_{PQ}	2	5 12	– –	– –	300 200	ns
Propagation Delay – R to Q2	t_P	2	5 12	– –	100 50	200 100	ns
Chip Select Setup Time Leading CS to Falling CLK	t_{SCS}	2	5 12	1 1			µs
Chip Select Hold Time Falling CTS to Falling CS	t_{HCS}	2	5 12	10 10	– –	– –	ns

NOTE 1: For time slot 0, t_{PHLE} and t_{PLHE} are measured from leading edge of DC or FST (FSR), whichever occurs last.

FIGURE 1 — TIMING DIAGRAMS



NOTE: No restriction on falling edge.



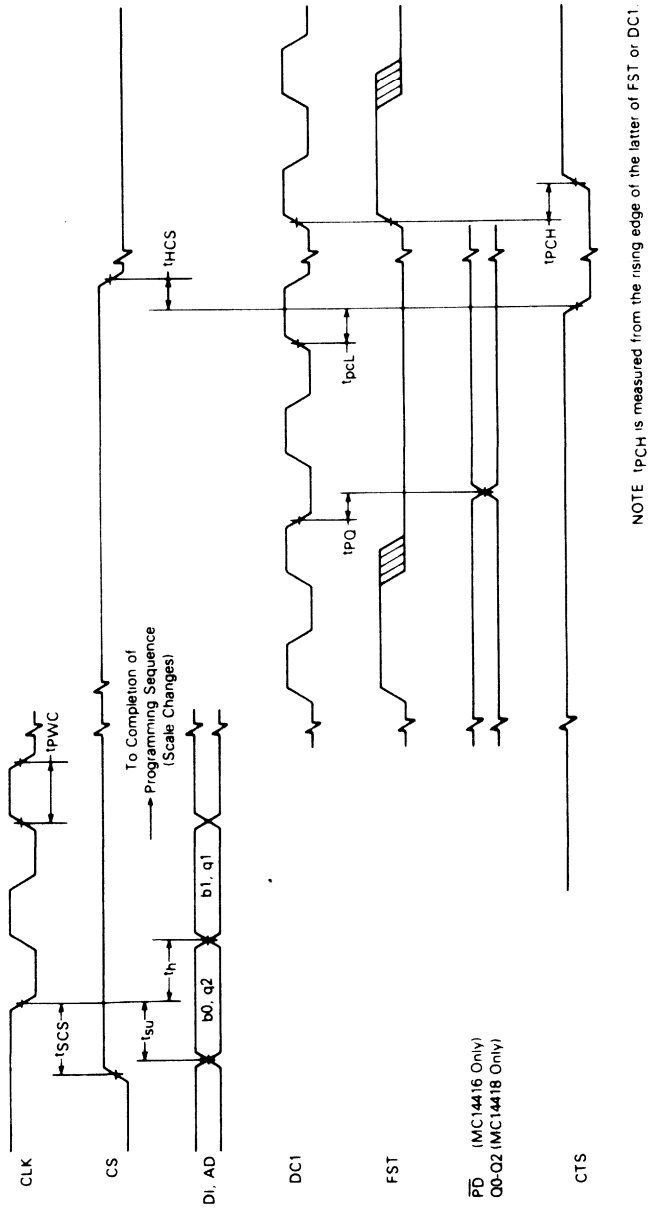


FIGURE 2 – PROPAGATION DELAYS FOR PROCESSOR INTERFACE PINS

NOTE: t_{PCH} is measured from the rising edge of the latter of FST or DC1.

FIGURE 4 – MC14416 16 PIN

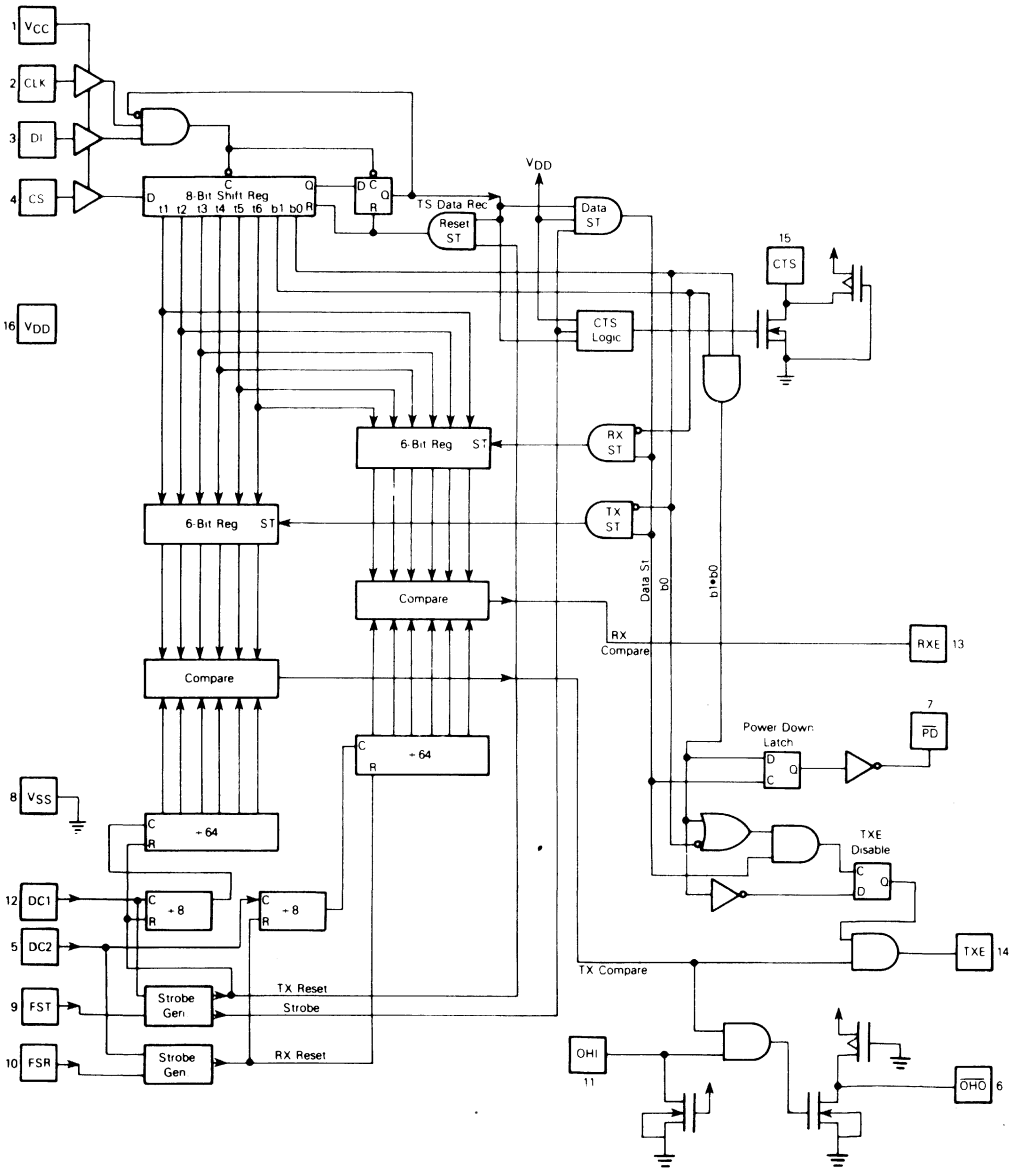
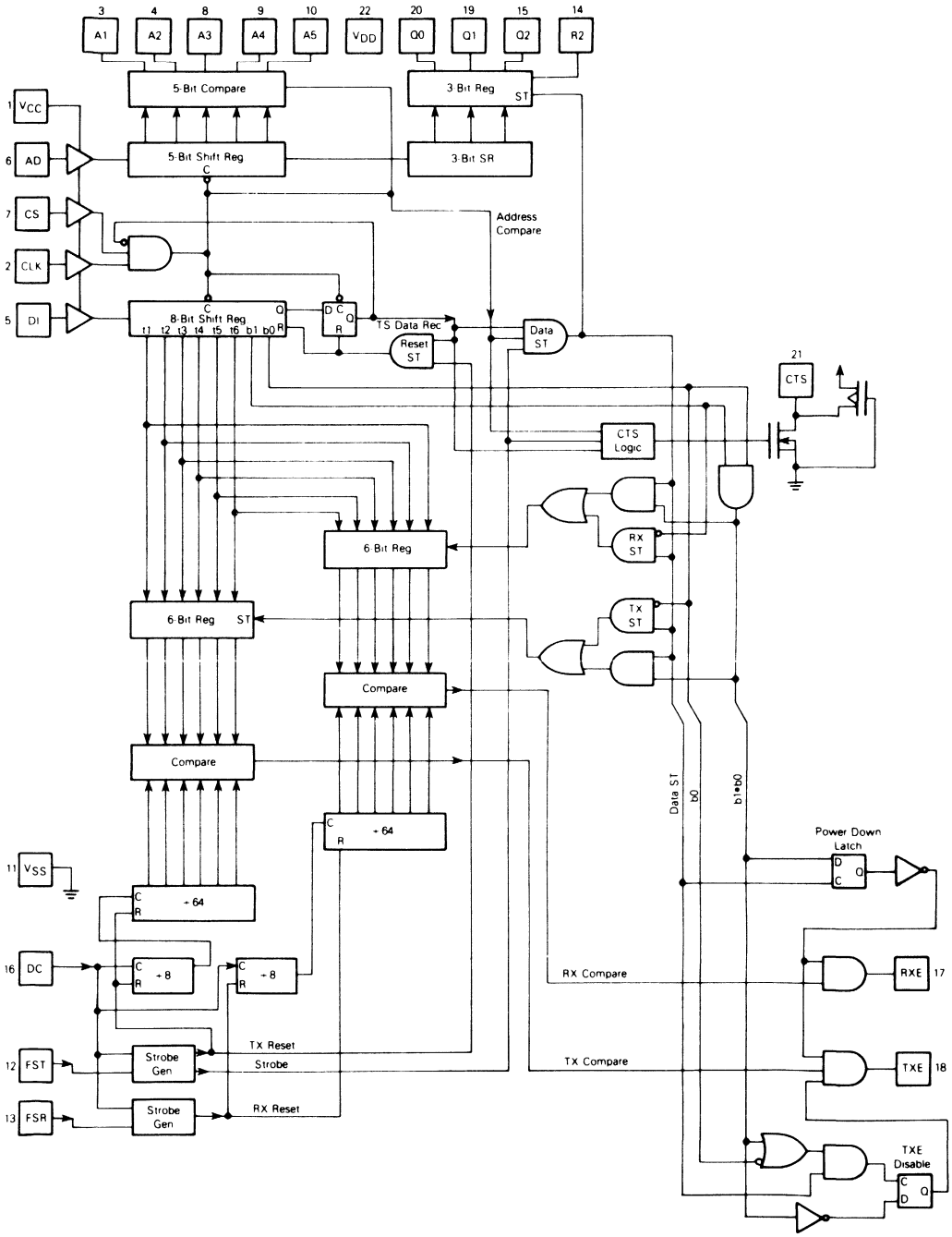


FIGURE 3 – MC14418 22 PIN



GENERAL DEVICE DESCRIPTION

The MC14416 and MC14418 TSACs are microprocessor peripherals intended to be used to control and supervise per channel codec subscriber channel units. The TSACs consist of three basic functions.

The Serially Programmable Microprocessor Port consists of V_{CC}, CLK, DI, CS and CTS for the MC14416 and further includes AD and A1 through A5 for the MC14418. This port allows the call processing microprocessor to access load data into each TSAC. See the applications section for a detailed description of the microprocessor port. Figure 5 defines the data word bit assignments.

The Supervision Controls consist of Q0, Q1, Q2, R2 on the MC14418 and OHI, $\overline{OHO}$ and $\overline{PD}$ on the MC14416. These functions provide data path for the supervision and control of user selected requirements in the subscriber channel unit. Figure 3 shows some typical uses of these bits.

The Time Slot Computation section of the chip derives separate transmit and receive time slot outputs (TXE and RXE) for the controlled codec from the bit rate clock and sync pins DC1, DC2, FST and FSR, respectively. The computed time slot is then derived from the information received through the microprocessor port.

PIN DESCRIPTIONS

V_{CC} (Positive Supply for Microprocessor Port) – If this is a 5-volt supply, AD, DI, CS and CLK are TTL compatible CMOS inputs. V_{CC} may be any voltage from 4.5 V to V_{DD} allowing either TTL or CMOS compatibility.

CS (Chip Select Input) – For the MC14418, the pin is used to select a bank of TSACs.

For the MC14416, the CS is used to select that individual TSAC. All CSs are normally held low. To PROGRAM A SPECIFIC TSAC, CS must go high prior to the first falling edge of CLK. CS must stay high until the selected CTS goes low to guarantee a valid access.

CS is synchronous with DI, AD and CLK. CS can be asynchronous with DC1, DC2, FST or FSR. (This pin is normally intended to be set by a microprocessor.)

CLK (Microprocessor Clock Input) – Serial data is entered through the AD and DI pins under the control of CLK. The data is entered on the trailing edge of CLK. CLK is synchronous with CS, AD and DI and can be asynchronous with the TSAC's data clocks (DC1 or DC2).

DI (Serial Time Slot Data and Mode Input) – 8-bit words are clocked into the device through DI under the control of CLK after CS is brought high. The first 2 bits of DI control the various programming modes while the last 6 bits are time slot data. (See Figure 5 for the format of the DI word.)

AD (Serial Address and Control Bits Input – MC14418 only) – 8-bit words are clocked into the device through AD under the control of CLK after CS is brought high. AD words are loaded in parallel with the DI words. The first 3 bits of AD program the control bits Q0, Q1, and Q2 while the last 5 bits are compared with the hardware address on A1 through A5 to identify a specific TSAC in a bank. (See Figure 5 for the format of the AD words.)

A1-A5 (Codec Address Inputs – MC14418 only) – These five pins provide a unique identity for each TSAC. The TSAC address pins are either hardwired on the PC board or in the channel bank backplane. The processor loads the 5-bit address data into AD, and each MC14418 in the selected bank compares this data to the hardwired address set by its A1-A5 to determine if the time slot data loaded into DI is intended for that TSAC. By this process, only one of 32 TSACs in a bank will accept the transmitted time slot data. A1-A5 are CMOS inputs, logical "1" = V_{DD} and logical "0" = V_{SS}.

Q0, Q1, Q2 (Status Bit Outputs – MC14418 Only) – These three bits are programmed by the first 3 bits of the 8-bit word which is loaded into AD. The bits are used for the basic control functions of a line circuit. See the applications section (ref. Figure 11) for an example of how these status bits are used. In this example, Q1 selects to receive data streams, Q0 is used for the power down control, and Q2 is used for the ring enable. These are CMOS outputs.

R2 (Reset Input for Q2) – The R2 input provides a direct reset of the Q2 output. When R2 is taken high, Q2 is set to "0" independent of all other TSAC functions. See the applications section (ref Figure 11) for an example of how this reset bit is used, i.e., the ring trip signal is used to reset Q2 which is the ring enable. This combination of R2 and Q2 allows a simple solution to the ring trip function.

CTS (Clear to Send Output) – This output provides a simple diagnostic capability for the processor TSAC combination. The selected TSAC outputs the CTS signal after it has accepted data. This output goes low three data clock cycles after the next FST, and returns high on the subsequent FST. For the MC14418, only the TSAC which accepts transmitted data will respond with CTS low. All other TSACs in the bank will leave CTS high. The CTS output is an open drain transistor with a weak internal pullup. Normally a bank of CTS outputs are wire ORed together to provide a single diagnostic bus, which can be used to verify that transmitted data was properly acknowledged by some TSAC in the bank.

CTS may also be used to strobe additional supervision data into a selected channel unit, due to its dependence upon the address selection logic of the MC14418.

DC1, DC2 (Data Clock Input) – The data clock input establishes the bit rate of the TSAC and its associated codec. It is intended to be between 1.536 and 2.56 MHz and is the same as the codec's bit rate clock. Both TSACs divide

these inputs by eight to derive the time slot rate. For the MC14418, DC1 provides the data rate clock for both transmit and receive time slot computation. The MC14416 derives transmit timing from DC1 and receive timing from DC2. They are CMOS compatible inputs.

FST, FSR (Frame Sync Transmit and Frame Sync Receive Inputs) – These inputs are leading-edge sensitive synchronization pulses for establishing the position of time slot zero in the transmit and receive frames, respectively.

The rising edge of DC (1 or 2) associated with the rising edge of FST or FSR identifies the sign bit period of time slot zero. See Figures 6 and 7 for detailed timing. In the MC14418, both zero time slots are derived from DC1 but may be different by an integral number of bits. In the MC14416, FST and DC1 derive the transmit time slot zero, while FSR and DC2 derive the receive time slot zero independently. DC1 and DC2 can be asynchronous. FSR and FST are CMOS inputs.

TXE, RXE (Transmit Enable and Receive Enable Outputs) – These are the outputs of the time slot computation circuitry. Each output is high for eight data clocks; i.e., an integral number of time slots after the rising edge of FST and FSR for TXE and RXE, respectively. The binary number entered in the last 6 bits of the DI input indicates the number of eight data clock intervals (time slots) between FST or FSR and the eight data clock time slot, when TXE or RXE will be high. These are CMOS B series outputs which will drive one TTL LS input when V_{DD} is five volts. See Figure 6 and Figure 7 for detailed timing and numbering.

3

TABLE 1 – BASIC OPERATION OF MC14418

Input Conditions							Action to Outputs After Next FST			
TS Data Received	Address Compare	b0	b1	CTS	TX Reg. Load	RX Reg. Load	TXE Disabled	RXE Disabled	Data Reg. (Q0-Q2) Load	Time Slot Counters Running
No	X	X	X	1	No	No	No Change	No Change	No	No Change
Yes	No	X	X	1	No	No	No Change	No Change	No	No Change
Yes	Yes	0	0	0	Yes	Yes	No	No	Yes	Yes
Yes	Yes	0	1	0	Yes	No	No	No	Yes	Yes
Yes	Yes	1	0	0	No	Yes	No Change	No	Yes	Yes
Yes	Yes	1	1	0	X	Yes	Yes	Yes	Yes	No

TABLE 2 – BASIC OPERATION OF MC14416

Input Conditions					Action to Outputs After Next FST			
TX Data Received	CS	b0	b1	CTS	TX Reg. Load	RX Reg. Load	TXE Disabled	$\overline{PD}$ Output
No	X	X	X	1	No	No	No Change	No Change
Yes	0	X	X	1	No	No	No Change	No Change
Yes	1	0	0	0	Yes	Yes	No	1
Yes	1	0	1	0	Yes	No	No	1
Yes	1	1	0	0	No	Yes	No Change	1
Yes	1	1	1	0	No	No	Yes	0

Note 1: The $\overline{OHO}$ output remains operational when TXE is disabled.

FIGURE 5 — FORMAT FOR DI AND AD WORDS

MC14418	DI Word Input								AD Word Input							
	First Bit Sent								First Bit Sent							
Results of Bit Pattern	Mode		Time Slot Data						Status Bits			Address Data				
	b0	b1	t6	t5	t4	t3	t2	t1	q2	q1	q0	a5	a4	a3	a2	a1
Assign TSAC 16 to the first time slot (TSO) for both receive and transmit and set its status bit to 011	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0
Assign TSAC 1 to time slot 8 for receive only and set status bits to 011	1	0	0	0	1	0	0	0	0	1	1	0	0	0	0	1
Assign TSAC 8 to time slot 2 for transmit only and set status bits to 011	0	1	0	0	0	0	1	0	0	1	1	0	1	0	0	0
Program TSAC 4 to idle (no time slot outputs) and set status bits to 011	1	1	X	X	X	X	X	X	0	1	1	0	0	1	0	0
Codec 1 is powered down (80 = 0)	X	X	X	X	X	X	X	X	0	1	0	0	0	0	0	1
Line circuit associated with codec 2 is programmed to ring the line (See Fig. 13)	X	X	X	X	X	X	X	X	1	1	1	0	0	0	1	0

MC14416								
Assign the selected TSAC to the first time slot (TSO) for both receive and transmit and set $\overline{PD} = 1$	0	0	0	0	0	0	0	0
Assign the selected TSAC to time slot 8 for receive only and set $\overline{PD} = 1$	1	0	0	0	1	0	0	0
Assign the selected TSAC to time slot 2 for transmit only and set $\overline{PD} = 1$	0	1	0	0	0	0	1	0
Power down the selected TSAC, i.e., $\overline{PD}$ to "0"	1	1	X	X	X	X	X	X

*See Figures 12 and 13 for the hardware implementations using MC14418 and MC14416.

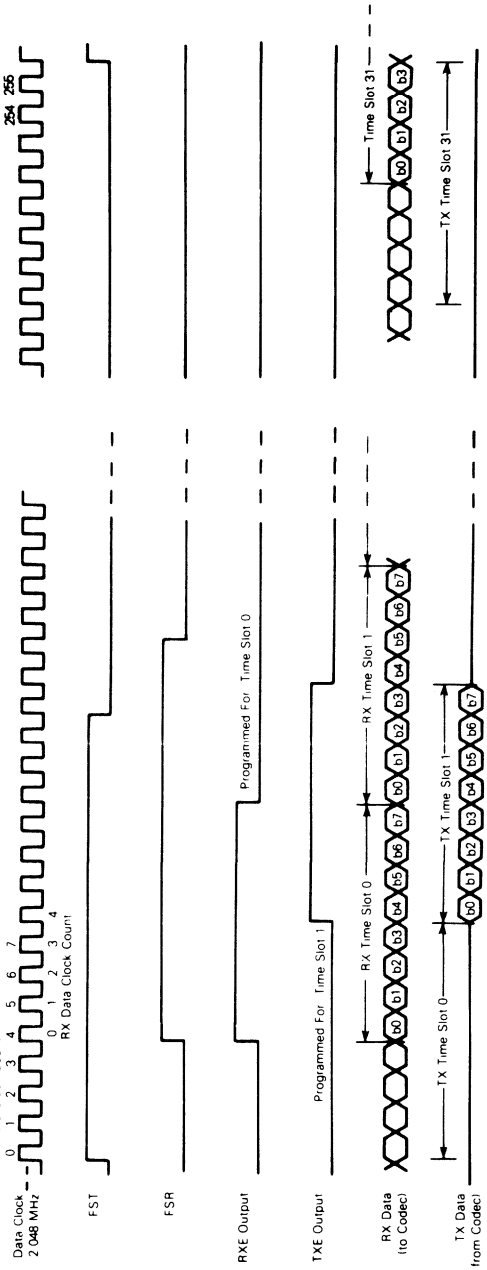


FIGURE 6 – DATA MULTIPLEX TIMING FOR 2.048 MHz

3

3

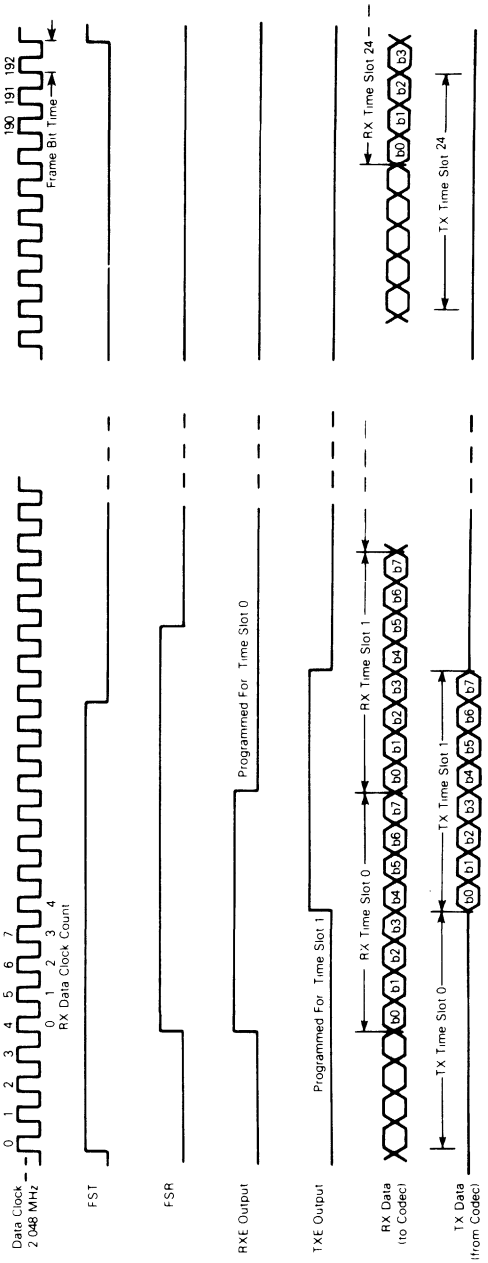


FIGURE 7 — DATA MULTIPLEX TIMING FOR 1.544 MHz

$\overline{PD}$ (Power Down Output — MC14416 Only) — The $\overline{PD}$ output is normally high. It is set high whenever b0 or b1 is a zero and the TSAC is programmed. If b0 and b1 are both one, then PD will be set low. This output is intended to be used to power down other circuitry in the channel unit when the channel unit is idle. This is a CMOS B series output which will drive one TTL LS load when V_{DD} is five volts.

OHI (Off Hook Input — MC14416 Only) — The OHI is a CMOS input with an internal pull-down resistor. A DC level at this pin will appear at the OHO output during the programmed TXE time slot.

$\overline{OHO}$ (Off Hook Output Inverted — MC14416 Only) — During the programmed transmit time slot, the data at OHI appears inverted at $\overline{OHO}$; otherwise $\overline{OHO}$ will be pulled high passively. The $\overline{OHO}$ output is an open drain N-channel transistor with a weak pull-up to V_{DD}. A number of these outputs can be wire ORed together to form a hook status bus consisting of a serial stream of hook information from a bank of channels. When the MC14416 powers down its codec, the TXE output is disabled; but the $\overline{OHO}$ output continues to multiplex out OHI and transmit time slot information during the previously entered transmit time slot.

V_{SS} — This is the most negative supply pin and digital ground for the package.

V_{DD} — This is the most positive supply. V_{DD} is typically 12 V with an operation range of 5 to 16 volts. All logic outputs swing the full supply voltage.

APPLICATIONS

The following section is intended to facilitate device understanding through several application examples. Included are Data Multiplex Timing Diagrams, a description of the TSAC Microprocessor port, a sample program, two circuit configurations using Motorola's devices, a systems drawing and two suggested clock circuits for obtaining codec data and control clocks.

In Figures 6 and 7 are shown Data Multiplex Timing Diagrams for 2.048 MHz and 1.544 MHz data clocks. The major points to be seen from these examples are:

1) Receive and transmit programming for the MC14418 are bit synchronous and word asynchronous. The MC14416 can be completely asynchronous.
2) The rising edges of FST and FSR initiate the programming frame for transmit and receive channels, respectively, and identify transmit and receive time slot "0," respectively.
3) Time slots identify eight data clock words. In this example: the transmit time slot is programmed as time slot "1." Therefore, bits 8 through 15 after FST are time slot "1."
4) For the 1.544 MHz clock, the framing bit is at the very end of the frame.

TSAC Microprocessor Port (MC14418 and MC14416) — The MC14418 provides four pins with 5-volt microprocessor input characteristics. These are AD, CS, CLK, and DI. The input supply for these inputs is V_{CC}. The CTS output is an open drain device with a weak pull up to V_{DD}. Typically, these five pins are bused in parallel to 24 or 32 TSACs per processor port. If desired, AD, CLK, DI, and CTS may be bused to greater than 32 TSACs by using the CS input as a group select. A microprocessor port of eight bits can thus control four groups of 32 TSACs with no additional decoding, as shown in Figure 8.

In order to program any given codec to a transmit or receive time slot, the processor simply exercises the corresponding 8-bit port.

Beginning with CS1 to CS4 low, all TSACs in the bank have their data registers in the Ready for Data Mode. The microprocessor takes the appropriate CS high and clocks in two bits of data into the 32 selected TSACs through DI and AD using CLK. The microprocessor presents data on the leading edge of CLK and the TSACs clock in data on the trailing edge of CLK. After eight CLK pulses (high, then low) the 32 selected TSACs will have two new 8-bit words; one in the data register through DI and one in the address register through AD. The unique TSAC, whose last 5 bits of the address register match its hardwired address on A1 through A5, acknowledges the new data. After the next FST, the selected TSAC will pull CTS low. This event notifies the processor that its transmission has been recognized. If CTS occurs at any other time, the processor can recognize the fault condition and restart the transmission using the reset function of the TSAC chip select. The uniquely selected TSAC will load its new program data into the appropriate TIME SLOT register on the next leading edge of FST. The bank of 32 TSACs will internally reset to the Ready for Data Mode when the transmission is completed, after the next FST. The TSAC, which was uniquely selected, and which has CTS low, will clear CTS to the pulled-up condition with the next FST. The processor may now program a new time slot immediately, with or without returning the selected CS low. Time Slot data can thus be sent at the rate of once every 256 μsec. for 8 kHz sampling (FST). The processor need not operate in an interrupt mode even though the TSAC's DC and CLK are asynchronous.

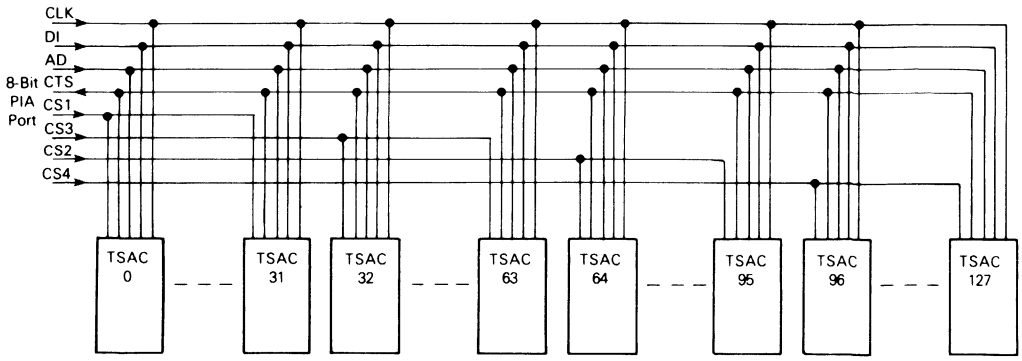
The processor port of the MC14416 works similarly to the MC14418, but will accept data if CS is high, and does not compare a hardwired address to the address word.

Figure 11 shows the typical signal timing for programming the microprocessor port.

To demonstrate the programming of the TSAC, consider the following configuration. A microprocessor is used to control four groups of thirty-two TSACs through an eight-bit PIA port. Four of the PIA lines are used for group select lines. The other four lines are dedicated to CLK, DI, AD, and CTS. The TSACs are programmed by serially loading bits into the DI and AD leads. Data bits are latched on the falling edge of CLK. The PIA port is connected as shown in Figure 9. The flow chart in Figure 10 and the following program illustrate one method of TSAC programming.

Before running the following program, the address, time slot, and group number must be entered in appropriate locations. During execution, CS (group select), AD, and DI words are arranged for serial presentation to the TSACs. The bits are presented with CLK high and are latched in with the falling edge of CLK. After eight passes through the loop, the TSAC is programmed, and CTS falls on the third data clock pulse after the next FST. The program waits for CTS to go high again before removing CS to prevent aborting the TSAC's programming. This program allows a maximum rate of programming equal to one TSAC per two frames.

FIGURE 8 — TYPICAL 8-BIT PORT



3

FIGURE 9 — PIA PORT ASSIGNMENT

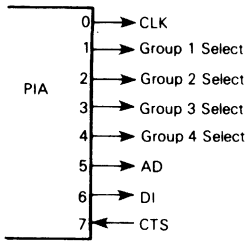
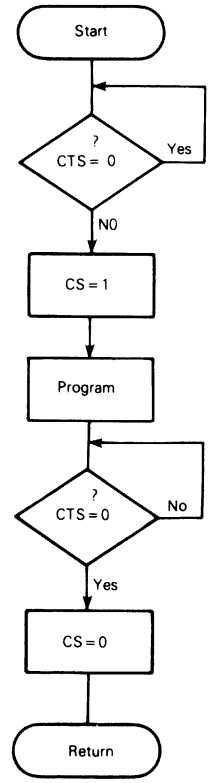


FIGURE 10 — TSAC PROGRAMMING FLOW CHART



Instructions for use:
Load in AD word (Q2, Q1, Q0, A5, A4, A3, A2, A1)
DI word (b0, b1, t6, t5, t4, t3, t2, t1)
group word
Start routine.

```
        LDAA GROUP      STORE GROUP # IN ACCA
        DECA            CHECK IF EQ. TO ONE
        BNE ONE         IF NOT GO TO NEXT TEST
        LDAB #03        EQUALS ONE
        STAB SELECT     LOAD PROPER SELECT BITS IN SELECT WORD
        BRA START       JUMP TO NEXT PART
ONE     DECA            IS GROUP EQ. TO TWO?
        BNE TWO         IF NOT GO TO NEXT TEST
        LDAB #05        LOAD PROPER SELECT BITS IN SELECT WORD
        STAB SELECT
        BRA START       JUMP TO NEXT PART
TWO     DECA            CHECK IF EQ. TO THREE
        BNE THREE       IF NOT IS EQ. TO FOUR
        LDAB #09        LOAD PROPER SELECT BITS IN SELECT WORD
        STAB SELECT
        BRA START       JUMP TO NEXT PART
THREE   LDAB #11        LOAD GROUP SELECT BITS FOR GROUP FOUR
        STAB SELECT
START   LDAA #00        INITIALIZE PIA
        STAA CONTRLB    INITIALIZE PIA
        LDAA #7F        INITIALIZE PIA
        STAA DDRB       INITIALIZE PIA
        LDAA #04        INITIALIZE PIA
        STAA CONTRLB    INITIALIZE PIA
        LDAB #80        TEST FOR CTS HIGH
WAIT    BITB PIAOUT     WAIT FOR CTS HIGH
        BEQ WAIT
        LDAA #01        NOW CTS IS HIGH, SET CLK HI AND LEAVE CS LOW
        STAA PIAOUT
        LDAA #08        INITIALIZE LAP COUNTER
        STAA COUNTER
        LDX 00          MOVE AD AND DI INPUTS
        STX 02          TO SHIFT LOCATIONS
        LDAA SELECT     BRING CS HIGH
        STAA PIAOUT
LOOP    LDAA SELECT     START BIT STUFFING
        ROL 0002        CHECK AD WORD
        BCC 02          CHECK AD WORD
        ORAA 20         CHECK AD WORD
        ROL 0003        CHECK DI WORD
        BCC 02          CHECK DI WORD
        ORAA 40         CHECK DI WORD
        STAA PIAOUT     WRITE BITS TO TSAC
        DECA            WRITE FALLING EDGE OF CLK
        NOP             WRITE FALLING EDGE OF CLK
        NOP             WRITE FALLING EDGE OF CLK
        STAA PIAOUT     WRITE FALLING EDGE OF CLK
        DEC COUNTER     DECREMENT LAP COUNTER
        BNE LOOP        TEST FOR LOOP COMPLETION
        LDAB #80        TEST AND WAIT FOR CTS LOW
ISITLO  BITB PIAOUT     TEST AND WAIT FOR CTS LOW
        BNE ISITLO      TEST AND WAIT FOR CTS LOW
        CLR PIAOUT      REMOVE CS (GROUP SELECT)
        RTS             RETURN FROM SUBROUTINE
```

3

FIGURE 11 — MICROPROCESSOR PORT TIMING

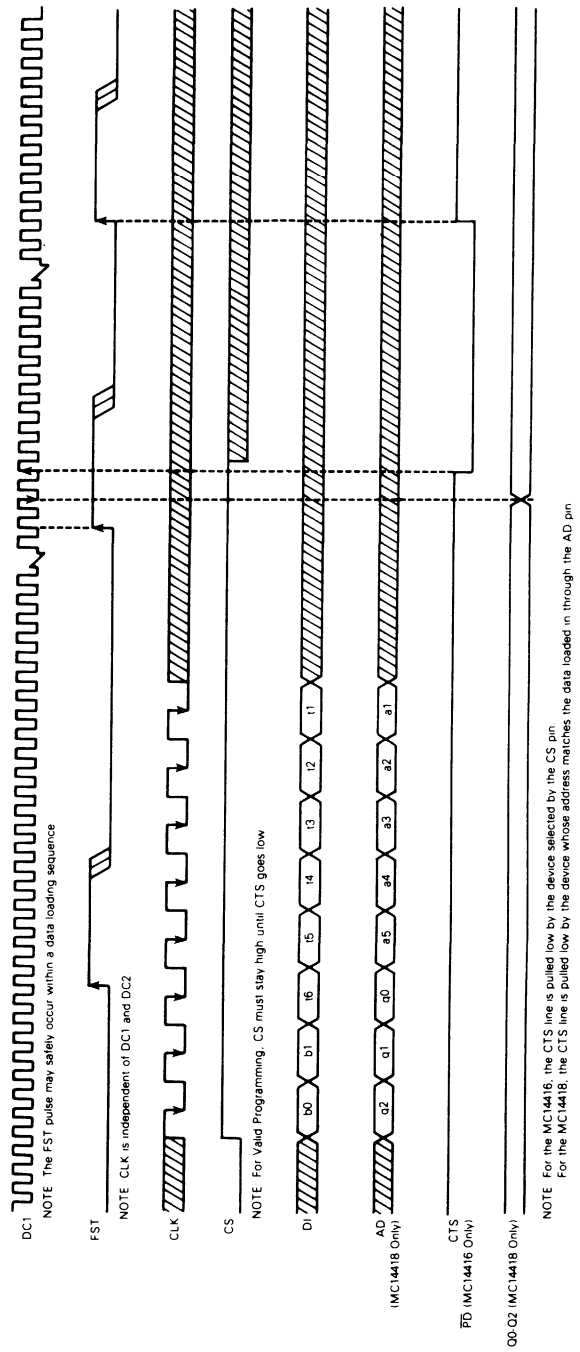
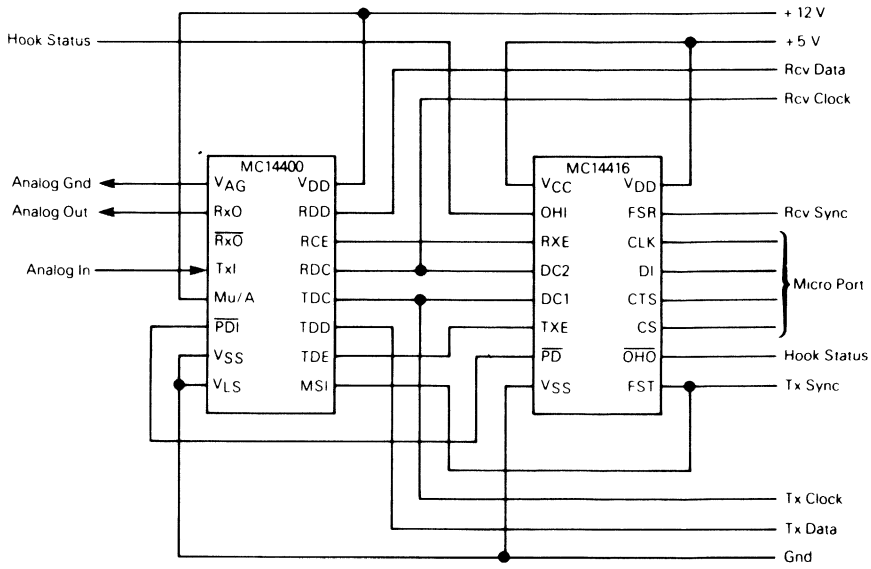


FIGURE 12 – TYPICAL CIRCUIT CONFIGURATION USING MC14416 IN CONJUNCTION WITH MC14400



3

3

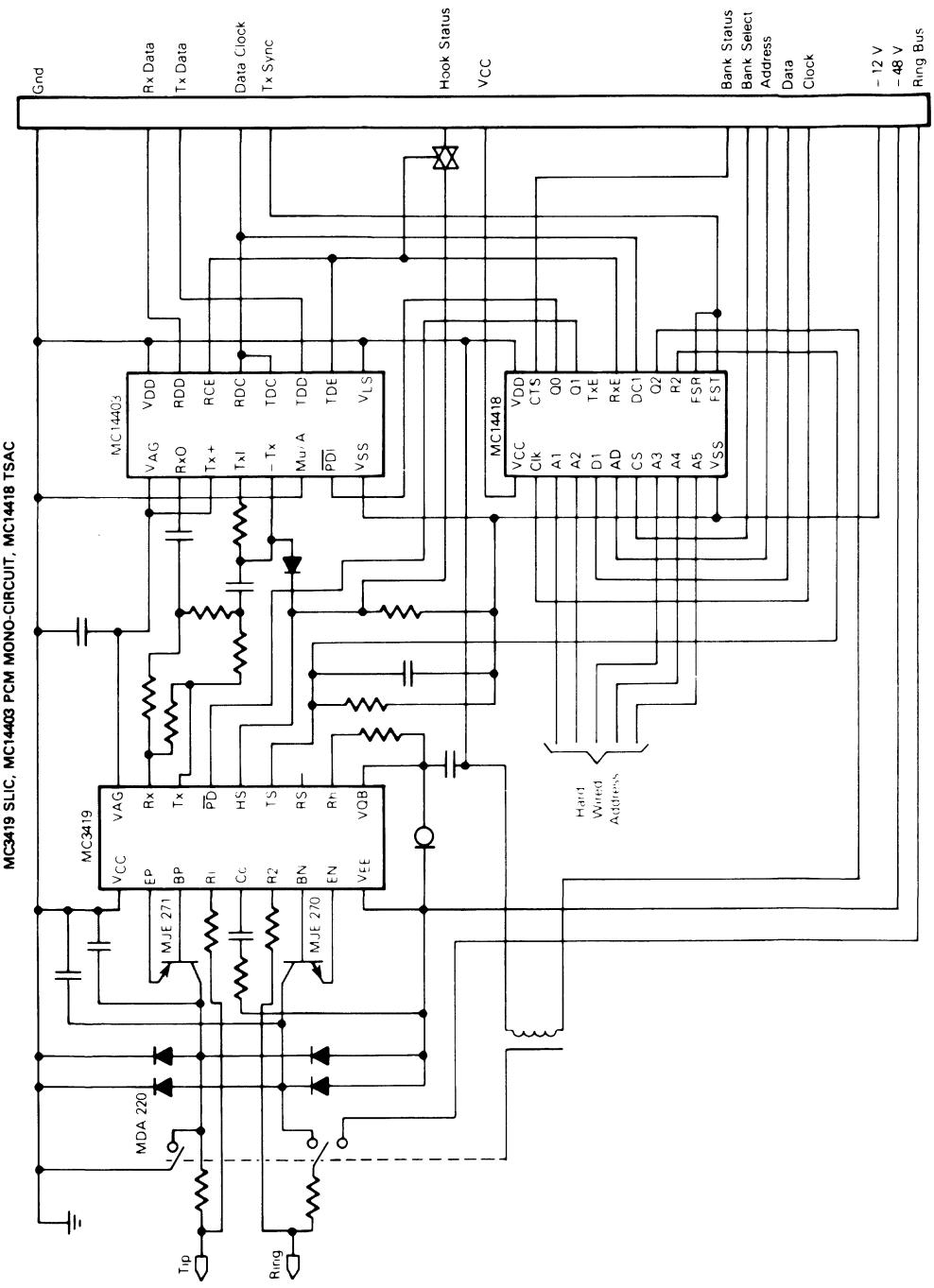
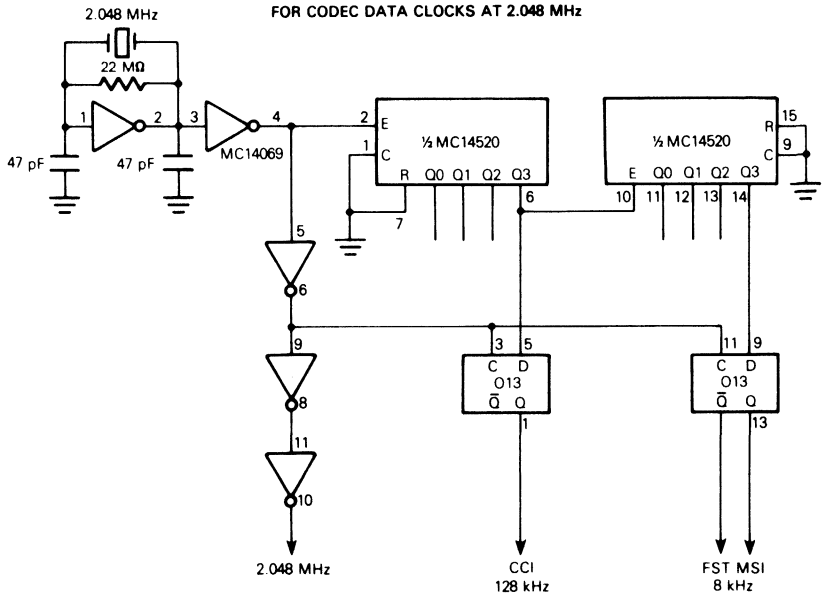
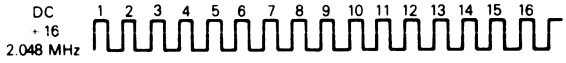
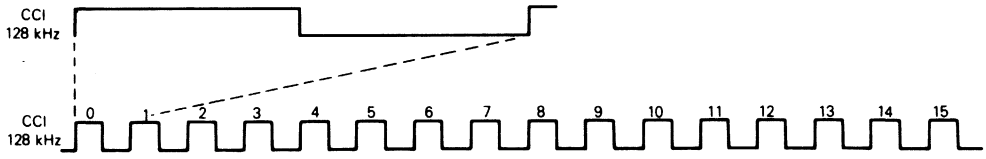


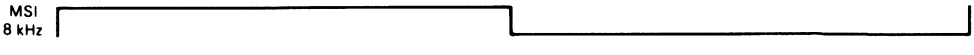
FIGURE 13 — A COMPLETE SINGLE PARTY CHANNEL UNIT USING MC3419 SLIC, MC14403 PCM MONO-CIRCUIT, MC14418 TSAC

FIGURE 14 – CLOCK CIRCUIT AND TIMING
FOR CODEC DATA CLOCKS AT 2.048 MHz









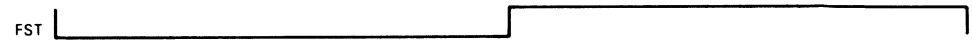
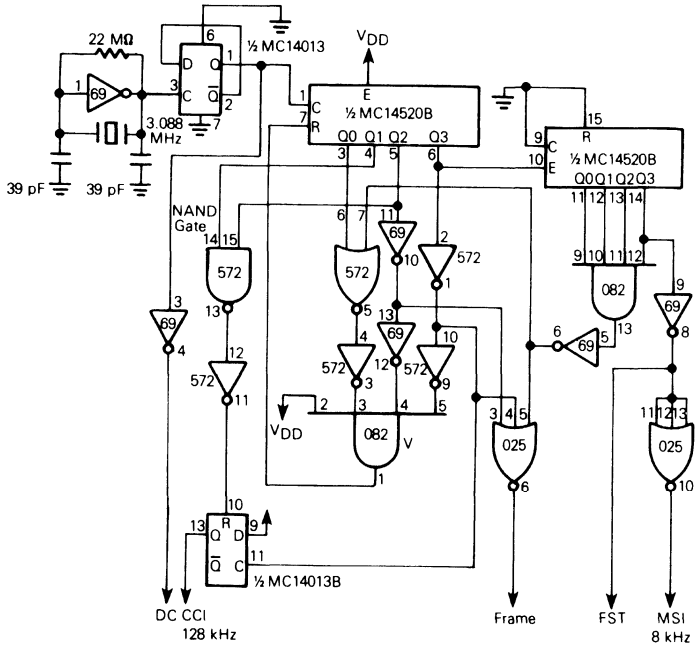
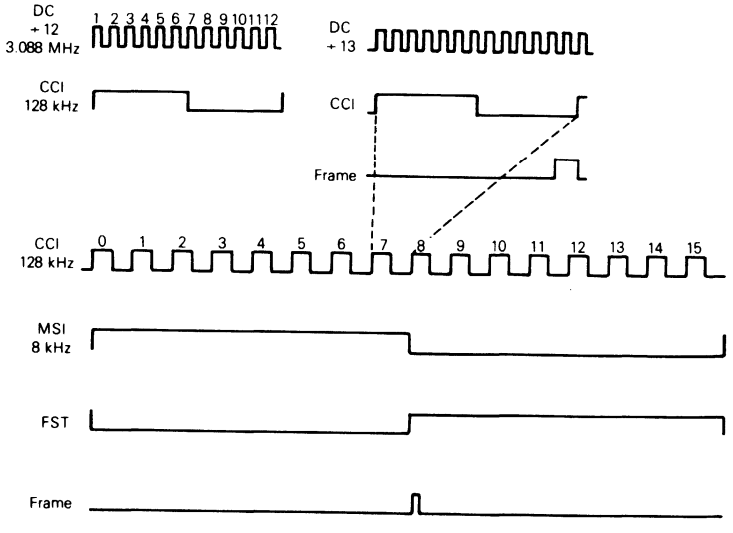


FIGURE 15 – CLOCK CIRCUIT AND TIMING
FOR CODEC DATA CLOCKS AT 1.544 MHz





MOTOROLA

MC14417

CMOS LSI
(LOW-POWER COMPLEMENTARY MOS)

TSAC
TIME SLOT ASSIGNER CIRCUIT

3

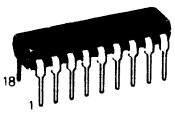
BASIC TIME SLOT ASSIGNER CIRCUIT (TSAC)

The MC14417 is a per channel Time Slot Assigner Circuit (TSAC) that produces 8-bit receive and transmit time slots for a PCM Codec. The pins D0 to D5 are the time slot data inputs which can be either hard-wired on the printed circuit board for fixed time slot assignment, or externally programmed through the use of these pins and the latch enable function. The receive and transmit frame syncs and enables are independent. In addition, a T/R (TXE/RXE swap) input is provided which allows a simplified switching mechanism for a small systems architecture (i.e., key systems).

The MC14417 can operate from a single 5-volt supply for TTL levels or up to 16-volts for CMOS levels. The MC14417 is fabricated using the CMOS technology for reliable low-power performance.

- TTL and CMOS Level Compatibility
- 5 to 16 Volt Operation
- Low Operating Power Consumption
- For Use With Up to 2.56 MHz Clocks
- Independent Transmit and Receive Frame Syncs and Enables
- Up to 64 Time Slots Per Frame
- Compatible with MC14400/01/02/03/05 PCM Mono-Circuits
- Allows Swapping of Transmit Enable (TXE) and Receive Enable (RXE) Signals
- CMOS Metal Gate for High Reliability

L SUFFIX
CERAMIC PACKAGE
CASE 726

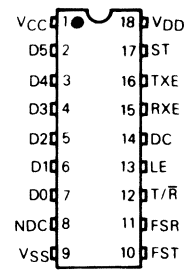


P SUFFIX
PLASTIC PACKAGE
CASE 707

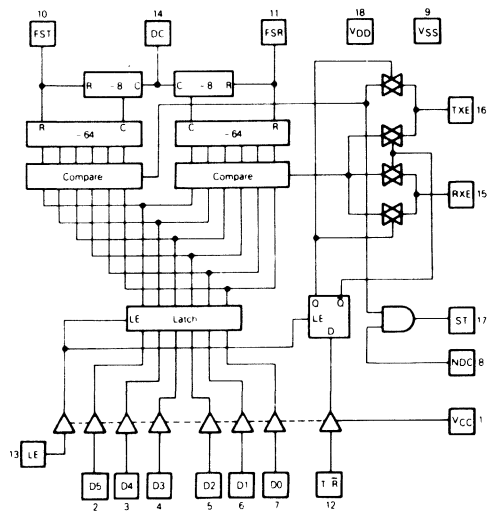
ORDERING INFORMATION

MC14XXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package

PIN ASSIGNMENT



BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

DS9891

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to 18	V
Level Shift Voltage	V_{CC}	−0.5 to V_{DD}	V
Input Voltage Inputs Referenced to V_{DD} to V_{CC}	 V_{in1} V_{in2}	 −0.5 to V_{DD} + 0.5 −0.5 to V_{DD} + 0.5	V
DC Current Drain per Pin	I	10	mA
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +165	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

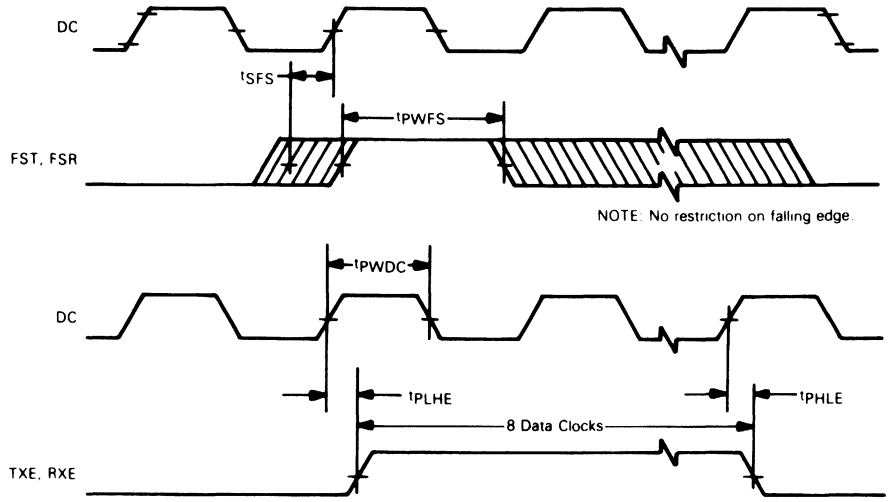
Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
DC Supply Voltage, V_{SS} = 0 V	V_{DD}	–	4.5	12	16	V
DC Supply Voltage, V_{SS} = 0 V	V_{CC}	–	4.5	5	V_{DD}	V
Output Current TXE, RXE, ST (V_{OL} = 0.4 V) (V_{OL} = 1.0 V)	I_{OL}	 5 12	 0.51 2.0	 – 4.0	 – –	mA
(V_{OH} = 4.6 V) **(V_{OH} = 11.0 V)**	I_{OH}	5 12	−0.2 −2.0	– −4.0	– –	mA
Input Voltage (CMOS) FST, FSR, DC1, DC2, NDC "0"	V_{IL}	5 12	– –	– –	1.0 2.4	V
"1"	V_{IH}	5 12	4.0 9.6	– –	– –	V
Input Voltage (TTL) D0-D5, LE, T/$\overline{R}$, V_{CC} = 5 V "0"	V_{IL}	5 12 16	– – –	– – –	0.8 0.8 0.7	V
"1"	V_{IH}	5 12	2.0 2.0	– –	– –	V
Total Supply Current (Outputs Unloaded) DC1 at 2.048 MHz	I_T	5 12	– –	1.5 2.5	– –	mA

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C, Unless Otherwise Noted)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time, TXE, RXE, ST	t_r	5 12	– –	100 50	200 100	ns
Output Fall Time, TXE, RXE, ST	t_f	5 12	– –	100 50	200 100	ns
Frame Sync Setup Time (See Figure 1)	t_{SFS}	5 12	−150 −75	– –	+150 +75	ns
Frame Sync Pulse Width	t_{PWFS}	5 12	200 100	– –	– –	ns
Propagation Delay (Note 1) DC1 to TXE, DC2 to RXE, C_L = 20 pF	t_{PHLE}, t_{PLHE}	5 12	– –	130 80	180 125	ns
Data Clock Frequency	f_{DC}	5 12	– –	– –	2.048 2.6	MHz
Data Clock Pulse Width at f_{DC} (Max)	t_{PWDC}	5 12	200 140	244 192	293 260	ns
LE Pulse Width	t_{PWLE}	5 12	1 1	– –	– –	µs
NDC to ST Propagation Delay		5 12	– –	– –	120 80	ns
FST to ST Propagation Delay		5 12	– –	– –	200 130	ns

NOTE 1: For time slot 0, t_{PHLE} and t_{PLHE} are measured from the leading edge of DC or FST (FSR), whichever occurs last.

FIGURE 1 – TIMING DIAGRAMS



PIN DESCRIPTIONS

V_{CC} (Positive Supply) – The V_{CC} power supply controls the inputs LE, D0-D5 and T/$\overline{R}$. It can be supplied by any voltage from 4.5 to V_{DD}. In typical usage, V_{CC} is 5 volts for TTL or microprocessor compatibility of the control inputs to the TSAC while V_{DD} and V_{SS} are connected to the Codec supplies.

D5-D0 (Parallel Time Slot Data Inputs) – The six inputs to the input-storage latch are the time-slot data. D0 is the least-significant bit while D5 is the most-significant. The binary word at this input represents the number of 8 bit time slots from FST and FSR where TXE and RXE will occur, respectively. These can be 5-volt input compatible with TTL and are internally level shifted to the V_{DD} supply.

LE (Latch Enable Input with Internal Pull-Up) – This input allows the data D0 through D5 and T/$\overline{R}$ bits to be latched in the input-storage latch. If LE is held high, then the inputs to the latch are combinational and directly applied to the compare circuits. When LE is pulled low, the input values applied at D0 through D5 and T/$\overline{R}$ are latched and held in the storage latch.

T/$\overline{R}$ (TXE/RXE Swap Input with Internal Pull-Up) – This input allows the TXE and RXE inputs to be swapped. When T/$\overline{R}$ is a one, the TXE output is derived from FST and RXE from FSR. If T/$\overline{R}$ is a zero, the derivation is reversed. If FST and FSR are eight data clocks apart, then two TSAC channels programmed to the same D0 through D5 and different T/$\overline{R}$ bits will create a completed conversation. This feature is intended for use in simplifying small-key systems.

DC (Data Clock Input) – The data clock input establishes the bit rate for the TSAC. This is typically 1.544 or 2.048 MHz but can be any frequency up to 2.56 MHz. The data clock is divide-by-8 for both transmit- and receive-time slots. The data clock input is a CMOS compatible input between V_{DD} and V_{SS}.

FST (Frame Sync Transmit Input) – This input identifies the beginning of the zero-transmit time slot by resetting the divide-by-8 and divide-by-64 counters. FST is a CMOS compatible input between V_{DD} and V_{SS}. The TXE output will begin and end on one 8-bit word boundary which is synchronized with the FST input. The FST signal should be aligned with the leading edge of data clock and is typically 8 kHz.

FSR (Frame Sync Receive Input) – The FSR input provides the same functions for the RXE output as FST did for TXE. The FSR and FST inputs can be any number of data clocks different, or can be the same.

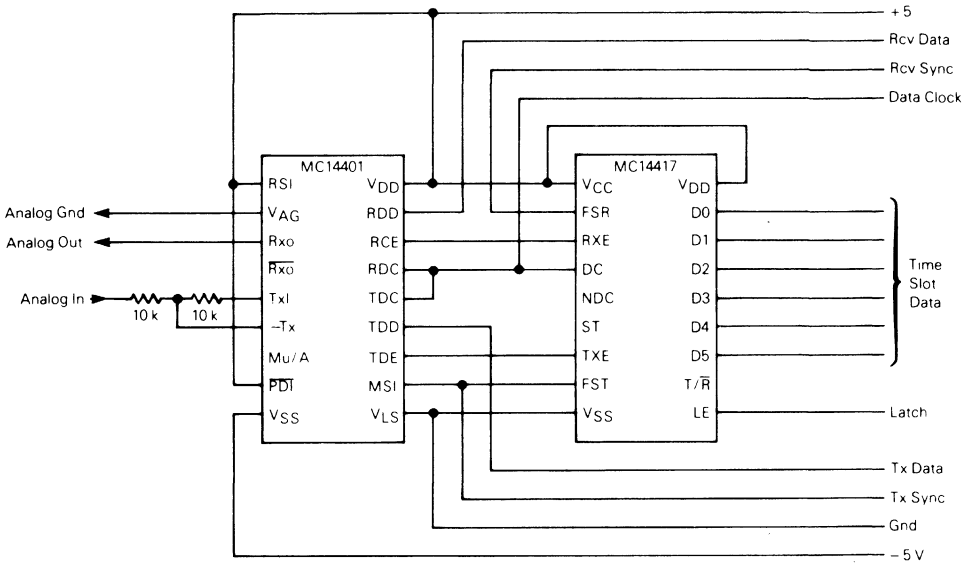
TXE, RXE (Transmit-Enable and Receive-Enable Outputs) – These outputs are used to control the transmitting and receiving of data words to and from Codecs. Each output swings from V_{DD} to V_{SS} and is eight data clocks long. TXE and RXE go high at the beginning of the programmed time slot and low at the end. TXE is derived from FST and RXE is derived from FSR, provided the T/$\overline{R}$ bit is high.

ST (Strobe Output) – The strobe output is provided to allow simplified input data storage or off-hook multiplexing control. ST is the logical AND of an enable signal (NDC) and the TXE time slot period. Thus, ST can only be high during a programmed TXE time slot. Since no other TSAC in a bank can have the same TXE programming, the ST output on any TSAC can be used to uniquely identify that TSAC by a pulse input on NDC. In many applications ST is used to control the LE input.

NDC (New Data Clock Input with Internal Pull-Up) – This input can be used in conjunction with ST to strobe data into a TSAC bank. NDC can be used to enable the strobe output.

V_{DD}, V_{SS} – The TSAC will operate from any single supply from 4.5 to 16 volts. The TSAC can be used in a 5-volt-only system by making both V_{CC} and V_{DD} 5 volts.

FIGURE 2 – MOTOROLA MONO-CIRCUIT/TSAC COMBINATIONS



The MC14417 TSAC offers simple flexible time slot assignment for the PCM mono-circuit. Assignments are wired or latched into the data port. The MC14401 offers supply flexibility of ±5, ±6, +12, or +10 V with 18 pin packages and TTL compatibility.

MOTOROLA

MC14419

2-OF-8 KEYPAD-TO-BINARY ENCODER

The MC14419 is designed for phone dialer system applications, but finds many applications as a keypad-to-binary encoder. The device contains a 2-of-8 to binary encoder, a strobe generator, and an illegal state detector. The encoder has four row inputs and four column inputs, and is designed to accept inputs from 16 keyswitches arranged in a 4 × 4 matrix. For an output on the four data lines, one and only one row along with one and only one column input line must be activated. All other combinations are suppressed by the illegal state detector to eliminate false data output.

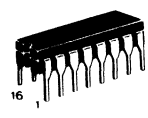
The strobe generator produces a strobe pulse when any of the 10 keys corresponding to numerals 0 through 9 are depressed. The strobe output can be used to eliminate erroneous data entry due to contact bounce. For a strobe output to occur, the key row and column input lines must remain stable for 80 clock pulses after activation. When the contact bounce has settled and 80 clock pulses have occurred, the output will be a single strobe pulse equal in width to that of the clock low state. The strobe generator will output one and only one pulse each time a numerical key is depressed. After the pulse has occurred, noise and bounce due to contact break will not cause another strobe pulse. With a 16 kHz input clock frequency, the pulse occurs 5 ms after the last bounce.

- Suppressed Output for Illegal Input Codes
- On-Chip Pullup Resistors for Row and Column Inputs
- Clock Input Conditioning Circuit
- Low Current Drain in Standby Mode
  5.0μA Typical @ 5.0 Vdc
- Subsystem Complement to the MC14408/14409 Phone Pulse Converter
- Codes for Numbers 0-9 Produce a Strobe Pulse
- One Key Rollover Feature

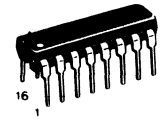
CMOS
(LOW-POWER COMPLEMENTARY MOS)

2-OF-8 KEYPAD-TO-BINARY ENCODER

3



L SUFFIX
CERAMIC PACKAGE
CASE 620



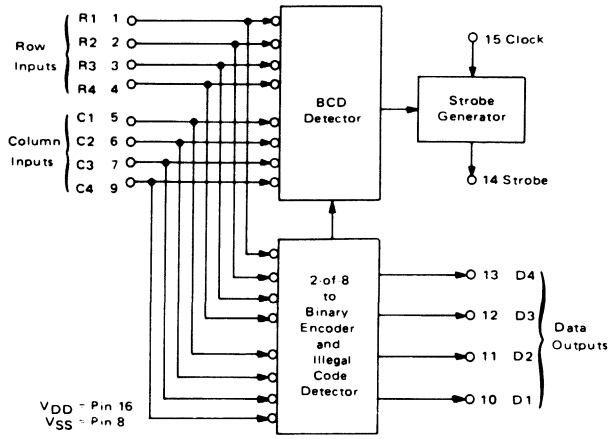
P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

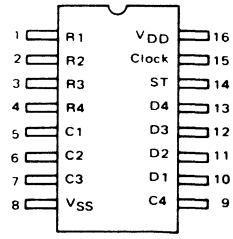
MC14XXX_

Suffix Denotes
L = Ceramic
P = Plastic

BLOCK DIAGRAM



PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

DS9892

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	+6.0 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} + 0.5 to V_{SS} -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

3

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	-40°C Min	-40°C Max	25°C Min	25°C Typ	25°C Max	+85°C Min	+85°C Max	Unit
Supply Voltage Operating Range	V_{DD}	–	3.0	6.0	3.0	5.0	6.0	3.0	6.0	Vdc
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
Output Voltage "1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
Noise Immunity ($\Delta V_{out} \leq 0.8$ Vdc)	V_{NL}	5.0	1.5	–	1.5	2.25	–	1.4	–	Vdc
	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source	I_{OH}	5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	mAdc
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
Input Leakage Current ($V_{in} = V_{DD}$)	I_{IH}	5.0	–	–	–	10	–	–	–	pAdc
Pullup Resistor Source Current (Row and Column Inputs) ($V_{in} = V_{SS}$)	I_{IL}	5.0	265	460	190	250	330	125	215	μAdc
Input Capacitance ($V_{in} = V_{SS}$)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Standby Supply Current (f_{clock} = 16 kHz, No Keys Depressed)	I_{DDS}	3.0	–	3.0	–	1.0	3.0	–	6.0	μAdc
		5.0	–	15	–	5.0	15	–	30	
		6.0	–	60	–	20	60	–	120	
Standby Supply Current as a Function of Clock Frequency* (No Keys Depressed)	I_{DDS}	5.0	I_{DDS} = 0.09 μA/kHz + 3.0 μA							μAdc

*The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise and Fall Times, D1 thru D4 (Figure 1)	t_r, t_f	5.0	–	300	–	ns
Propagation Delay Time, Row or Column Input to Data Output (Figure 1)	t_{PLH}, t_{PHL}	5.0	–	1000	–	ns
Clock Pulse Frequency Range	PRF	3.0 to 6.0	4.0	16	80	kHz

FIGURE 1 – SWITCHING TIME WAVEFORMS

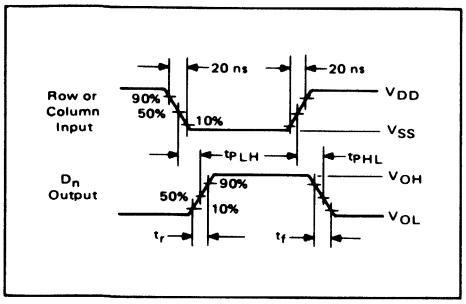


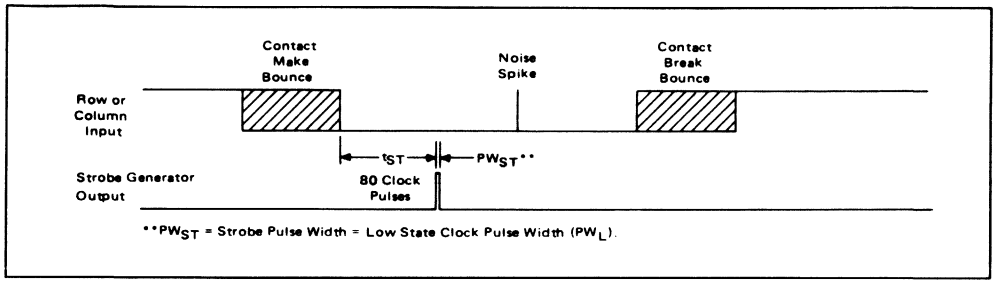
FIGURE 2 – TYPICAL STROBE PULSE DELAY TIMES

PRF Clock Frequency kHz	t_{ST}* Strobe Pulse Delay Time ms
4.0	20
8.0	10
16	5.0
32	2.5
80	1.0

*t_{ST} = (1/PRF) • 80, with PRF in kHz, t_{ST} in ms.

3

FIGURE 3 – STROBE GENERATOR TIMING DIAGRAM



**PW_{ST} = Strobe Pulse Width = Low State Clock Pulse Width (PW_L).

TRUTH TABLE

	Inputs								Outputs				
	Row				Column								
Key**	R4	R3	R2	R1	C4	C3	C2	C1	D4	D3	D2	D1	Strobe
1	1	1	1	0	1	1	1	0	0	0	0	1	
2	1	1	1	0	1	1	0	1	0	0	1	0	
3	1	1	1	0	1	0	1	1	0	0	1	1	
A	1	1	1	0	0	1	1	1	1	1	0	0	0
4	1	1	0	1	1	1	1	0	0	1	0	0	
5	1	1	0	1	1	1	0	1	0	1	0	1	
6	1	1	0	1	1	0	1	1	0	1	1	0	
B	1	1	0	1	0	1	1	1	1	1	0	1	0
7	1	0	1	1	1	1	1	0	0	1	1	1	
8	1	0	1	1	1	1	0	1	1	0	0	0	
9	1	0	1	1	1	0	1	1	1	0	0	1	
C	1	0	1	1	0	1	1	1	1	1	1	0	0
*	0	1	1	1	1	1	1	0	1	0	1	0	0
0	0	1	1	1	1	1	0	1	0	0	0	0	
#	0	1	1	1	1	0	1	1	1	0	1	1	0
D	0	1	1	1	0	1	1	1	1	1	1	1	0
	All Other Combinations								0	0	0	0	0

**See Figure 4 for keypad designation.

FIGURE 4 – TYPICAL KEYPAD INTERFACE APPLICATION

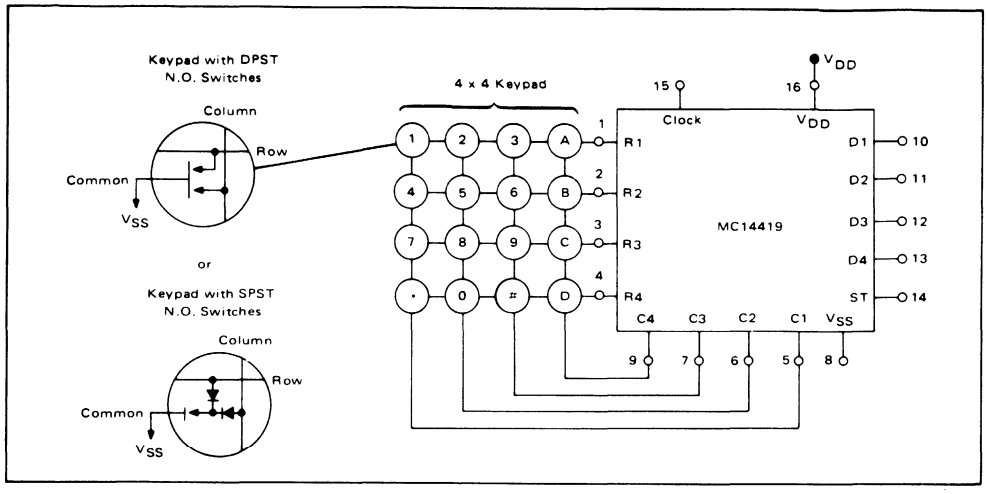
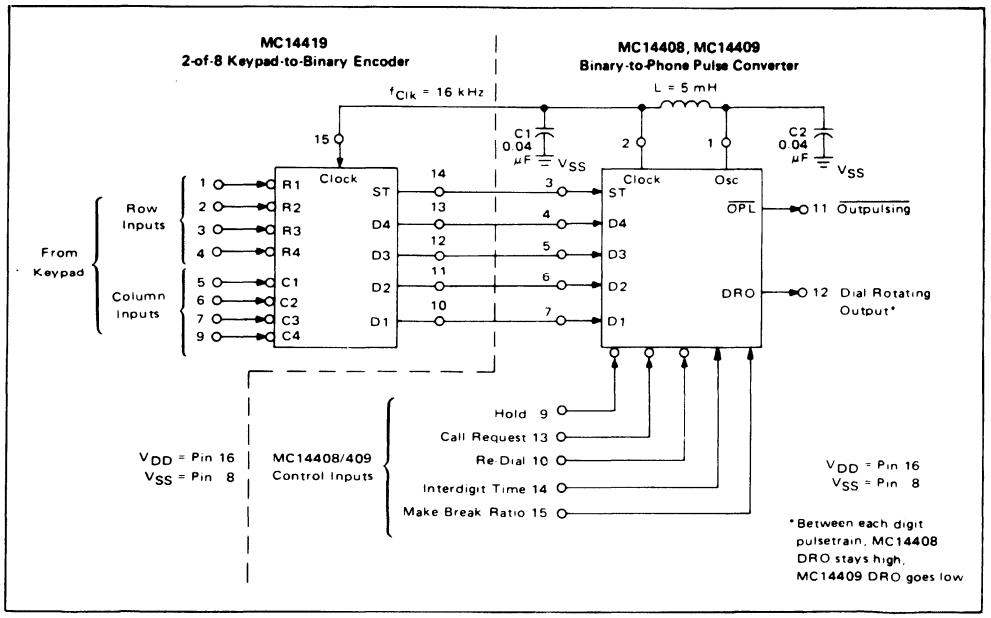


FIGURE 5 – PHONE DIALER SYSTEM



MOTOROLA

MC34010

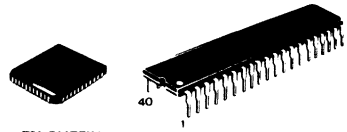
Advance Information

ELECTRONIC TELEPHONE CIRCUIT

- Provides All Basic Telephone Station Apparatus Functions in a Single IC, Including DTMF Dialer, Tone Ringer, Speech Network and Line Voltage Regulator
- DTMF Generator Uses Low-Cost Ceramic Resonator with Accurate Frequency Synthesis Technique
- Tone Ringer Drives Piezoelectric Transducer and Satisfies EIA RS-470 Impedance Signature Requirements
- Speech Network Provides Two–Four Wire Conversion with Adjustable Sidetone Utilizing an Electret Transmitter
- On-Chip Regulator Insures Stable Operation Over Wide Range of Loop Lengths
- I^2L Technology Provides Low 1.4 Volt Operation and High Static Discharge Immunity
- Microprocessor Interface Port for Automatic Dialing Features

ELECTRONIC TELEPHONE CIRCUIT

BIPOLAR LINEAR/I^2L

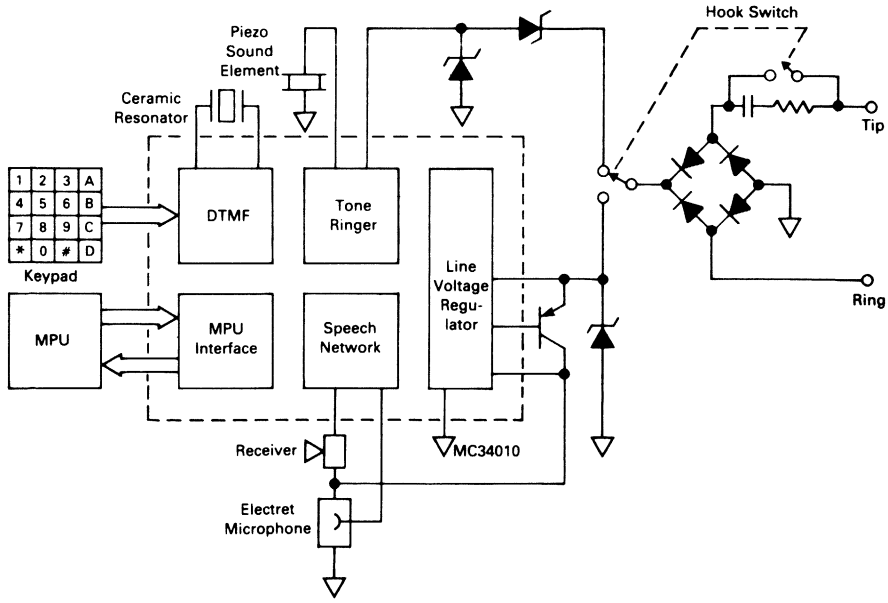


FN SUFFIX
44-PIN
PLCC
CASE 777-01

P SUFFIX
PLASTIC PACKAGE
CASE 711-03

3

FIGURE 1 — ELEMENTS OF THE ELECTRONIC TELEPHONE



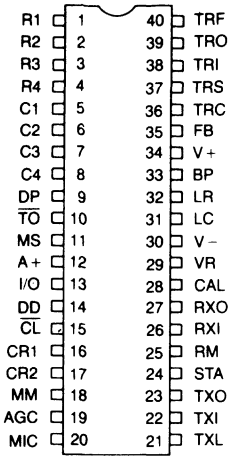
This document contains information on a new product. Specifications and information herein are subject to change without notice.

ADI1386

MAXIMUM RATINGS (Voltage References to V−)

Parameter	Value	Unit
V+ Terminal Voltage (Pin 34)	+20, −1.0	V
VR Terminal Voltage (Pin 29)	+2.0, −1.0	V
RXO Terminal Voltage (Pin 27)	+2.0, −1.0	V
TRS Terminal Voltage (Pin 37)	+35, −1.0	V
TRO (With Tone Ringer Inactive) Terminal Voltage	+2.0, −1.0	V
R1–R4 Terminal Current (Pins 1–4) C1–C4 (Pins 5–8)	±100	mA
$\overline{CL}$, $\overline{TO}$, DD, I/O, A+	+122, −1.0	V
Operating Ambient Temperature Range	−20 to +60	°C
Storage Temperature Range	−65 to +150	°C

PIN CONNECTIONS



3

GENERAL CIRCUIT DESCRIPTION

Introduction

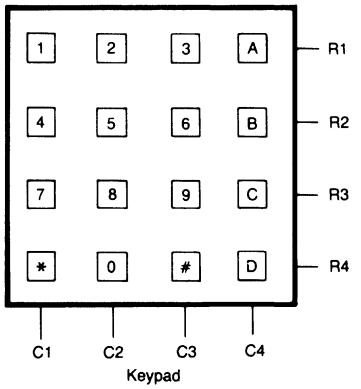
The MC34010 Electronic Telephone Circuit (ETC) provide all the necessary elements of a tone dialing telephone in a single IC. The functional blocks of the ETC include the DTMF dialer, speech network, tone ringer, and dc line interface circuit (Figure 1). The MC34010 also provides a microprocessor interface port that facilitates automatic dialing features.

Low voltage operation is a necessity for telephones in networks where parallel telephone connections are common. An electronic speech network operating in parallel with a conventional telephone may receive line voltages below 2.5 volts. DTMF dialers operate at similarly low-line voltages when signaling through battery powered station carrier equipment. These low voltage requirements have been addressed by realizing the MC34010 in a bipolar/I^2L technology with appropriate circuit techniques. The resulting speech and dialer circuits maintain specified performance with instantaneous input voltage as low as 1.4 volts.

Line Voltage Regulator

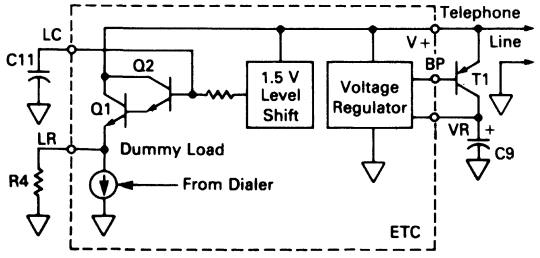
The dc line interface circuit (Figure 3) determines the dc input characteristic of the telephone. At low input voltages (less than 3 volts) the ETC draws only the

FIGURE 2 — MPU INTERFACE CODES



Key	Row	Column	Code (B3–B0)
1	1	1	1111
2	1	2	0111
3	1	3	1011
4	2	1	1101
5	2	2	0101
6	2	3	1001
7	3	1	1110
8	3	2	0110
9	3	3	1010
0	4	2	0100
A	1	4	0011
B	2	4	0001
C	3	4	0010
D	4	4	0000
*	4	1	1100
#	4	3	1000

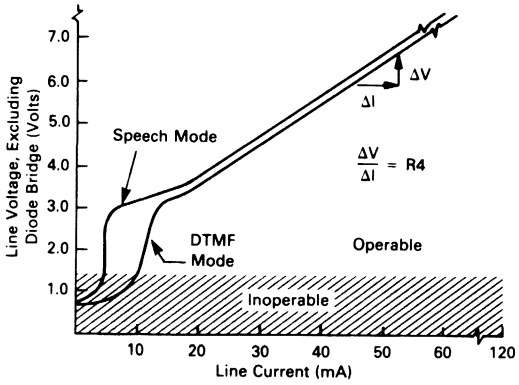
FIGURE 3 — DC LINE INTERFACE BLOCK DIAGRAM



GENERAL CIRCUIT DESCRIPTION (continued)

speech and dialer bias currents through the VR regulator. As input voltage increases, Q1 conducts the excess dc line current through resistor R4. The 1.5 volt level shift prevents saturation of Q2 with telephone line signals up to 2.0 volts peak (+5.2 dBm). A constant current (dummy load) is switched off when the DTMF dialer is activated to reduce line current transients. Figure 4 illustrates the dc voltage/current characteristic of an MC34010 telephone.

FIGURE 4 — DC V-I CHARACTERISTIC OF THE ETC



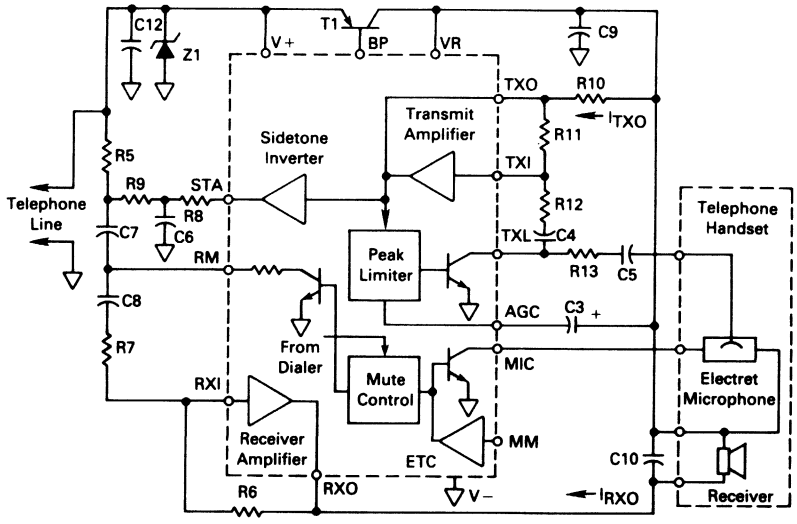
Speech Network

The speech network (Figure 5) provides the two-to-four wire interface between the telephone line and the instrument's transmitter and receiver. An electret microphone biased from VR drives the transmit amplifier. For very loud talkers, the peak limiter circuit reduces the transmit input level to maintain low distortion. The transmit amplifier output signal is inverted at the STA terminal and driven through an external R-C network to control the receiver sidetone level. The switched ac resistance at the RM terminal reduces receiver signal when dialing and suppresses clicks due to hook or keypad switch transitions. When transmitting, audio signal currents (i_{TXO} and i_{RXO}) flow through the voltage regulator pass transistor (T1) to drive the telephone line. This feature has two consequences: 1) In the transmitting mode the receiver sidetone current i_{RXO} contributes to the total signal on the line along with i_{TXO}; 2) The ac impedance of the telephone is determined by the receiver impedance and the voltage gain from the line to the receiver amplifier output.

DTMF Dialer

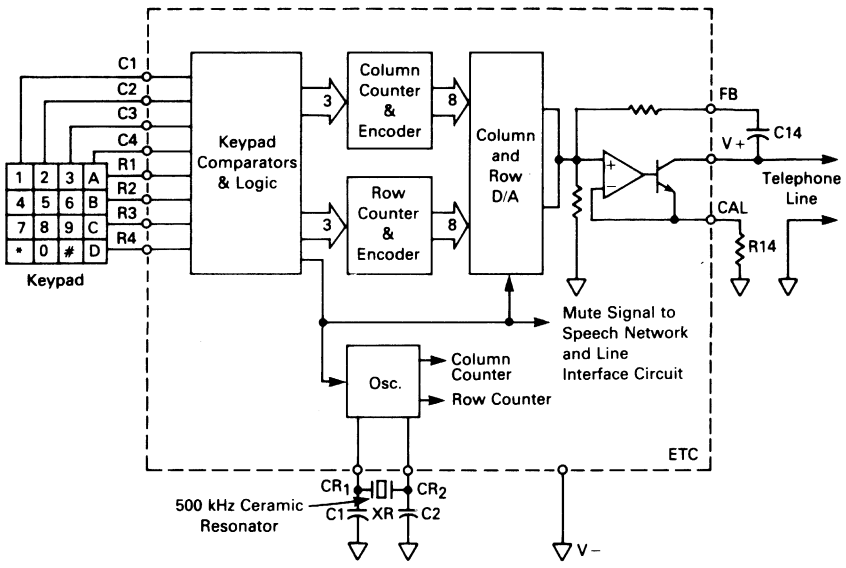
Keypad interface comparators activate the DTMF row and column tone generators (Figure 6) when a row and column input are connected through a SPST keypad. The keypad interface is designed to function with contact resistances up to 1.0 kΩ and leakage resistances as low as 150 kΩ. Single tones may be initiated by depressing two keys in the same row or column.

FIGURE 5 — SPEECH NETWORK BLOCK DIAGRAM



The programmable counters employ a novel design to produce non-integer frequency ratios. The various DTMF tones are synthesized with frequency division errors less than ±0.16% (Table 1). Consequently an inexpensive ceramic resonator can be used instead of a quartz crystal as the DTMF frequency reference. Total frequency error less than ±0.8% can be achieved with ±0.3% ceramic resonator. The row and column D/A converters produce 16-step approximations of sinusoidal waveforms. Feedback through terminal FB reduces the DTMF output impedance to approximately 2.0 kΩ to satisfy return loss specifications.

FIGURE 6 — DTMF DIALER BLOCK DIAGRAM



Tone Ringer

The tone ringer (Figure 7) generates a warbling square wave output drive to a piezo sound element when the ac line voltage exceeds a predetermined threshold level. The threshold detector uses a current mode comparator to prevent on/off chatter when the output current reduces the voltage available at the ringer input. When the average current into the tone ringer exceeds the threshold level, the ringer output TRO commences driving the piezo transducer. This output current sourced from TRI increases the average current measured by the threshold detector. As a result, hysteresis is produced beween the tone ringer on and off thresholds. The output frequency at TRO alternates between $f_O/8$ and $f_O/10$ at a warble rate of $f_O/640$, where f_O is the ringer oscillator frequency.

Microprocessor Interface

The MPU interface connects the keypad and DTMF sections of the ETC to a microprocessor for storing and retrieving numbers to be dialed. Figure 8 shows the major blocks of the MPU interface section and the interconnections between the keypad interface, DTMF generator and microprocessor. Each button of a 12 or 16 number keypad is represented by a four-bit code (Figure 2). This four-bit code is used to load the programmable counters to generate the appropriate row and column tones. The code is transferred serially to or from the microprocessor when the shift register is clocked by the microprocessor. Data is transferred through the I/O terminal, and the direction of data flow is determined by the Data Direction (DD) input terminal. In the manual dialing mode, DD is a Logic "0" and the four-bit code from the keypad is fed to the DTMF generator by the digital multiplexer and also output on the I/O terminal through the four-bit shift register. The data sequence on the I/O terminal is B3, B2, B1, B0 and is transferred on the negative edge of the clock input ($\overline{CL}$). In this mode the shift register load enable circuit cycles the register between the load and read modes such that multiple read cycles may be run for a single-key closure. Six complete clock cycles are required to output data from the ETC and reload the register for a second look.

In the automatic dialing mode, DD is a Logic "1" and the four-bit code is serially entered in the sequence B3, B2, B1, B0 into the four-bit shift register. Thus, only four clock cycles are required to transfer a number into the ETC. The keypad is disabled in this mode. A Logic "1" on the Tone Output ($\overline{TO}$) will disable tone outputs until valid data from the microprocessor is in place. Subsequently $\overline{TO}$ is switched to a Logic "0" to enable the DTMF generator. Figures 9 and 10 show the timing waveforms for the manual and automatic dialing modes and Table 2 specifies timing limitations.

The keypad decoder's exclusive OR circuit generates the DP and MS output signals. The DP output indicates (when at a Logic "1") that one, and only one, key is

depressed, thereby indicating valid data is available to the MPU. The DP output can additionally be used to initiate a data transfer sequence to the microprocessor. The MS output (when at a Logic "1") indicates the DTMF generator is enabled and the speech network is muted.

Pin A+ is to be connected to a source of 2.5 to 10 volts (generally from the microprocessor circuit) to enable the pullup circuits on the microprocessor interface outputs (DP, MS, I/O). Additionally, this voltage will power the entire circuitry (except Tone Ringer) in the absence of voltage at V+. This permits use of the transmit and receive amplifiers, keypad interface, and DTMF generator for non-typical telephone functions.

See Figure 45 for a typical interconnection to an MC6821 PIA (Peripheral Interface Adapter). Connection to a port on any other class of microprocessor will be similar.

FIGURE 7 — TONE RINGER BLOCK DIAGRAM

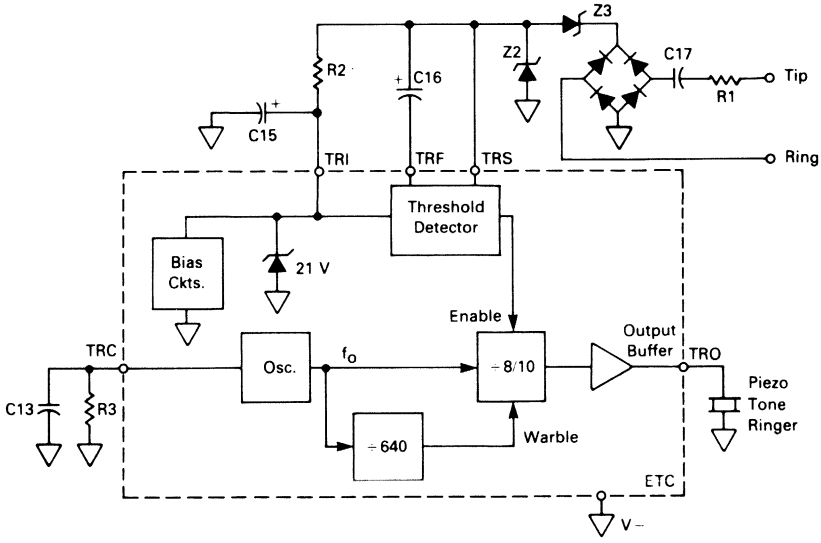


FIGURE 8 — MICROPROCESSOR INTERFACE BLOCK DIAGRAM

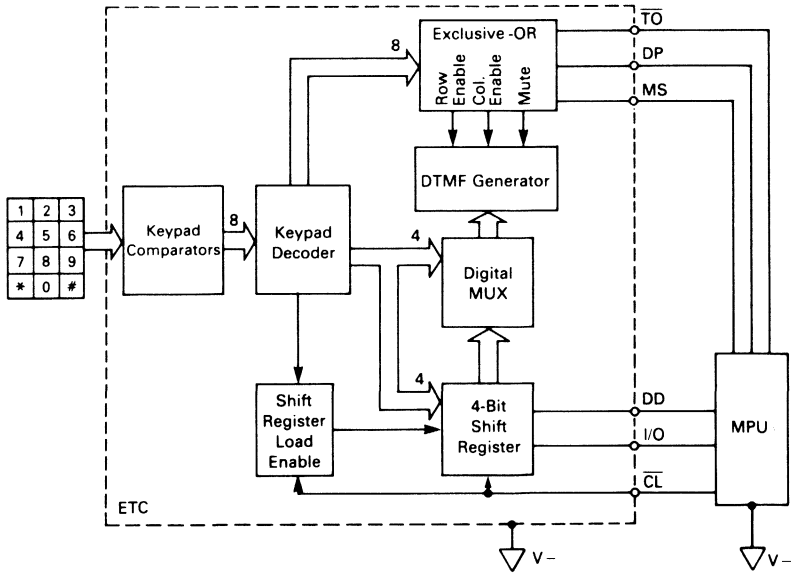


FIGURE 9 — OUTPUT DATA CYCLE

NOTE: $\overline{TO}$ may be low (Tone generator enabled) if desired.

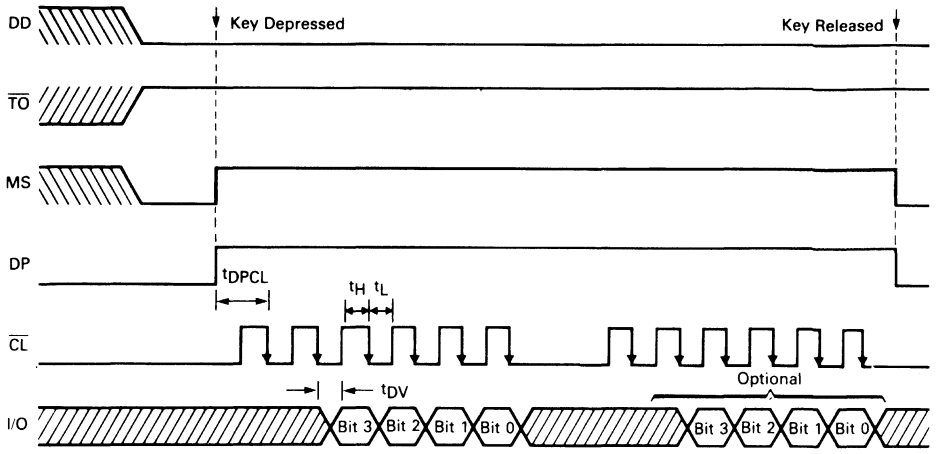


FIGURE 10 — INPUT DATA CYCLE

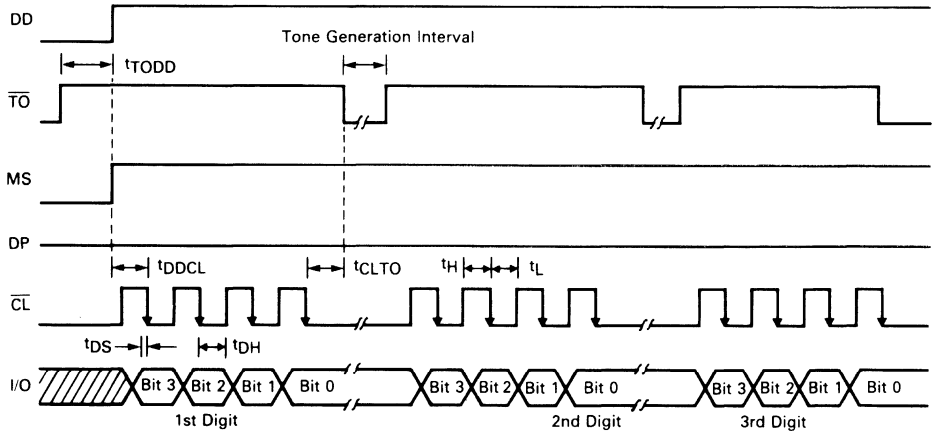


TABLE 1 — FREQUENCY SYNTHESIZER ERRORS

	DTMF Standard (Hz)	Tone Output Frequency with 500 kHz Oscillator	% Deviation from Standard
Row 1	697	696.4	−0.086
Row 2	770	769.2	−0.104
Row 3	852	853.2	+0.141
Row 4	941	939.8	−0.128
Column 1	1209	1207.7	−0.108
Column 2	1336	1336.9	+0.067
Column 3	1477	1479.3	+0.156
Column 4	1633	1634.0	+0.061

TABLE 2 — TIMING LIMITATIONS

Symbol	Parameter	Min	Typ	Max	Unit	Ref
f_{CL}	Clock Frequency	0	20	30	kHz	
t_H	Clock High Time	15	—	—	μs	Figs. 9,10
t_L	Clock Low Time	15	—	—	μs	Figs. 9,10
t_r, t_f	Clock Rise, Fall Time	—	—	2.0	μs	
t_{DV}	Clock Transition to Data Valid	—	—	10	μs	Fig. 9
t_{DPCL}	Time from DP High to $\overline{CL}$ Low	20	—	—	μs	Fig. 9
t_{DDCL}	Time from DD High to $\overline{CL}$ Low	20	—	—	μs	Fig. 10
t_{DS}	Data Setup Time	10	—	—	μs	Fig. 10
t_{DH}	Data Hold Time	10	—	—	μs	Fig. 10
t_{CLTO}	Time from $\overline{CL}$ Low to $\overline{TO}$ Low	10	—	—	μs	Fig. 10
t_{TODD}	Time from $\overline{TO}$ High to DD High	20	—	—	μs	Fig. 10

PIN DESCRIPTION

(See Figure 45 for external component identifications.)

PIN (PLCC)	PIN (DIP)	Designation	Function
1–4	1–4	R1–R4	Keypad inputs for Rows 1 through 4. When open, internal 8.0 kΩ resistors pull up the row inputs to a regulated (≈0.5 volt) supply. In normal operation, a row and a column input are connected through a SPST switch by the telephone keypad. Row inputs can also be activated by a Logic "0" (<250 mV) from a microprocessor port.
7–10	5–8	C1–C4	Keypad inputs for Columns 1 through 4. When open, internal 8.0 kΩ resistors pull down the column inputs to V−. In normal operation, connecting any column input to any row input produces the respective row and column DTMF tones. In addition to being connected to a row input, column inputs can be activated by a Logic "1" (>250 mV and <1.0 volt).
11	9	DP	Depressed Pushbutton (Output) — Normally low; A Logic "1" indicates one and only one, button of the DTMF keypad is depressed.
12	10	$\overline{TO}$	$\overline{Tone\ Output}$ (Input) — When a Logic "1," disables the DTMF generator. Keypad is not disabled.
13	11	MS	Mute/Single Tone (Output) — A Logic "1" indicates the tone generator is enabled. A Logic "0" indicates tone generator is disabled.
14	12	A+	MPU Power Supply (Input) — Enables pullups on the microprocessor section outputs. Additionally, this voltage will power the entire circuit (except Tone Ringer) in the absence of voltage at V+.
15	13	I/O	Input/Output — Serial Input or Output data (determined by DD input) to or from the microprocessor for storing or retrieving telephone numbers. Guaranteed to be a Logic "1" on powerup if DD = Logic "0."
16	14	DD	Data Direction (Input) — Determines direction of data flow through I/O pin. As a Logic "1," I/O is an input to the DTMF generator. As a Logic "0," I/O outputs keypad entries to the microprocessor.
17	15	$\overline{CL}$	$\overline{Clock}$ (Input) — Serially shifts data in or out of I/O pin. Data is transferred on negative edge typically at 20 kHz.
18,19	16,17	CR1, CR2	Ceramic Resonator oscillator input and feedback terminals, respectively. The DTMF dialer is intended to operate with a 500 kHz ceramic resonator from which row and column tones are synthesized.
31	28	CAL	Amplitude CALibration terminal for DTMF dialer. Resistor R14 from the CAL pin to V− controls the DTMF output signal level at Tip and Ring.
38	35	FB	FeedBack terminal for DTMF output. Capacitor C14 connected from FB to V+ provides ac feedback to reduce the output impedance to Tip and Ring when tone dialing.
32	29	VR	Voltage Regulator output terminal. VR is the output of a 1.1 volt voltage regulator which supplies power to the speech network amplifiers and DTMF generator during signaling. To improve regulator efficiency at low line current conditions, an external PNP pass-transistor T1 is used in the regulator circuit. Capacitor C9 frequency compensates the VR regulator to prevent oscillation.
36	33	BP	Base of a PNP Pass-transistor. Under long-loop conditions where low line voltages would cause VR to fall below 1.1 volts, BP drives the PNP transistor T1 into saturation, thereby minimizing the voltage drop across the pass transistor. At line voltages which maintain VR above 1.1 volts, BP biases T1 in the linear region thereby regulating the VR voltage. Transistor T1 also couples the ac speech signals from the transmit amplifier to Tip and Ring at V+.
37	34	V+	The more positive input to the regulator, speech, and DTMF sections connected to Tip and Ring through the polarity guard diode bridge.
33	30	V−	The dc common (more negative input) connected to Tip and Ring through the polarity guard bridge.
35	32	LR	DC Load Resistor. Resistor R4 from LR to V− determines the dc input resistance at Tip and Ring. This resistor is external not only to enable programming the dc resistance but also to avoid high on-chip power dissipation with short telephone lines. It acts as a shunt load conducting the excess dc line current. At low line voltages (<3.0 volts), no current flows through LR.
34	31	LC	DC Load Capacitor. Capacitor C11 from LC to V− forms a low-pass filter which prevents the resistor at LR from loading ac speech and DTMF signals.
22	20	MIC	MICrophone negative supply terminal. The dc current from the electret microphone is returned to V− through the MIC terminal which is connected to the collector of an on-chip NPN transistor. The base of this transistor is controlled either internally by the mute signal from the DTMF generator, or externally by the logic input pin MM.

(continued)

PIN DESCRIPTION (continued)

PIN (PLCC)	PIN (DIP)	Designation	Function
20	18	MM	Microphone Mute. The MM pin provides a means to mute the microphone in response to a digital control signal. When this pin is connected to a Logic "1" (>2.0 V) the microphone dc return path through the MIC terminal is disabled.
25	22	TXI	Transmit amplifier Input. TXI is the input to the transmit amplifier from an electret microphone. AC coupling capacitors allow the dc offset at TXI to be maintained approximately 0.6 V above V− by feedback through resistor R11 from TXO.
24	21	TXL	Transmit Input Limiter. An internal variable resistance element at the TXL terminal controls the transmitter input level to prevent clipping with high signal levels. Coupling capacitors C4 and C5 prevent dc current flow through TXL. The dynamic range of the transmit peak limiter is controlled by resistors R12 and R13.
26	23	TXO	Transmit Amplifier Output. The transmit amplifier output drives ac current through the voltage regulator pass-transistor T1 via resistor R10. The dc bias voltage at TXO is typically 0.6 volts above V−. The transmit amplifier gain is controlled by the R11/(R12 + R13) ratio.
21	19	AGC	Automatic Gain Control low-pass filter terminal. Capacitor C3 connected between AGC and VR sets the attack and decay time of the transmit limiter circuit. This capacitor also aids in reducing clicks in the receiver due to hook-switch transients and DTMF on/off transients. In conjunction with internal resistors, C3 (1.0 μF) forms a timer which mutes the receiver amplifier for approximately 20 milliseconds after the user goes off-hook or releases a DTMF Key.
30	27	RXO	Receiver Amplifier Output. This terminal is connected to the open-collector NPN output transistor of the receiver amplifier. DC bias current for the output device is sourced through the receiver from VR. The bias voltage at RXO is typically 0.6 volts above the V−. Capacitor C10 from RXO to VR provides frequency compensation for the receiver amplifier.
29	26	RXI	Receiver Amplifier Input. RXI is the input terminal of the receiver amplifier which is driven by ac signals from V+ and STA. Input coupling capacitor C8 allows RXI to be biased approximately 0.6 volts above the V− via feedback resistor R6.
28	25	RM	Receiver Amplifier Mute. A switched resistance at the RM terminal attenuates the receiver amplifier input signal produced by DTMF dialing tones at V+. RM also mutes clicks at the receiver which result from keypad or hook switch transitions. The ac resistance at RM is typically 540 Ω in the mute mode and 200 kΩ otherwise. Coupling capacitors C7 and C8 prevent dc current flow through RM.
27	24	STA	SideTone Amplifier output. STA is the output of the sidetone inverter amplifier whose input is driven by the transmit signal at TXO. The inverted transmit signal from STA subtracts from the receiver amplifier input current from V+, thus reducing the receiver sidetone level. Since the transmitted signal at V+ is phase shifted with respect to TXO by the reactive impedance of the phone line, the signal from STA must be similarly phase-shifted in order to provide adequate sidetone reduction. This phase relationship between the transmit signal at TXO and the sidetone cancellation signal from STA is controlled by R8, R9, and C6.
41	37	TRS	Tone Ringer Input Sense. TRS is the most positive input terminal of the tone ringer and the reference for the threshold detector.
42	38	TRI	Tone Ringer Input terminal. TRI is the positive supply voltage terminal for tone ringer circuitry. Current is supplied to TRI through resistor R2. When the average voltage across R2 exceeds an internal reference voltage (typically 1.6 volts) the tone ringer output is enabled.
44	40	TRF	Tone Ringer Input Filter capacitor terminal. Capacitor C16 connected from TRF to TRS forms a low-pass filter. This filter averages the signal across resistor R2 and presents this dc voltage to the input of the threshold detector. Line voltage transients are rejected if the duration is insufficient to charge C16 to 1.6 volts.
40	36	TRC	Tone Ringer oscillator Capacitor and resistor terminal. The relaxation oscillator frequency f_O is set by resistor R3 and capacitor C13 connected from TRC to V−. Typically, $f_O = (R3C13 + 8.0\ \mu s)^{-1}$.
43	39	TRO	Tone Ringer Output terminal. The frequency of the square wave output signal at TRO alternates from $f_O/8$ to $f_O/10$ at a warble rate of $f_O/640$. Typical output frequencies are 1000 Hz and 800 Hz with a 12.5 Hz warble rate. TRO sources or sinks up to 20 mA to produce an output voltage swing of 18 volts peak-to-peak across the piezo transducer. Tone ringer volume control can be implemented by a variable resistor in series with the piezo transducer.

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

KEYPAD INTERFACE CIRCUIT

Characteristic	Test Method	Symbol	Min	Typ	Max	Unit
Row Input Pullup Resistance m^{th} Row Terminal: m = 1,2,3,4	7	R_{Rm}	4.0	8.0	11	kΩ
Column Input Pulldown Resistance n^{th} Column Terminal: n = 1,2,3,4	8	R_{Cn}	4.0	8.0	11	kΩ
Ratio of Row-to-Column Input Resistances $K_{m,n} = \frac{R_{Rm}}{R_{Cn}}$, m = 1,2,3,4 n = 1,2,3,4	7 & 8	$K_{m,n}$	0.88	1.0	1.12	—
Row Terminal Open Circuit Voltage	7a	V_{ROC}	280	380	500	mVdc
Row Threshold Voltage for m^{th} Row Terminal: m = 1,2,3,4	9	V_{Rm}	0.70 V_{ROC}	—	—	Vdc
Column Threshold Voltage for n^{th} Column Terminal: n = 1,2,3,4	10	V_{Cn}	—	—	0.39 V_{ROC}	Vdc

MICROPROCESSOR INTERFACE

Voltage Regulator Output A+ Regulator	29	$V_{R/A}$	0.95	1.1	1.3	V
A+ Input Current Off-Hook	28a	I_A(off)	300	500	700	μA
A+ Input Current On-Hook	28b	I_A(on)	4.0	6.0	9.0	mA
Input Resistance (DD, $\overline{TO}$, $\overline{CL}$)	30	R_{in}	50	100	150	kΩ
Input Current (I/O)	31	I_{in}	—	80	200	μA
Input High Voltage (DD, $\overline{TO}$, $\overline{CL}$, I/O)	—	V_{IH}	2.0	—	A+	V
Input Low Voltage (DD, $\overline{TO}$, $\overline{CL}$, I/O)	—	V_{IL}	—	—	0.8	V
Output High Voltage (MS, DP, I/O)	32	V_{OH}	2.4	4.0	—	V
Output Low Voltage (MS, DP, I/O)	33	V_{OL}	—	0.1	0.4	V

LINE VOLTAGE REGULATOR

Voltage Regulator Output	1a	V_R	1.0	1.1	1.2	Volts
V+ Current in DTMF Mode	2a	I_{DT}	8.0	12	14	mA
Change in I_{DT} with Change in V+ Voltage	2b	ΔI_{DT}	—	0.8	2.0	mA
V+ Current in Speech Mode		I_{SP}				mA
V+ = 1.7 V	1b		3.5	5.0	7.0	
V+ = 5.0 V	1c		8.0	11	15	
Speech to DTMF Mode Current Difference	3	ΔI_{TR}	−2.0	2.0	3.5	mA
LR Level Shift		ΔV_{LR}				Vdc
V+ = 5.0 V, I_{LR} = 10 mA	4a		2.5	2.9	3.5	
V+ = 18 V, I_{LR} = 110 mA	4b		2.8	3.3	4.0	
LC Terminal Resistance	5	R_{LC}	30	50	75	kΩ
Load Regulation	6	ΔV_R	−20	−6.0	20	mVdc

3

ELECTRICAL CHARACTERISTICS (continued)

SPEECH NETWORK

Characteristic	Test Method	Symbol	Min	Typ	Max	Unit
MIC Terminal Saturation Voltage	20	V_{MIC}	—	60	125	mVdc
MIC Terminal Leakage Current	21a	I_{MIC}	—	0.0	5.0	μA
MM Terminal Input Resistance	21b	R_{MM}	50	100	170	kΩ
TXO Terminal Bias	22a	B_{TXO}	0.46	0.53	0.62	—
TXI Terminal Input Bias Current	22b	I_{TXI}	—	50	250	nA
TXO Terminal Positive Swing	22c	$V_{TXO(+)}$	—	25	60	mVdc
TXO Terminal Negative Swing	22d	$V_{TXO(-)}$	—	130	200	mVdc
Transmit Amplifier Closed-Loop Gain	23a	G_{TX}	16.5	19	20	V/V
Sidetone Amplifier Gain	23b	G_{STA}	0.41	0.45	0.55	V/V
STA Terminal Output Current	24	I_{STA}	50	100	250	μA
RXO Terminal Bias	25a	B_{RXO}	0.46	0.62	0.62	—
RXI Terminal Input Bias Current	25b	I_{RXI}	—	100	400	nA
RXO Terminal Positive Swing	25c	$V_{RXO(+)}$	—	1.0	20	mVdc
RXO Terminal Negative Swing	25d	$V_{RXO(-)}$	—	40	100	mVdc
TXL Terminal OFF Resistance	26a	$R_{TXL(OFF)}$	125	200	300	kΩ
TXL Terminal ON Resistance	26b	$R_{TXL(ON)}$	—	20	100	Ω
RM Terminal OFF Resistance	27a	$R_{RM(OFF)}$	125	180	300	kΩ
RM Terminal ON Resistance	27b	$R_{RM(ON)}$	410	570	770	Ω

DTMF GENERATOR

Row Tone Frequency	Row 1	11a, 11b	f_{Rm}	692.9	696.4	699.9	Hz
	Row 2			765.3	769.2	773.0	
	Row 3			848.9	853.2	857.5	
	Row 4			935.1	939.8	944.5	
Column Tone Frequency	Column 1	11c, 11d	f_{Cn}	1201.6	1207.7	1213.7	Hz
	Column 2			1330.2	1336.9	1343.6	
	Column 3			1471.9	1479.3	1486.7	
	Column 4			1625.2	1633.4	1641.5	
Row Tone Amplitude		11e	V_{Row}	0.34	0.39	0.50	V_{rms}
Column Tone Amplitude		11f	V_{Col}	0.43	0.48	0.62	V_{rms}
Column Tone Pre-emphasis		11g	dB_{CR}	0.5	1.8	3.0	dB
DTMF Distortion		12	% Dis	—	4.0	6.0	%
DTMF Output Resistance		13	R_o	1.0	2.5	3.0	kΩ

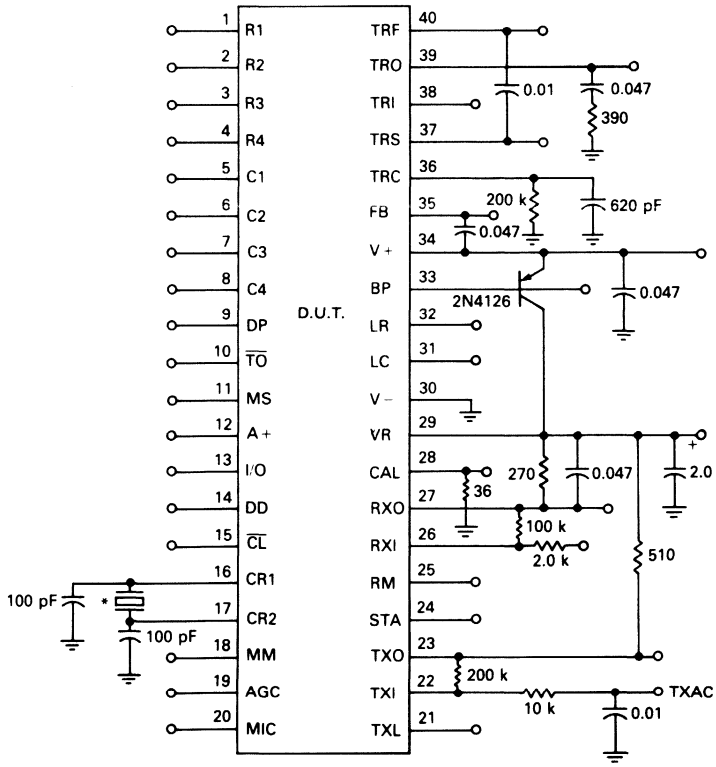
ELECTRICAL CHARACTERISTICS (continued)

TONE RINGER

Characteristic	Test Method	Symbol	Min	Typ	Max	Unit
TRI Terminal Voltage	14	V_{TRI}	20	21.5	23	Vdc
TRS Terminal Input Current		I_{TRS}				
V_{TRS} = 24 volts	15a		70	120	170	μA
V_{TRS} = 30 volts	15b		0.4	0.8	1.5	mA
TRF Threshold Voltage	16a	V_{TRF}	1.2	1.6	1.9	Vdc
TRF Threshold Hysteresis	16b	ΔV_{TRF}	100	200	400	mVdc
TRF Filter Resistance	17	R_{TRF}	30	50	75	kΩ
High Tone Frequency	18	f_H	920	1000	1080	Hz
Low Tone Frequency	18	f_L	736	800	864	Hz
Warble Frequency	18	f_W	11.5	12.5	13.5	Hz
Tone Ringer Output Voltage	19	$V_{o(p-p)}$	18	20	22	Vp-p

3

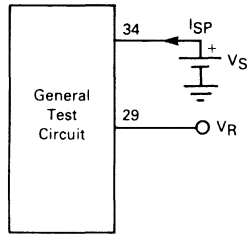
FIGURE 11 — GENERAL TEST CIRCUIT



Notes:
1. *Selected ceramic resonator: 500 kHz ±2.0 kHz.
2. Capacitances in μF unless noted.
3. All resistances in ohms.
4. Pin outs shown are for the 40 pin DIP.

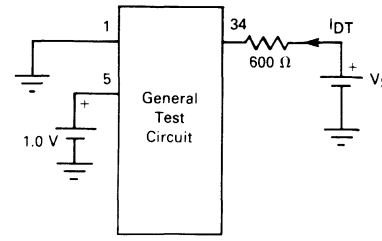
3

FIGURE 12 — TEST ONE



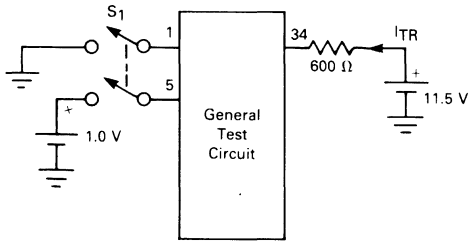
a. Measure V_R with V_S = 1.7 V
b. Measure I_{SP} with V_S = 1.7 V
c. Measure I_{SP} with V_S = 5.0 V

FIGURE 13 — TEST TWO



a. Measure I_{DT} with V_S = 11.5 V
b. Measure I_{DT} with V_S = 26 V. Calculate
$\Delta I_{DT} = I_{DT}\Big|_{26\ V} - I_{DT}\Big|_{11.5\ V}$

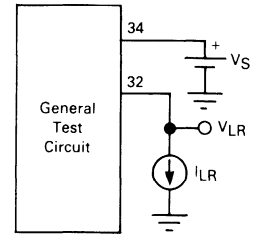
FIGURE 14 — TEST THREE



With S_1 open measure I_{TR}. Close S_1 and again measure I_{TR}. Calculate:

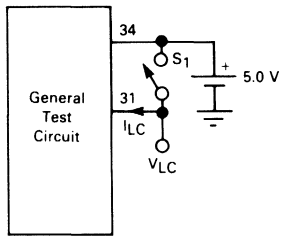
$$\Delta I_{TR} = I_{TR}\Big|_{S_1\ Closed} - I_{TR}\Big|_{S_1\ Open}$$

FIGURE 15 — TEST FOUR



a. Set V_S = 5.0 V and I_{LR} = 10 mA. Measure V_{LR}. Calculate $\Delta V_{LR} = V_S - V_{LR}$
b. Repeat Test 4a with V_S = 18 V and I_{LR} = 110 mA

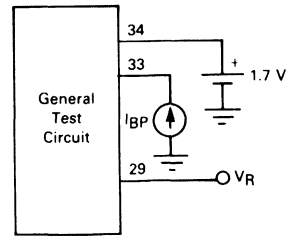
FIGURE 16 — TEST FIVE



With S_1 open measure V_{LC}.
Close S_1 and measure I_{LC}.
Calculate:

$$R_{LC} = \frac{5.0 - V_{LC}}{I_{LC}}$$

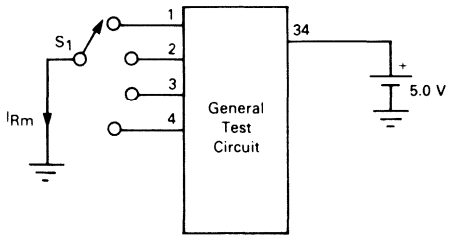
FIGURE 17 — TEST SIX



Set I_{BP} = 0.0 μA and measure V_R.
Set I_{BP} = 150 μA and measure V_R. Calculate:

$$\Delta V_R = V_R\Big|_{0.0\ \mu A} - V_R\Big|_{150\ \mu A}$$

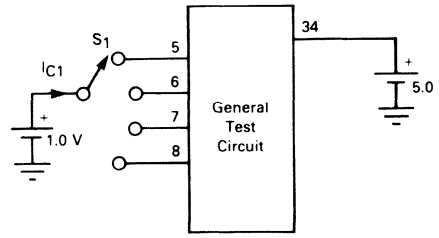
FIGURE 18 — TEST SEVEN



Subscript m corresponds to row number.

a. Set S_1 to Terminal 2 and measure voltage at Terminal 1 (V_{ROC}).
b. Set S_1 to Terminal 1 (m = 1) and measure I_{R1}. Calculate:
$R_{R1} = V_{ROC} \div I_{R1}$
c,d,e. Repeat Test 7b for m = 2,3,4.

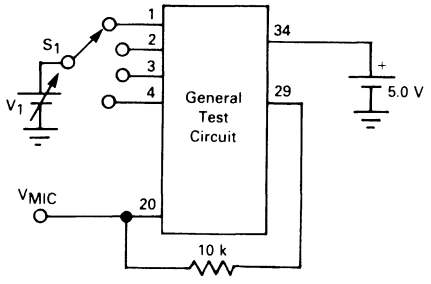
FIGURE 19 — TEST EIGHT



Subscript n corresponds to column number.

a. Set S_1 to Terminal 5 (n = 1) and measure I_{C1}. Calculate:
$R_{C1} = 1.0\ V \div I_{C1}$
b,c,d. Repeat Test 8a for n = 2,3,4.

FIGURE 20 — TEST NINE

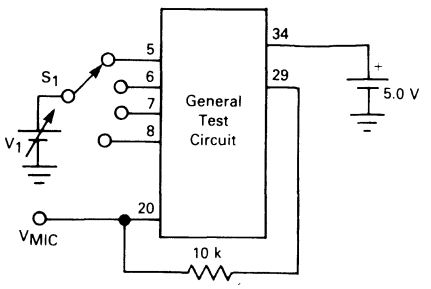


m corresponds to row number.

a. Set S_1 to Terminal 1 (m = 1) with V_1 = 1.0 Vdc. Verify V_{MIC} is Low (V_{MIC} < 0.3 Vdc). Decrease V_1 to 0.70 V_{ROC} and verify V_{MIC} switches high. (V_{MIC} > 0.5 Vdc). V_{ROC} is obtained from Test 7a.

b,c,d. Repeat Test 9a for rows 2,3, and 4. (m = 2,3,4)

FIGURE 21 — TEST TEN

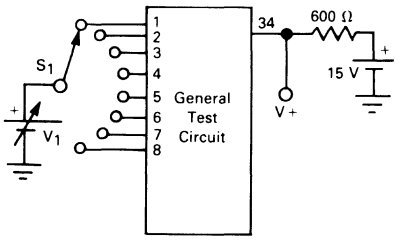


n corresponds to column number.

a. Set S_1 to Terminal 5 (n = 1) with V_1 = 0 Vdc. Verify V_{MIC} is low (V_{MIC} < 0.3 Vdc). Increase V_1 to 0.39 V_{ROC} and verify V_{MIC} switches high, (V_{MIC} > 0.5 Vdc). V_{ROC} is obtained from Test 7a.

b,c,d. Repeat Test 10a for columns 2,3, and 4. (n = 2,3,4)

FIGURE 22 — TEST ELEVEN



m corresponds to row number.
n corresponds to column number.

a. With V_1 = 0.0 V set S_1 to Terminal 1 (m = 1) and measure frequency of tone at V+.

b. Repeat Test 11a for rows 2,3 and 4. (m = 2,3,4).

c. With V_1 = 1.0 V set S_1 to Terminal 5. (n = 1) and measure frequency of tone at V+.

d. Repeat Test for columns 2,3, and 4. (n = 2,3,4).

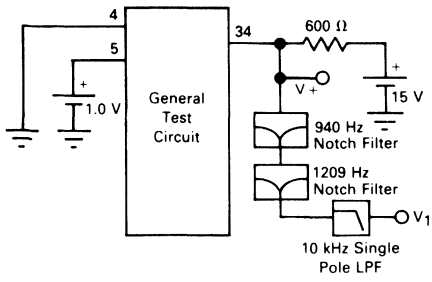
e. Set S_1 to Terminal 4 and V_1 = 0.0 V. Measure row tone amplitude at V+ (V_{ROW}).

f. Set S_1 to Terminal 8 and V_1 = 1.0 V. Measure column tone amplitude at V+. (V_{COL}).

g. Using results of Tests 11e and 11f, calculate:

$$dB_{CR} = 20 \log_{10} \frac{V_{COL}}{V_{ROW}}$$

FIGURE 23 — TEST TWELVE

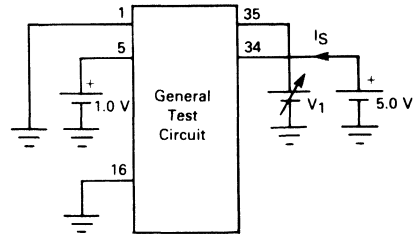


Note: The notch filters must have 50 dB attenuation at their respective center frequencies.

Measure V+ and V_1 with a true rms voltmeter. Calculate:

$$\% \text{ DIS} = \frac{V_1(\text{rms})}{V+(\text{rms})} \times 100$$

FIGURE 24 — TEST THIRTEEN

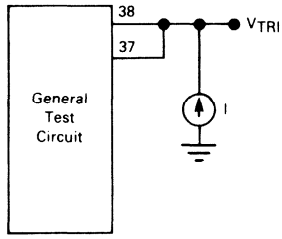


Measure I_S at V_1 = 1.8 V and V_1 = 2.8 V.

Calculate:

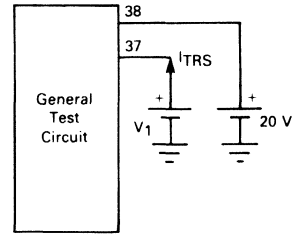
$$R_O = 1.0 \text{ V} \div \left[I_S\Big|_{2.8\text{ V}} - I_S\Big|_{1.8\text{ V}} \right]$$

FIGURE 25 — TEST FOURTEEN



Set I = 1.0 mA and measure V_{TRI}.

FIGURE 26 — TEST FIFTEEN



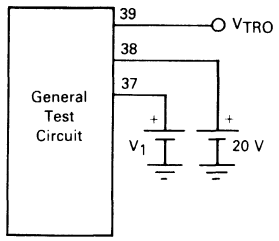
a. Measure I_{TRS} with V_1 = 24 V.

b. Measure I_{TRS} with V_1 = 30 V.

3

3

FIGURE 27 — TEST SIXTEEN



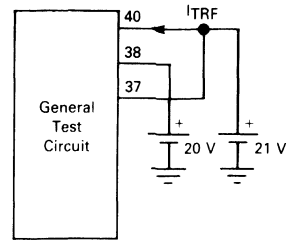
a. Increase V_1 from 21 V until V_{TRO} switches on. Note that V_{TRO} will be an 16 V_{pp} square wave. Record this value of V_1. Calculate:

$V_{TRF} = V_1 - 20$ V

b. Decrease V_1 from its setting in Test 16a until V_{TRO} ceases switching. Record this value of V_1. Calculate:

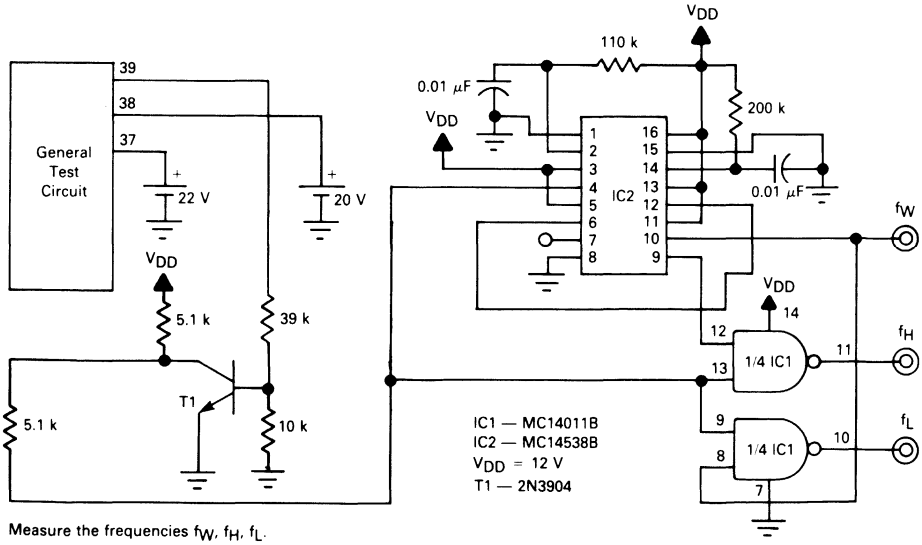
$\Delta V_{TRF} = V_1\big|_{\substack{\text{Test}\\16a}} - V_1\big|_{\substack{\text{Test}\\16b}}$

FIGURE 28 — TEST SEVENTEEN



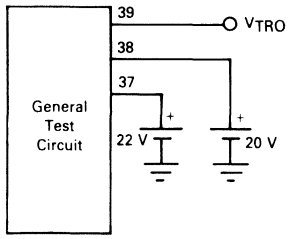
Measure I_{TRF}. Calculate: $R_{TRF} = 1.0 \div I_{TRF}$.

FIGURE 29 — TEST EIGHTEEN



Measure the frequencies f_W, f_H, f_L.

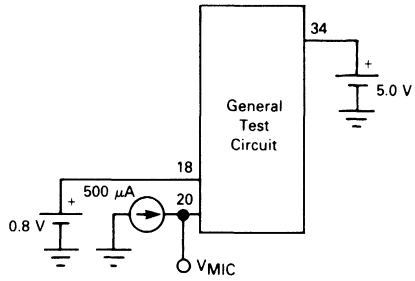
FIGURE 30 — TEST NINETEEN



Measure V_{TRO} peak-to-peak voltage swing. Using V_{TRI} from Test 14 Calculate:

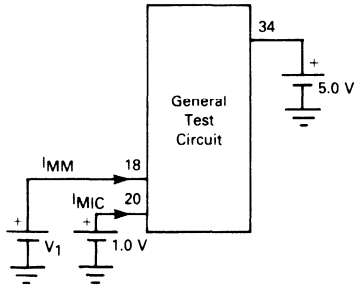
$V_{o(p-p)} = V_{TRI} - 20\ V + V_{TRO}$

FIGURE 31 — TEST TWENTY



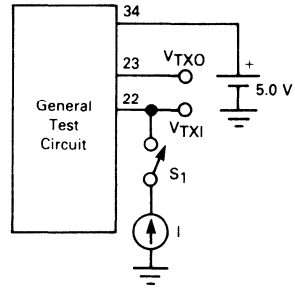
Measure V_{MIC}

FIGURE 32 — TEST TWENTY-ONE



a. Set V_1 = 2.0 V and measure I_{MIC}.
b. Set V_1 = 5.0 V and measure I_{MM}. Calculate: $R_{MM} = 5.0\ V \div I_{MM}$

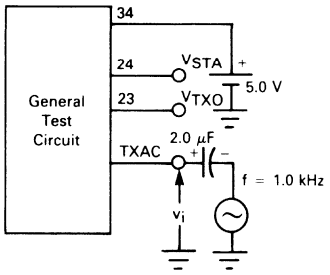
FIGURE 33 — TEST TWENTY-TWO



a. With S_1 open, measure V_{TXO}. Using V_R obtained in Test 1 Calculate: $B_{TXO} = V_{TXO} \div V_R$
b. With S_1 open, measure V_{TXO} and V_{TXI}. Calculate: $I_{TXI} = (V_{TXO} - V_{TXI}) \div 200\ k\Omega$
c. Close S_1 and set I = −10 μA. Measure V_{TXO}. Calculate: $V_{TXO}(+) = V_R - V_{TXO}$ where V_R is obtained from Test 1.
d. Close S_1 and set I = +10 μA. Measure V_{TXO}. $V_{TXO}(-) = V_{TXO}$.

3

FIGURE 34 — TEST TWENTY-THREE



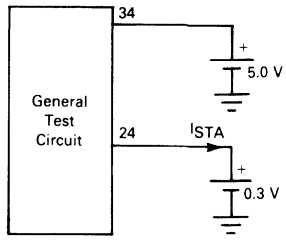
a. Set the generator for v_i = 3.0 mV_{rms}. Measure ac voltage V_{TXO}. Calculate:

$$G_{TX} = \frac{V_{TXO}}{v_i}$$

b. Measure ac voltage V_{STA}. Using V_{TXO} from Test 23a calculate:

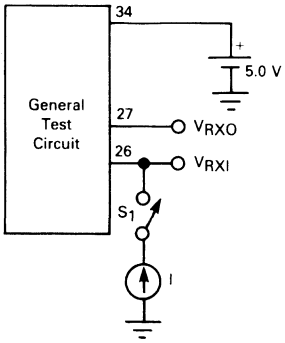
$$G_{STA} = \frac{V_{STA}}{V_{TXO}}$$

FIGURE 35 — TEST TWENTY-FOUR



Measure I_{STA}.

FIGURE 36 — TEST TWENTY-FIVE



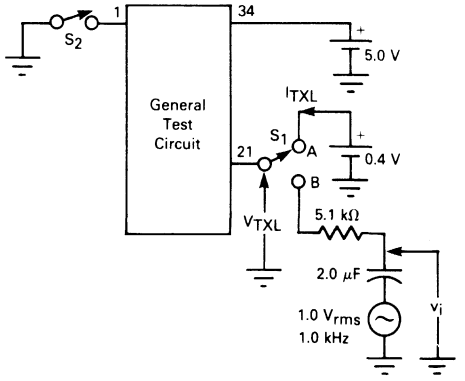
a. With S_1 open, measure V_{RXO}. Using V_R obtained in Test 1, calculate: $B_{RXO} = V_{RXO} \div V_R$.

b. With S_1 open, measure V_{RXO} and V_{RXI}. Calculate: $I_{RXI} = (V_{RXO} - V_{RX1}) \div 100\ k\Omega$

c. Close S_1 and set I = −10 μA. Measure V_{RXO}. Using V_R obtained in Test 1, calculate: $V_{RXO}(+) = V_R - V_{RXO}$.

d. Close S_1 and set I = +10 μA and measure V_{RXO}. $V_{RXO}(-) = V_{RXO}$.

FIGURE 37 — TEST TWENTY-SIX

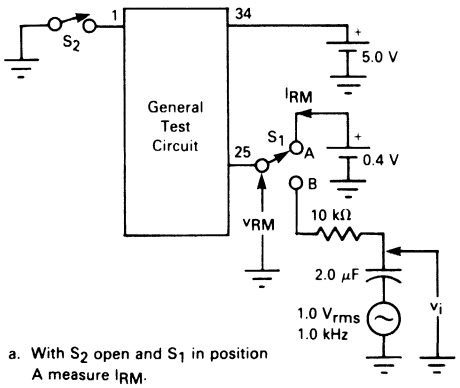


a. Set S_1 to position A with S_2 open. Measure I_{TXL}. Calculate: R_{TXL} (OFF) = 0.4 V ÷ I_{TXL}.

b. Set S_1 to position B and close S_2. Measure ac voltages v_i and V_{TXL}. Calculate:

$$R_{TXL}\ (ON) = \frac{V_{TXL}}{v_i - V_{TXL}} \times 5.1\ k\Omega$$

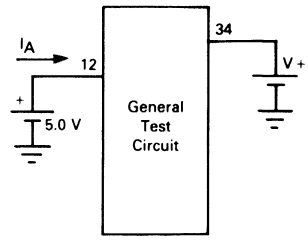
FIGURE 38 — TEST TWENTY-SEVEN



a. With S_2 open and S_1 in position A measure I_{RM}.
Calculate: $R_{RM}(OFF) = 0.4\ V \div I_{RM}$

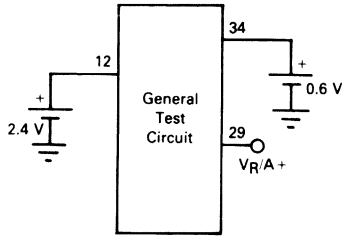
b. Close S_2 and switch S_1 to position B. Measure ac voltages v_i and V_{RM}.
Calculate:
$$R_{RM}(ON) = \frac{V_{RM}}{v_i - V_{RM}} \times 10\ k\Omega$$

FIGURE 39 — TEST TWENTY-EIGHT



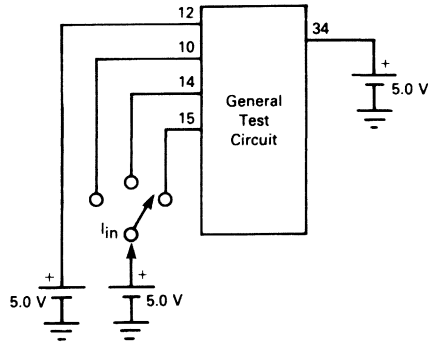
a. Set V+ = 1.4 V. Measure $I_A(OFF)$
b. Set V+ = 0.6 V. Measure $I_A(ON)$

FIGURE 40 — TEST TWENTY-NINE



Measure $V_R/A+$

FIGURE 41 — TEST THIRTY



Measure I_{in} at each of three inputs. For each, calculate:
$R_{in} = 5.0\ V/I_{in}$

FIGURE 42 — TEST THIRTY-ONE

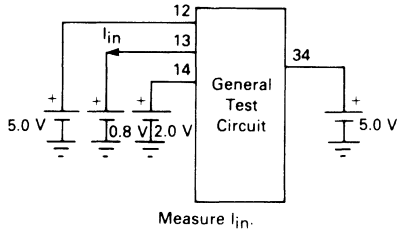
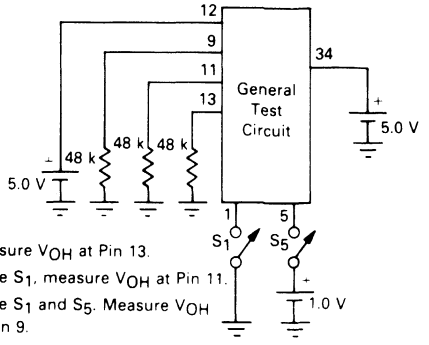
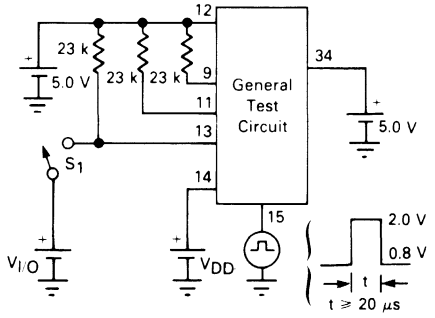


FIGURE 43 — TEST THIRTY-TWO



a. Measure V_{OH} at Pin 13.
b. Close S_1, measure V_{OH} at Pin 11.
c. Close S_1 and S_5. Measure V_{OH} at Pin 9.

FIGURE 44 — TEST THIRTY-THREE



a. Set V_{DD} to 0.8 V Measure V_{OL} voltages at Pins 9 and 11.
b. Close S_1. Force $V_{I/O}$ to 0.8 V and V_{DD} to 2.0 V. Apply 4 clock pulses to Pin 15. Open S_1 and decrease V_{DD} to 0.8 V. Measure V_{OL} at Pin 13.

APPLICATIONS INFORMATION

Figure 45 specifies a typical application circuit for the MC34010. Complete listings of external components are provided at the end of this section along with nominal component values.

The hook switch and polarity guard bridge configuration in Figure 45 is one of several options. If two bridges are used, one for the tone ringer and the other for speech and dialer circuits, then the hook switch can be simplified. Component values should be varied to optimize telephone performance parameters for each application. The relationships between the application circuit components and certain telephone parameters are briefly described in the following:

On-Hook Input Impedance

R1, C17, and Z3 are the significant components for on-hook impedance. C17 dominates at low frequencies, R1 at high frequencies and Z3 provides the non-linearity required for 2.5 V and 10 V impedance signature tests. C17 must generally be ≤ 1.0 μF to satisfy 5.0 Hz impedance specifications.

Tone Ringer Output Frequencies

R3 and C13 control the frequency (f_o) of a relaxation oscillator. Typically $f_o = (R3C13 + 8.0\ \mu s)^{-1}$. The output tone frequencies are $f_o/10$ and $f_o/8$. The warble rate is $f_o/640$. The tone ringer will operate with f_o from 1.0 kHz to 10 kHz. R3 should be limited to values between 150 k and 300 k.

Tone Ringer Input Threshold

After R1, C17, and Z3 are chosen to satisfy on-hook impedance specifications, R2 is chosen for the desired ring start threshold. Increasing R2 reduces the ac input voltage required to activate the tone ringer output. R2 should be limited to values between 0.8 k and 2.0 kΩ.

Off-Hook DC Resistance

R4 conducts the dc line current in excess of the speech and dialer bias current. Increasing R4 increases the input resistance of the telephone for line currents above 10 mA. R4 should be selected between 30 Ω and 120 Ω.

Off-Hook AC Impedance

The ac input impedance is equal to the receive amplifier load impedance (at RXO) divided by the receive amplifier gain (voltage gain from V+ to RXO). Increasing the impedance of the receiver increases the impedance of the telephone. Increasing the gain of the receiver amplifier decreases the impedance of the telephone.

DTMF Output Amplitude

R14 controls the amplitude of the row and column DTMF tones. Decreasing R14 increases the level of tones generated at V+. The ratio of the row and column tone amplitudes is internally fixed. R14 should be greater than 20 Ω to avoid excessive current in the DTMF output amplifier.

Transmit Output Level

R10 controls the maximum signal amplitude produced at V+ by the transmit amplifier. Decreasing R10 increases the transmit output signal at V+. R10 should be greater than 220 Ω to limit current in the transmit amplifier output.

Transmit Gain

The gain from the microphone to the telephone line varies directly with R11. Increasing R11 increases the signal applied to R10 and the ac current driven through R10 to the telephone line. The closed loop-gain from the microphone to the TXO terminal should be greater than 10 to prevent transmit amplifier oscillations.

Note: Adjustments to transmit level and gain are complicated by the addition of receiver sidetone current to the transmit amplifier output current at V+. Normally the sidetone current from the receiver will increase the transmit signal (if the current in the receiver is in phase with that in R10). Thus the transmit gain and sidetone levels cannot be adjusted independently.

Receiver Gain

Feedback resistor R6 adjusts the gain at the receiver amplifier. Increasing R6 increases the receiver amplifier gain.

Sidetone Level

Sidetone reduction is achieved by the cancellation of receiver amplifier input signals from R9 and R5. R8, R15, and C6 determine the phase of the sidetone balance signal in R9. The ac voltage at the junction of R8 and R9 should be 180° out of phase with the voltage at V+. R9 is selected such that the signal current in R9 is slightly greater than that in R5. This insures that the sidetone current in the receiver adds to the transmit amplifier output current.

Hook-Switch Click Suppression

When the telephone is switched to the off-hook condition C3 charges from 0 volts to a 300 mV bias voltage. During this time interval, receiver clicks are suppressed by a low impedance at the RM terminal. If this click suppression mechanism is desired during a rapid succession of hook switch transitions, then C3 must be quickly discharged when the telephone is on-hook, R16 and S3 provide a rapid discharge path for C3 to reset the click suppression timer. R16 is selected to limit the discharge current in S3 to prevent damage to switch contacts.

Microprocessor Interface

The six microprocessor interface lines (DP, $\overline{TO}$, MS, DD, I/O, and $\overline{CL}$) can be connected directly to a port, as shown in Figure 47. The DP line (Depressed Pushbutton) is also connected to an interrupt line to signal the microprocessor to begin a read data sequence when storing a number into memory. The MC34010A clock speed requirement is slow enough (typically 20 kHz) so that it is not necessary to divide down the processor's system clock, but rather a port output can be toggled. This facilitates synchronizing the clock and data transfer, eliminating the need for hardware to generate the clock.

The DD pin must be maintained at a Logic "0" when the microprocessor section is not in use, so as to permit normal operation of the keypad.

When the microprocessor interface section is not in use, the supply voltage at Pin 12 (A+) may be disconnected to conserve power. Normally the speech circuitry is powered by the voltage supplied at the V+ terminal (Pin 34) from the telephone lines. During this time, A+ powers only the active pullups on the three microprocessor outputs (DP, MS, and I/O). When the telephone is "on-hook," and V+ falls below 0.6 volts, power is then supplied to the telephone speech and dialer circuitry from A+. Powering the circuit from the A+ pin permits communication with a microprocessor, and/or use of the transmit and receiver amplifiers, while the telephone is "on-hook."

3

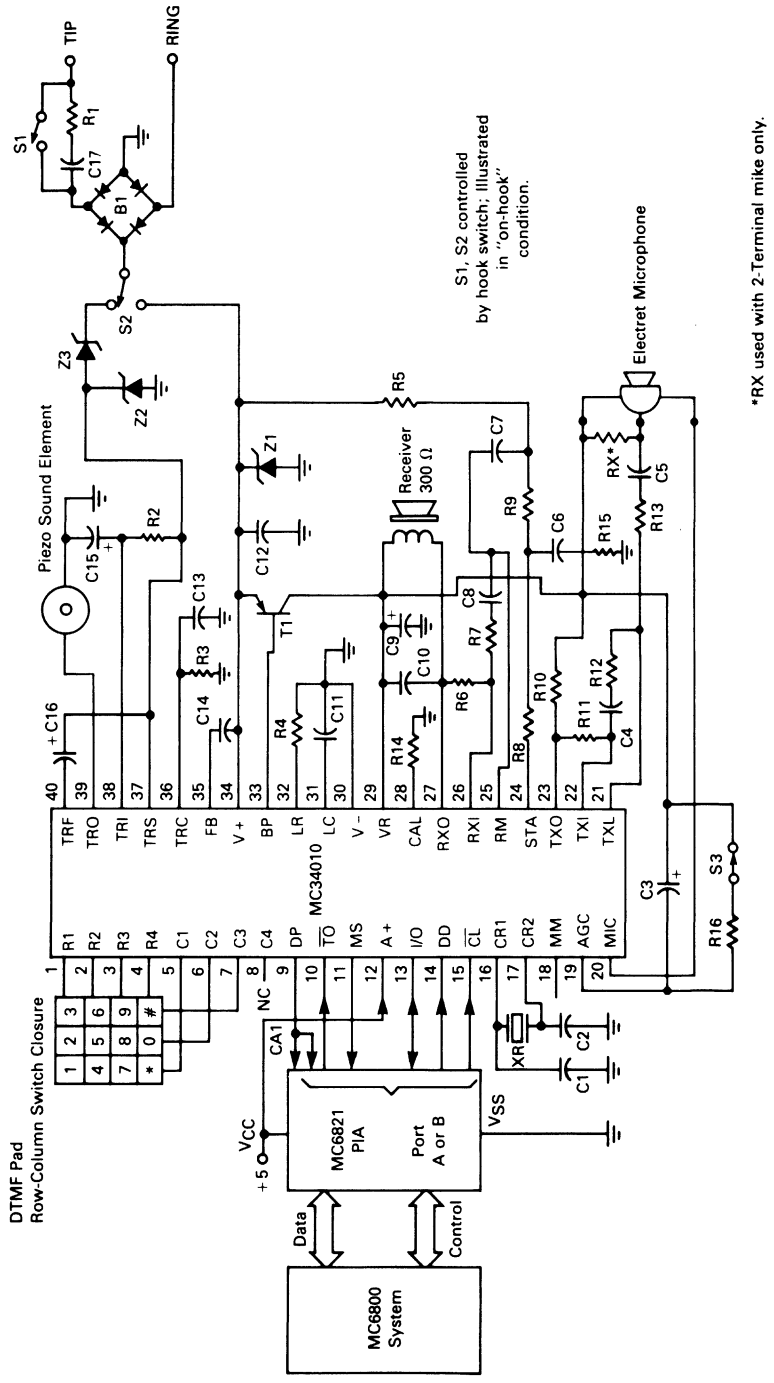


FIGURE 45 — ELECTRONIC TELEPHONE APPLICATION CIRCUIT

EXTERNAL COMPONENTS

(Component Labels Referenced to Figure 45)

Capacitors	Nominal Value	Description
C1, C2	100 pF	Ceramic Resonator oscillator capacitors.
C3	1.0 μF, 3.0 V	Transmit limiter low-pass filter capacitor: controls attack and decay time of transmit peak limiter.
C4, C5	0.1 μF	Transmit amplifier input capacitors: prevent dc current flow into TXL pin and attenuate low-frequency noise on microphone lead.
C6	0.05 μF	Sidetone network capacitor: provides phase-shift in sidetone path to match that caused by telephone line reactance.
C7, C8	0.05 μF	Receiver amplifier input capacitors: prevent dc current flow into RM terminal and attenuates low frequency noise on the telephone line.
C9	2.2 μF, 3.0 V	VR regulator capacitor: frequency compensates the VR regulator to prevent oscillation.
C10	0.01 μF	Receiver amplifier output capacitor: frequency compensates the receiver amplifier to prevent oscillation.
C11	0.1 μF	DC load filter capacitor: prevents the dc load circuit from attenuating ac signals on V+.
C12	0.01 μF	Telephone line bypass capacitor: terminates telephone line for high frequency signals and prevents oscillation in the VR regulator.
C13	620 pF	Tone ringer oscillator capacitor: determines clock frequency for tone and warble frequency synthesizers.
C14	0.1 μF	DTMF output feedback capacitor: ac couples feedback around the DTMF output amplifier which reduces output impedance.
C15	4.7 μF, 25 V	Tone ringer input capacitor: filters the rectified tone ringer input signal to smooth the supply potential for oscillator and output buffer.
C16	1.0 μF, 10 V	Tone ringer filter capacitor: integrates the voltage from current sense resistor R2 at the input of the threshold detector.
C17	1.0 μF, 250 Vac Non-polarized	Tone ringer line capacitor: ac couples the tone ringer to the telephone line; partially controls the on-hook input impedance of telephone.

Resistors	Nominal Value	Description
R1	6.8 k	Tone ringer input resistor: limits current into the tone ringer from transients on the telephone line and partially controls the on-hook impedance of the telephone.
R2	1.8 k	Tone ringer current sense resistor: produces a voltage at the input of the threshold detector in proportion to the tone ringer input current.
R3	200 k	Tone ringer oscillator resistor: determines the clock frequency for tone and warble frequency synthesizers.
R4	82, 1.0 W	DC load resistor: conducts all dc line current in excess of the current required for speech or dialing circuits; controls the off-hook dc resistance of the telephone.
R5, R7	150 k, 56 k	Receiver amplifier input resistors: couple ac input signals from the telephone line to the receiver amplifier; signal in R5 subtracts from that in R9 to reduce sidetone in receiver.
R6	200 k	Receiver amplifier feedback resistor: controls the gain of the receiver amplifier.
R8, R9	1.5 k, 30 k	Sidetone network resistors: drive receiver amplifier input with the inverted output signal from the transmitter; phase of signal in R9 should be opposite that in R5.
R10	270	Transmit amplifier load resistor: converts output voltage of transmit amplifier into a current that drives the telephone line; controls the maximum transmit level.
R11	200 k	Transmit amplifier feedback resistor: controls the gain of the transmit amplifier.
R12, R13	4.7 k, 4.7 k	Transmit amplifier input resistors: couple signal from microphone to transmit amplifier; control the dynamic range of the transmit peak limiter.
R14	36	DTMF calibration resistor: controls the output amplitude of the DTMF dialer.
R15	2.0 k	Sidetone network resistor (optional): reduces phase shift in sidetone network at high frequencies.
R16	100	Hook switch click suppression current limit resistor (optional): limits current when S3 discharges C3 after switching to the on-hook condition.
R_X	3.0 k	Microphone bias resistor: sources current from VR to power a 2-terminal electret microphone; R_X is not used with 3-terminal microphones.

EXTERNAL COMPONENTS (continued)

Semiconductors	Electret Mic	Receiver
B1 = MDA101A, or equivalent, or 4-1N4005 T1 = 2N4126 or equivalent Z1 = 18 V, 1.5 W, 1N5931A Z2 = 30 V, 1.5 W, 1N5936A Z3 = 4.7 V, 1/2 W, 1N750 XR — muRata Erie CSB 500 kHz Resonator, or equivalent Piezo — PBL 5030BC Toko Buzzer or equivalent	2 Terminal, Primo EM-95 (Use R_X) or equivalent 3 Terminal, Primo 07A181P (Remove R_X) or equivalent	Primo Model DH-34 (300 Ω) or equivalent

Motorola Inc. does not endorse or warrant the suppliers referenced.

MOTOROLA

MC34011A

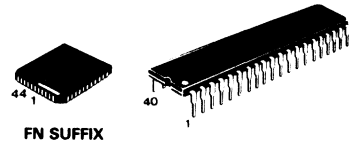
Advance Information

ELECTRONIC TELEPHONE CIRCUIT

- Provides All Basic Telephone Station Apparatus Functions in a Single IC, Including DTMF Dialer, Tone Ringer, Speech Network and Line Voltage Regulator
- DTMF Generator Uses Low-Cost Ceramic Resonator with Accurate Frequency Synthesis Technique
- Tone Ringer Drives Piezoelectric Transducer and Satisfies EIA RS-470 Impedance Signature Requirements
- Speech Network Provides Two–Four Wire Conversion with Adjustable Sidetone Utilizing an Electret Transmitter
- On-Chip Regulator Insures Stable Operation Over Wide Range of Loop Lengths
- I^2L Technology Provides Low 1.4 Volt Operation and High Static Discharge Immunity
- Equalization Provided to Compensate for Long/Short Line Performance

ELECTRONIC TELEPHONE CIRCUIT

BIPOLAR LINEAR/I^2L

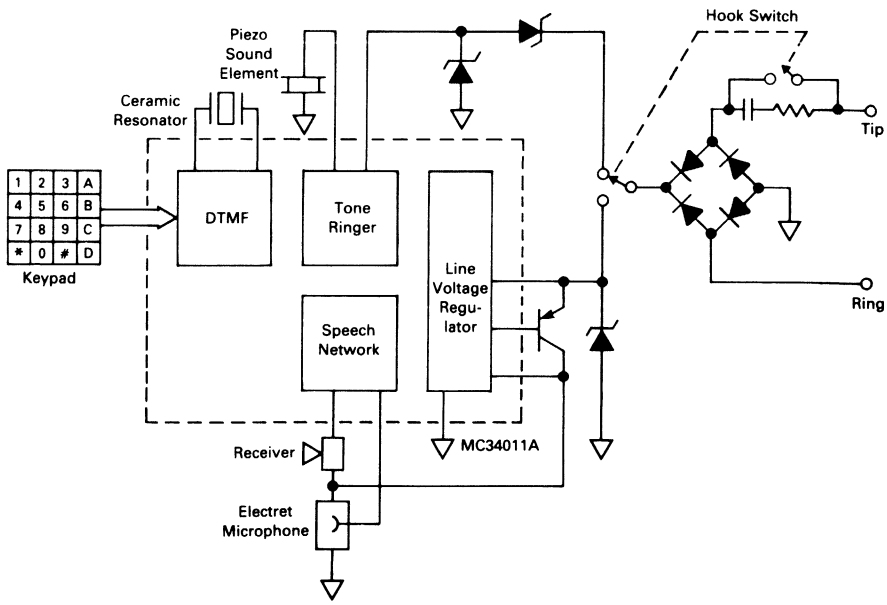


FN SUFFIX
44-PIN
PLCC
CASE 777-01

P SUFFIX
PLASTIC PACKAGE
CASE 711-03

3

FIGURE 1 — ELEMENTS OF THE ELECTRONIC TELEPHONE



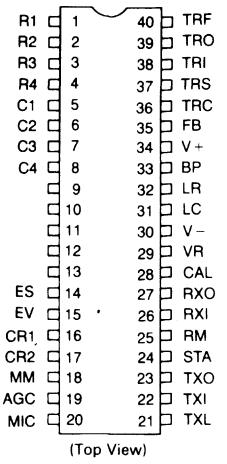
This document contains information on a new product. Specifications and information herein are subject to change without notice.

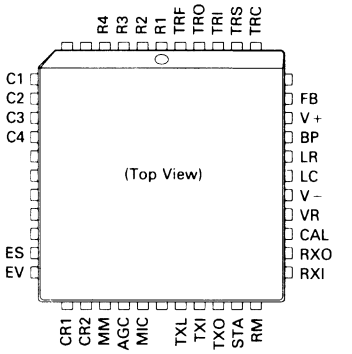
ADI745R2

MAXIMUM RATINGS (Voltage References to V−)

Parameter	Value	Unit
V+ Terminal Voltage (Pin 34)	+18, −1.0	V
VR Terminal Voltage (Pin 29)	+2.0, −1.0	V
RXO Terminal Voltage (Pin 27)	+2.0, −1.0	V
TRS Terminal Voltage (Pin 37)	+35, −1.0	V
TRO (With Tone Ringer Inactive) Terminal Voltage	+2.0, −1.0	V
R1–R4 Terminal Current (Pins 1–4) C1–C4 (Pins 5–8)	±100	mA
Operating Ambient Temperature Range	−20 to +60	°C
Storage Temperature Range	−65 to +150	°C

FIGURE 2 — PIN CONNECTIONS





3

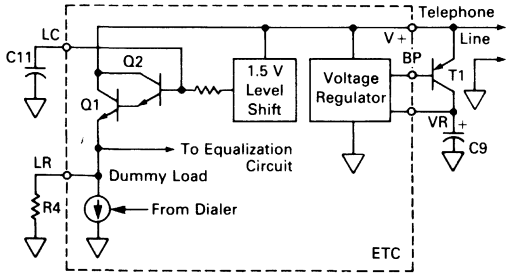
GENERAL CIRCUIT DESCRIPTION

Introduction

The MC34011A Electronic Telephone Circuit (ETC) provide all the necessary elements of a tone dialing telephone in a single IC. The functional blocks of the ETC include the DTMF dialer, speech network, tone ringer, and dc line interface circuit (Figure 1).

Low voltage operation is a necessity for telephones in networks where parallel telephone connections are common. An electronic speech network operating in parallel with a conventional telephone may receive line voltages below 2.5 volts. DTMF dialers operate at similarly low-line voltages when signaling through battery powered station carrier equipment. These low voltage requirements have been addressed by realizing the MC34011A in a bipolar/I^2L technology with appropriate circuit techniques. The resulting speech and dialer circuits maintain specified performance with instantaneous input voltage as low as 1.4 volts.

FIGURE 3 — DC LINE INTERFACE BLOCK DIAGRAM

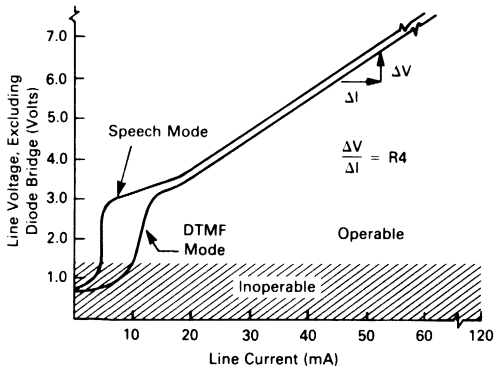


Line Voltage Regulator

The dc line interface circuit (Figure 3) determines the dc input characteristic of the telephone. At low input voltages (less than 3 volts) the ETC draws only the speech and dialer bias currents through the VR regulator. As input voltage increases, Q1 conducts the excess dc line current through resistor R4. The 1.5 volt level shift prevents saturation of Q2 with telephone line signals up to 2.0 volts peak (+5.2 dBm). A constant current (dummy load) is switched off when the DTMF dialer is activated to reduce line current transients. Figure 4 illustrates the dc voltage/current characteristic of an MC34011A telephone.

GENERAL CIRCUIT DESCRIPTION (continued)

FIGURE 4 — DC V-I CHARACTERISTIC OF THE ETC



Speech Network

The speech network (Figure 5) provides the two-to-four wire interface between the telephone line and the instrument's transmitter and receiver. An electret microphone biased from VR drives the transmit amplifier. For very loud talkers, the peak limiter circuit reduces the transmit input level to maintain low distortion. The transmit amplifier output signal is inverted at the STA terminal and driven through an external R-C network to control the receiver sidetone level. The switched ac resistance at the RM terminal reduces receiver signal when dialing and suppresses clicks due to hook or keypad switch transitions. When transmitting, audio signal currents (i_{TXO} and i_{RXO}) flow through the voltage regulator pass transistor (T1) to drive the telephone line. This feature has two consequences: 1) In the transmitting mode the receiver sidetone current i_{RXO} contributes to the total signal on the line along with i_{TXO}; 2) The ac impedance of the telephone is determined by the receiver impedance and the voltage gain from the line to the receiver amplifier output.

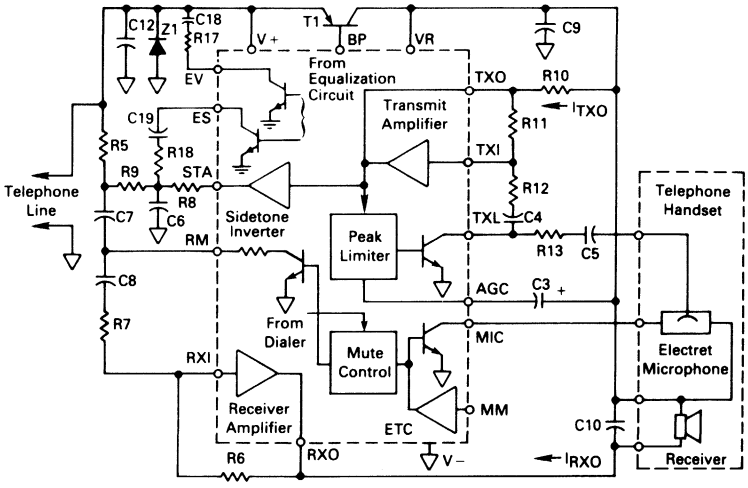
Equalization Circuit

The equalization circuit varies the transmit, receive and sidetone gains with loop current to compensate for losses in long lines. The LR terminal voltage varies directly as the dc loop current. The equalization circuit senses this voltage and switches in external resistors between V+ and V− and across capacitor C6 (Figure 5) when the loop current exceeds a threshold level. The speech network operates with full transmit, receive and sidetone gains for long loops. On short loops the LR voltage exceeds the threshold and these gains are reduced. The threshold detection circuit has a dc hysteresis to prevent distortion of speech signals when the telephone is operated at the threshold current. The equalization is disabled (gains at full value) during dialing.

DTMF Dialer

Keypad interface comparators activate the DTMF row and column tone generators (Figure 6) when a row and column input are connected through a SPST keypad. The keypad interface is designed to function with contact resistances up to 1.0 kΩ and leakage resistances as low as 150 kΩ. Single tones may be initiated by depressing two keys in the same row or column.

FIGURE 5 — SPEECH NETWORK BLOCK DIAGRAM



The programmable counters employ a novel design to produce non-integer frequency ratios. The various DTMF tones are synthesized with frequency division errors less than ±0.16% (Table 1). Consequently an inexpensive ceramic resonator can be used instead of a quartz crystal as the DTMF frequency reference. Total frequency error less than ±0.8% can be achieved with ±0.3% ceramic resonator. The row and column D/A converters produce 16-step approximations of sinusoidal waveforms. Feedback through terminal FB reduces the DTMF output impedance to approximately 2.0 kΩ to satisfy return loss specifications.

FIGURE 6 — DTMF DIALER BLOCK DIAGRAM

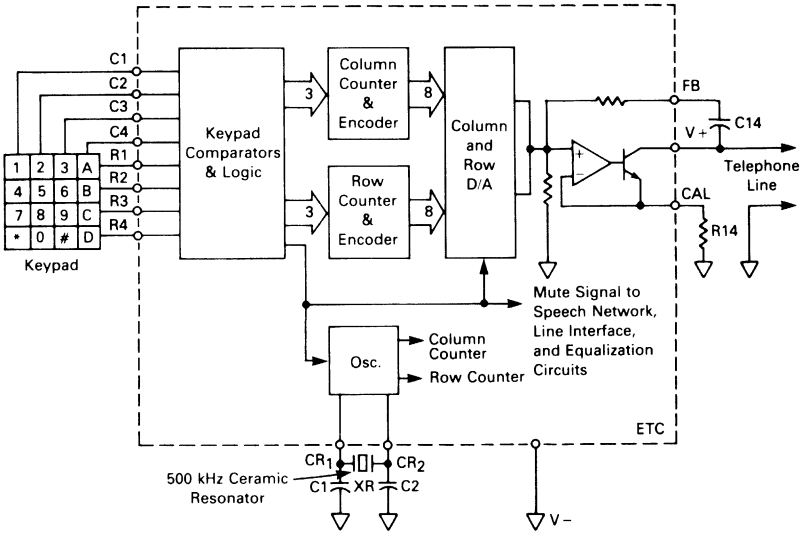


FIGURE 7 — TONE RINGER BLOCK DIAGRAM

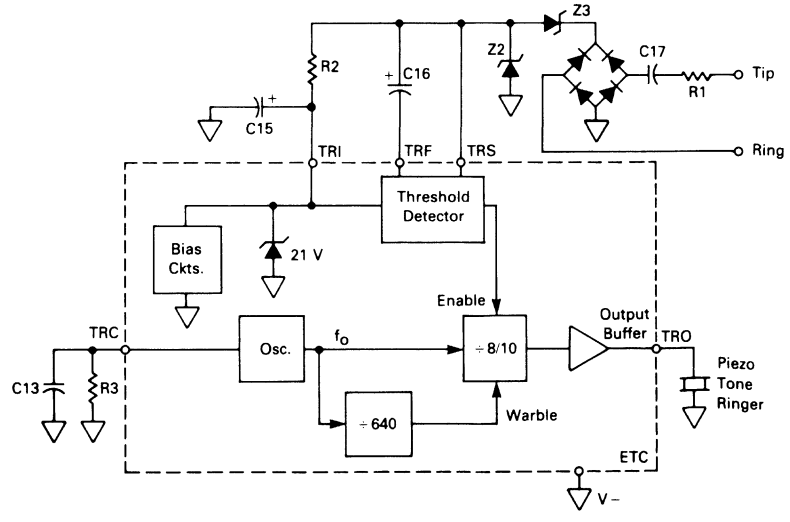


TABLE 1 — FREQUENCY SYNTHESIZER ERRORS

	DTMF Standard (Hz)	Tone Output Frequency with 500 kHz Oscillator	% Deviation from Standard
Row 1	697	696.4	−0.086
Row 2	770	769.2	−0.104
Row 3	852	853.2	+0.141
Row 4	941	939.8	−0.128
Column 1	1209	1207.7	−0.108
Column 2	1336	1336.9	+0.067
Column 3	1477	1479.3	+0.156
Column 4	1633	1634.0	+0.061

Tone Ringer

The tone ringer (Figure 7) generates a warbling square wave output drive to a piezo sound element when the ac line voltage exceeds a predetermined threshold level. The threshold detector uses a current mode comparator to prevent on/off chatter when the output current reduces the voltage available at the ringer input. When the average current into the tone ringer exceeds the threshold level, the ringer output TRO commences driving the piezo transducer. This output current sourced from TRI increases the average current measured by the threshold detector. As a result, hysteresis is produced beween the tone ringer on and off thresholds. The output frequency at TRO alternates between $f_O/8$ and $f_O/10$ at a warble rate of $f_O/640$, where f_O is the ringer oscillator frequency.

PIN DESCRIPTION

(See Figure 38 for external component identifications.)

PIN (PLCC)	PIN (DIP)	Designation	Function
1–4	1–4	R1–R4	Keypad inputs for Rows 1 through 4. When open, internal 8.0 kΩ resistors pull up the row inputs to a regulated (≈1.1 volt) supply. In normal operation, a row and a column input are connected through a SPST switch by the telephone keypad. Row inputs can also be activated by a Logic "0" (<500 mV) from a microprocessor port.
7–10	5–8	C1–C4	Keypad inputs for Columns 1 through 4. When open, internal 8.0 kΩ resistors pull down the column inputs to V−. In normal operation, connecting any column input to any row input produces the respective row and column DTMF tones. In addition to being connected to a row input, column inputs can be activated by a Logic "1" (>600 mV and <3.0 volt).
5, 6 11–15, 23,39	9–13	NC	No connection
16	14	ES	Sidetone Equalization terminal connects an external resistor between the junction of R8, R9 and V−. At loop currents greater than the equalization threshold this resistor is switched in to reduce the sidetone level. The resistor is switched out during dialing.
17	15	EV	Voice Equalization terminal connects an external resistor between V+ and V−, for loop length equalization. At loop currents greater than the equalization threshold this resistor is switched in to reduce the transmit and receive gains. The resistor is switched out during dialing.
18,19	16,17	CR1, CR2	Ceramic Resonator oscillator input and feedback terminals, respectively. The DTMF dialer is intended to operate with a 500 kHz ceramic resonator from which row and column tones are synthesized.
20	18	MM	Microphone Mute. The MM pin provides a means to mute the microphone and transmit amplifier in response to a digital control signal. When this pin is connected to a Logic "1" (>2.0 V) the microphone dc return path and the transmit amplifier output are disabled.
21	19	AGC	Automatic Gain Control low-pass filter terminal. Capacitor C3 connected between AGC and VR sets the attack and decay time of the transmit limiter circuit. This capacitor also aids in reducing clicks in the receiver due to hook-switch transients and DTMF on/off transients. In conjunction with internal resistors, C3 (1.0 μF) forms a timer which mutes the receiver amplifier for approximately 20 milliseconds after the user goes off-hook or releases a DTMF Key.
22	20	MIC	Microphone negative supply terminal. The dc current from the electret microphone is returned to V− through the MIC terminal which is connected to the collector of an on-chip NPN transistor. The base of this transistor is controlled either internally by the mute signal from the DTMF generator, or externally by the logic input pin MM.
24	21	TXL	Transmit Input Limiter. An internal variable resistance element at the TXL terminal controls the transmitter input level to prevent clipping with high signal levels. Coupling capacitors C4 and C5 prevent dc current flow through TXL. The dynamic range of the transmit peak limiter is controlled by resistors R12 and R13.
25	22	TXI	Transmit amplifier Input. TXI is the input to the transmit amplifier from an electret microphone. AC coupling capacitors allow the dc offset at TXI to be maintained approximately 0.6 V above V− by feedback through resistor R11 from TXO.
26	23	TXO	Transmit Amplifier Output. The transmit amplifier output drives ac current through the voltage regulator pass-transistor T1 via resistor R10. The dc bias voltage at TXO is typically 0.6 volts above V−. The transmit amplifier gain is controlled by the R11/(R12 + R13) ratio.

(continued)

PIN DESCRIPTION (continued)

PIN (PLCC)	PIN (DIP)	Designation	Function
27	24	STA	SideTone Amplifier output. STA is the output of the sidetone inverter amplifier whose input is driven by the transmit signal at TXO. The inverted transmit signal from STA subtracts from the receiver amplifier input current from V+, thus reducing the receiver sidetone level. Since the transmitted signal at V+ is phase shifted with respect to TXO by the reactive impedance of the phone line, the signal from STA must be similarly phase-shifted in order to provide adequate sidetone reduction. This phase relationship between the transmit signal at TXO and the sidetone cancellation signal from STA is controlled by R8, R9, and C6.
28	25	RM	Receiver Amplifier Mute. A switched resistance at the RM terminal attenuates the receiver amplifier input signal produced by DTMF dialing tones at V+. RM also mutes clicks at the receiver which result from keypad or hook switch transitions. The ac resistance at RM is typically 540 Ω in the mute mode and 200 kΩ otherwise. Coupling capacitors C7 and C8 prevent dc current flow through RM.
29	26	RXI	Receiver Amplifier Input. RXI is the input terminal of the receiver amplifier which is driven by ac signals from V+ and STA. Input coupling capacitor C8 allows RXI to be biased approximately 0.6 volts above the V− via feedback resistor R6.
30	27	RXO	Receiver Amplifier Output. This terminal is connected to the open-collector NPN output transistor of the receiver amplifier. DC bias current for the output device is sourced through the receiver from VR. The bias voltage at RXO is typically 0.6 volts above the V−. Capacitor C10 from RXO to VR provides frequency compensation for the receiver amplifier.
31	28	CAL	Amplitude CALibration terminal for DTMF dialer. Resistor R14 from the CAL pin to V− controls the DTMF output signal level at Tip and Ring.
32	29	VR	Voltage Regulator output terminal. VR is the output of a 1.1 volt voltage regulator which supplies power to the speech network amplifiers and DTMF generator during signaling. To improve regulator efficiency at low line current conditions, an external PNP pass-transistor T1 is used in the regulator circuit. Capacitor C9 frequency compensates the VR regulator to prevent oscillation.
33	30	V−	The dc common (more negative input) connected to Tip and Ring through the polarity guard bridge.
34	31	LC	DC Load Capacitor. Capacitor C11 from LC to V− forms a low-pass filter which prevents the resistor at LR from loading ac speech and DTMF signals.
35	32	LR	DC Load Resistor. Resistor R4 from LR to V− determines the dc input resistance at Tip and Ring. This resistor is external not only to enable programming the dc resistance but also to avoid high on-chip power dissipation with short telephone lines. It acts as a shunt load conducting the excess dc line current. At low line voltages (<3.0 volts), no current flows through LR.
36	33	BP	Base of a PNP Pass-transistor. Under long-loop conditions where low line voltages would cause VR to fall below 1.1 volts, BP drives the PNP transistor T1 into saturation, thereby minimizing the voltage drop across the pass transistor. At line voltages which maintain VR above 1.1 volts, BP biases T1 in the linear region thereby regulating the VR voltage. Transistor T1 also couples the ac speech signals from the transmit amplifier to Tip and Ring at V+.
37	34	V+	The more positive input to the regulator, speech, and DTMF sections connected to Tip and Ring through the polarity guard diode bridge.
38	35	FB	FeedBack terminal for DTMF output. Capacitor C14 connected from FB to V+ provides ac feedback to reduce the output impedance to Tip and Ring when tone dialing.
40	36	TRC	Tone Ringer oscillator Capacitor and resistor terminal. The relaxation oscillator frequency f_O is set by resistor R3 and capacitor C13 connected from TRC to V−. Typically, $f_O = (R3C13 + 8.0\ \mu s)^{-1}$.
41	37	TRS	Tone Ringer Input Sense. TRS is the most positive input terminal of the tone ringer and the reference for the threshold detector.
42	38	TRI	Tone Ringer Input terminal. TRI is the positive supply voltage terminal for tone ringer circuitry. Current is supplied to TRI through resistor R2. When the average voltage across R2 exceeds an internal reference voltage (typically 1.6 volts) the tone ringer output is enabled.
43	39	TRO	Tone Ringer Output terminal. The frequency of the square wave output signal at TRO alternates from $f_O/8$ to $f_O/10$ at a warble rate of $f_O/640$. Typical output frequencies are 1000 Hz and 800 Hz with a 12.5 Hz warble rate. TRO sources or sinks up to 20 mA to produce an output voltage swing of 18 volts peak-to-peak across the piezo transducer. Tone ringer volume control can be implemented by a variable resistor in series with the piezo transducer.
44	40	TRF	Tone Ringer Input Filter capacitor terminal. Capacitor C16 connected from TRF to TRS forms a low-pass filter. This filter averages the signal across resistor R2 and presents this dc voltage to the input of the threshold detector. Line voltage transients are rejected if the duration is insufficient to charge C16 to 1.6 volts.

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

KEYPAD INTERFACE CIRCUIT

Characteristic	Test Method	Symbol	Min	Typ	Max	Unit
Row Input Pullup Resistance m^{th} Row Terminal: m = 1,2,3,4	7	R_{Rm}	5.0	8.0	11	kΩ
Column Input Pulldown Resistance n^{th} Column Terminal: n = 1,2,3,4	8	R_{Cn}	5.0	8.0	11	kΩ
Ratio of Row-to-Column Input Resistances $K_{m,n} = \frac{R_{Rm}}{R_{Cn}}$, m = 1,2,3,4 n = 1,2,3,4	7 & 8	$K_{m,n}$	0.88	1.0	1.12	—
Row Terminal Open Circuit Voltage	7a	V_{ROC}	950	1100	1200	mVdc
Row Threshold Voltage for m^{th} Row Terminal: m = 1,2,3,4	9	V_{Rm}	0.70 V_{ROC}	—	—	Vdc
Column Threshold Voltage for n^{th} Column Terminal: n = 1,2,3,4	10	V_{Cn}	—	—	0.30 V_{ROC}	Vdc

LINE VOLTAGE REGULATOR

Voltage Regulator Output	1a	V_R	1.0	1.1	1.2	Volts
V+ Current in DTMF Mode	2a	I_{DT}	8.0	12	14.5	mA
Change in I_{DT} with Change in V+ Voltage	2b	ΔI_{DT}	—	0.8	2.0	mA
V+ Current in Speech Mode		I_{SP}				mA
V+ = 1.7 V	1b		3.0	5.0	7.0	
V+ = 5.0 V	1c		8.0	11	15	
Speech to DTMF Mode Current Difference	3	ΔI_{TR}	−2.0	2.0	3.5	mA
LR Level Shift		ΔV_{LR}				Vdc
V+ = 5.0 V, I_{LR} = 10 mA	4a		2.4	2.9	3.5	
V+ = 18 V, I_{LR} = 110 mA	4b		2.6	3.3	4.0	
LC Terminal Resistance	5	R_{LC}	30	50	75	kΩ
Load Regulation	6	ΔV_R	−20	−6.0	20	mVdc

3

ELECTRICAL CHARACTERISTICS (continued)

SPEECH NETWORK

Characteristic	Test Method	Symbol	Min	Typ	Max	Unit
MIC Terminal Saturation Voltage	20	V_{MIC}	—	60	125	mVdc
MIC Terminal Leakage Current	21a	I_{MIC}	—	0.0	5.0	μA
MM Terminal Input Resistance	21b	R_{MM}	50	100	170	kΩ
TXO Terminal Bias	22a	B_{TXO}	0.48	0.53	0.68	—
TXI Terminal Input Bias Current	22b	I_{TXI}	—	50	400	nA
TXO Terminal Positive Swing	22c	$V_{TXO(+)}$	—	25	60	mVdc
TXO Terminal Negative Swing	22d	$V_{TXO(-)}$	—	130	200	mVdc
Transmit Amplifier Closed-Loop Gain	23a	G_{TX}	16.5	19	20	V/V
Sidetone Amplifier Gain	23b	G_{STA}	0.40	0.45	0.54	V/V
STA Terminal Output Current	24	I_{STA}	50	100	250	μA
RXO Terminal Bias	25a	B_{RXO}	0.48	0.52	0.68	—
RXI Terminal Input Bias Current	25b	I_{RXI}	—	100	400	nA
RXO Terminal Positive Swing	25c	$V_{RXO(+)}$	—	1.0	20	mVdc
RXO Terminal Negative Swing	25d	$V_{RXO(-)}$	—	40	100	mVdc
TXL Terminal OFF Resistance	26a	$R_{TXL(OFF)}$	125	200	300	kΩ
TXL Terminal ON Resistance	26b	$R_{TXL(ON)}$	—	20	100	Ω
RM Terminal OFF Resistance	27a	$R_{RM(OFF)}$	125	180	300	kΩ
RM Terminal ON Resistance	27b	$R_{RM(ON)}$	410	570	770	Ω

DTMF GENERATOR

Row Tone Frequency	Row 1	11a, 11b	f_{Rm}	692.9	696.4	699.9	Hz
	Row 2			765.3	769.2	773.0	
	Row 3			848.9	853.2	857.5	
	Row 4			935.1	939.8	944.5	
Column Tone Frequency	Column 1	11c, 11d	f_{Cn}	1201.6	1207.7	1213.7	Hz
	Column 2			1330.2	1336.9	1343.6	
	Column 3			1471.9	1479.3	1486.7	
	Column 4			1625.2	1633.4	1641.5	
Row Tone Amplitude		11e	V_{Row}	0.38	0.45	0.55	V_{rms}
Column Tone Amplitude		11f	V_{Col}	0.48	0.55	0.67	V_{rms}
Column Tone Pre-emphasis		11g	dB_{CR}	0.5	1.8	3.0	dB
DTMF Distortion		12	% Dis	—	4.0	6.0	%
DTMF Output Resistance		13	R_o	1.0	2.5	3.0	kΩ

EQUALIZATION CONTROL

ES Terminal OFF Resistance	34a	$R_{ES(OFF)}$	100	200	325	kΩ
Equalization Threshold Voltage	34b	V_E	1.4	1.6	2.0	Vdc
Equalization Threshold Hysteresis	34c	ΔV_E	75	200	300	mVdc
EV Terminal OFF Resistance	35a	$R_{EV(OFF)}$	100	200	325	kΩ
EV Terminal ON Resistance	35b	$R_{EV(ON)}$	—	20	50	Ω

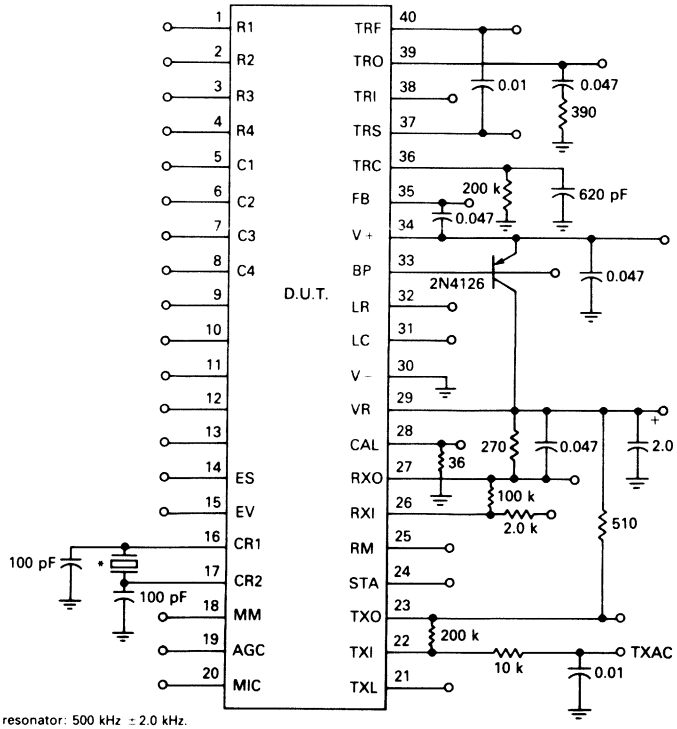
ELECTRICAL CHARACTERISTICS (continued)

TONE RINGER

Characteristic	Test Method	Symbol	Min	Typ	Max	Unit
TRI Terminal Voltage	14	V_{TRI}	20	21.5	23	Vdc
TRS Terminal Input Current		I_{TRS}				
V_{TRS} = 24 volts	15a		70	120	170	μA
V_{TRS} = 30 volts	15b		0.4	0.8	1.5	mA
TRF Threshold Voltage	16a	V_{TRF}	1.2	1.6	1.9	Vdc
TRF Threshold Hysteresis	16b	ΔV_{TRF}	100	200	400	mVdc
TRF Filter Resistance	17	R_{TRF}	30	50	75	kΩ
High Tone Frequency	18	f_H	920	1000	1080	Hz
Low Tone Frequency	18	f_L	736	800	864	Hz
Warble Frequency	18	f_W	11.5	12.5	13.5	Hz
Tone Ringer Output Voltage	19	$V_{o(p-p)}$	18	20	22	Vp-p

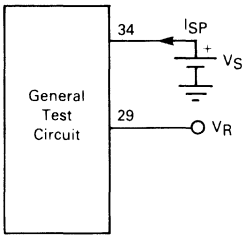
3

FIGURE 8 — GENERAL TEST CIRCUIT



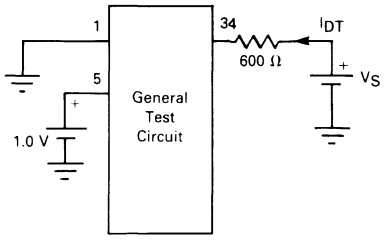
Notes:
1. *Selected ceramic resonator: 500 kHz ± 2.0 kHz.
2. Capacitances in μF unless noted.
3. All resistances in ohms.
4. Pin numbers in this Figure and in Test Circuits are for the DIP package.

FIGURE 9 — TEST ONE



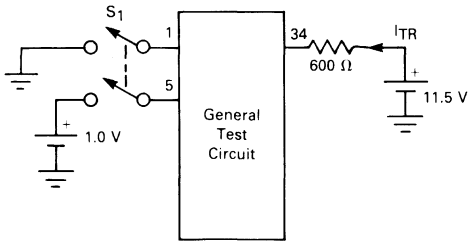
a. Measure V_R with V_S = 1.7 V
b. Measure I_{SP} with V_S = 1.7 V
c. Measure I_{SP} with V_S = 5.0 V

FIGURE 10 — TEST TWO



a. Measure I_{DT} with V_S = 11.5 V
b. Measure I_{DT} with V_S = 26 V. Calculate $\Delta I_{DT} = |I_{DT}|_{26\ V} - |I_{DT}|_{11.5\ V}$

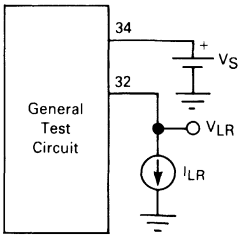
FIGURE 11 — TEST THREE



With S_1 open measure I_{TR}. Close S_1 and again measure I_{TR}. Calculate:

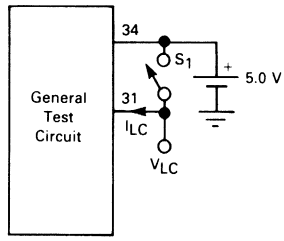
$$\Delta I_{TR} = |I_{TR}|_{S_1\ Closed} - |I_{TR}|_{S_1\ Open}$$

FIGURE 12 — TEST FOUR



a. Set V_S = 5.0 V and I_{LR} = 10 mA. Measure V_{LR}. Calculate $\Delta V_{LR} = V_S - V_{LR}$
b. Repeat Test 4a with V_S = 18 V and I_{LR} = 110 mA

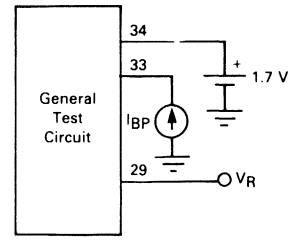
FIGURE 13 — TEST FIVE



With S_1 open measure V_{LC}.
Close S_1 and measure I_{LC}.
Calculate:

$$R_{LC} = \frac{5.0 - V_{LC}}{I_{LC}}$$

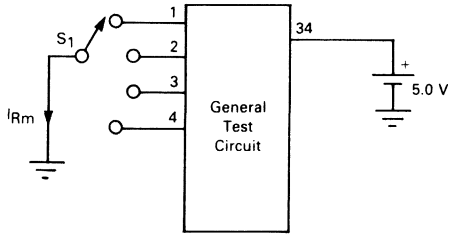
FIGURE 14 — TEST SIX



Set I_{BP} = 0.0 μA and measure V_R.
Set I_{BP} = 150 μA and measure V_R. Calculate:

$$\Delta V_R = |V_R|_{0.0\ \mu A} - V_R|_{150\ \mu A}|$$

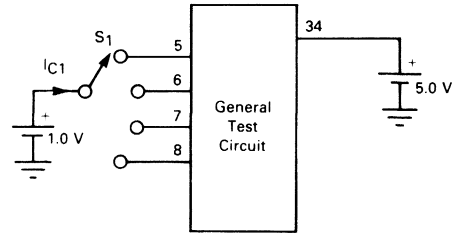
FIGURE 15 — TEST SEVEN



Subscript m corresponds to row number.

a. Set S_1 to Terminal 2 and measure voltage at Terminal 1 (V_{ROC}).
b. Set S_1 to Terminal 1 (m = 1) and measure I_{R1}. Calculate:
$R_{R1} = V_{ROC} \div I_{R1}$
c,d,e. Repeat Test 7b for m = 2,3,4.

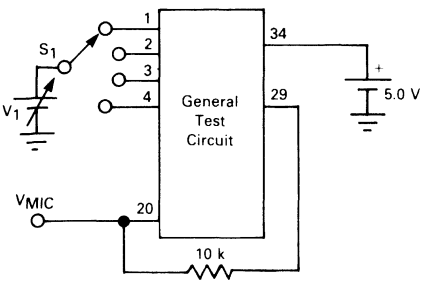
FIGURE 16 — TEST EIGHT



Subscript n corresponds to column number.

a. Set S_1 to Terminal 5 (n = 1) and measure I_{C1}. Calculate:
$R_{C1} = 1.0\ V \div I_{C1}$
b,c,d. Repeat Test 8a for n = 2,3,4.

FIGURE 17 — TEST NINE

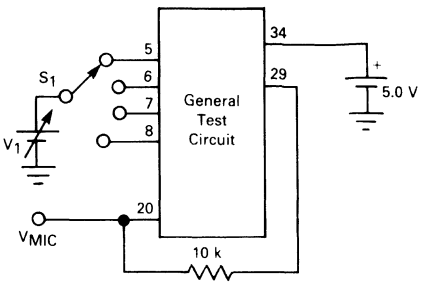


m corresponds to row number.

a. Set S_1 to Terminal 1 (m = 1) with V_1 = 1.0 Vdc. Verify V_{MIC} is Low (V_{MIC} < 0.3 Vdc). Decrease V_1 to 0.70 V_{ROC} and verify V_{MIC} switches high. (V_{MIC} > 0.5 Vdc). V_{ROC} is obtained from Test 7a.

b,c,d. Repeat Test 9a for rows 2,3, and 4. (m = 2,3,4)

FIGURE 18 — TEST TEN

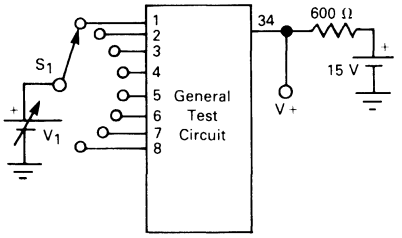


n corresponds to column number.

a. Set S_1 to Terminal 5 (n = 1) with V_1 = 0 Vdc. Verify V_{MIC} is low (V_{MIC} < 0.3 Vdc). Increase V_1 to 0.30 V_{ROC} and verify V_{MIC} switches high, (V_{MIC} > 0.5 Vdc). V_{ROC} is obtained from Test 7a.

b,c,d. Repeat Test 10a for columns 2,3, and 4. (n = 2,3,4)

FIGURE 19 — TEST ELEVEN



m corresponds to row number.
n corresponds to column number.

a. With V_1 = 0.0 V set S_1 to Terminal 1 (m = 1) and measure frequency of tone at V+.

b. Repeat Test 11a for rows 2,3 and 4. (m = 2,3,4).

c. With V_1 = 1.0 V set S_1 to Terminal 5. (n = 1) and measure frequency of tone at V+.

d. Repeat Test for columns 2,3, and 4. (n = 2,3,4).

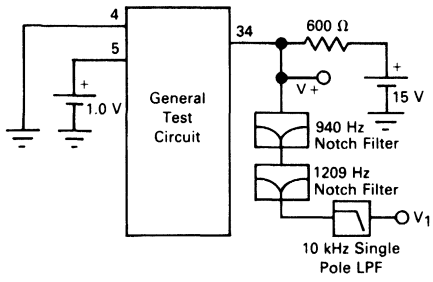
e. Set S_1 to Terminal 4 and V_1 = 0.0 V. Measure row tone amplitude at V+ (V_{ROW}).

f. Set S_1 to Terminal 8 and V_1 = 1.0 V. Measure column tone amplitude at V+. (V_{COL}).

g. Using results of Tests 11e and 11f, calculate:

$$dB_{CR} = 20 \log_{10} \frac{V_{COL}}{V_{ROW}}$$

FIGURE 20 — TEST TWELVE

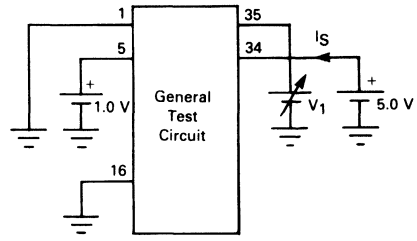


Note: The notch filters must have 50 dB attenuation at their respective center frequencies.

Measure V+ and V_1 with a true rms voltmeter. Calculate:

$$\% \text{ DIS} = \frac{V_1(\text{rms})}{V+(\text{rms})} \times 100$$

FIGURE 21 — TEST THIRTEEN

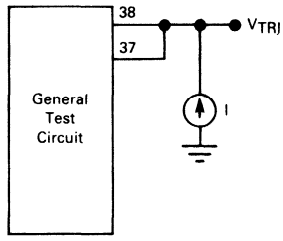


Measure I_S at V_1 = 1.8 V and V_1 = 2.8 V.

Calculate:

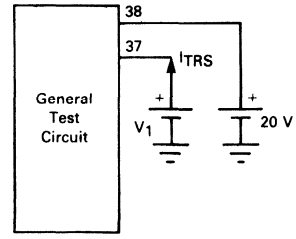
$$R_O = 1.0 \text{ V} \div \left[I_S \Big|_{2.8 \text{ V}} - I_S \Big|_{1.8 \text{ V}} \right]$$

FIGURE 22 — TEST FOURTEEN



Set I = 1.0 mA and measure V_{TRI}.

FIGURE 23 — TEST FIFTEEN

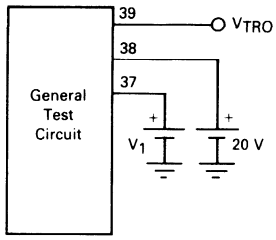


a. Measure I_{TRS} with V_1 = 24 V.

b. Measure I_{TRS} with V_1 = 30 V.

3

FIGURE 24 — TEST SIXTEEN



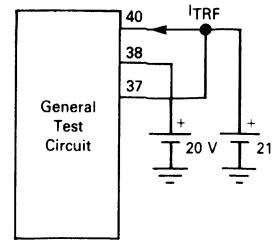
a. Increase V_1 from 21 V until V_{TRO} switches on. Note that V_{TRO} will be an 16 V_{pp} square wave. Record this value of V_1. Calculate:

$V_{TRF} = V_1 - 20\ V$

b. Decrease V_1 from its setting in Test 16a until V_{TRO} ceases switching. Record this value of V_1. Calculate:

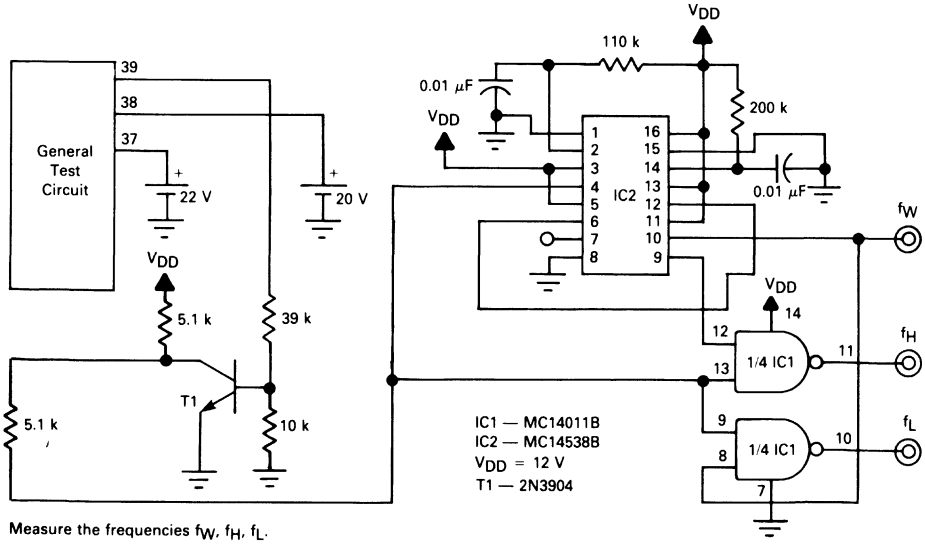
$\Delta V_{TRF} = V_{1\ Test\ 16a} - V_{1\ Test\ 16b}$

FIGURE 25 — TEST SEVENTEEN



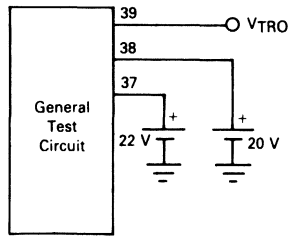
Measure I_{TRF}. Calculate: $R_{TRF} = 1.0 \div I_{TRF}$.

FIGURE 26 — TEST EIGHTEEN



Measure the frequencies f_W, f_H, f_L.

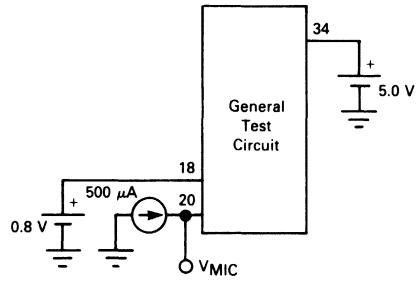
FIGURE 27 — TEST NINETEEN



Measure V_{TRO} peak-to-peak voltage swing. Using V_{TRI} from Test 14 Calculate:

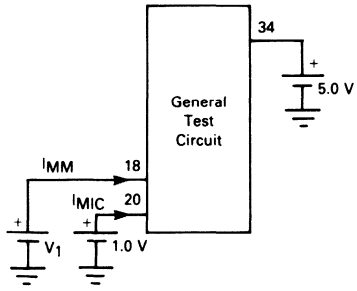
$V_{o(p-p)} = V_{TRI} - 20\ V + V_{TRO}$

FIGURE 28 — TEST TWENTY



Measure V_{MIC}

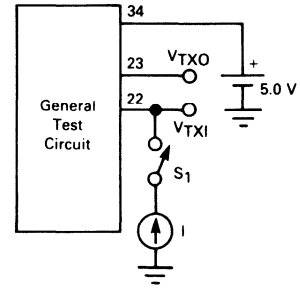
FIGURE 29 — TEST TWENTY-ONE



a. Set V_1 = 2.0 V and measure I_{MIC}.

b. Set V_1 = 5.0 V and measure I_{MM}. Calculate: $R_{MM} = 5.0\ V \div I_{MM}$

FIGURE 30 — TEST TWENTY-TWO



a. With S_1 open, measure V_{TXO}. Using V_R obtained in Test 1 Calculate: $B_{TXO} = V_{TXO} \div V_R$

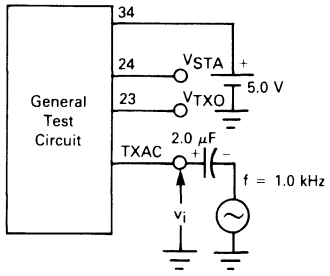
b. With S_1 open, measure V_{TXO} and V_{TXI}. Calculate: $I_{TXI} = (V_{TXO} - V_{TXI}) \div 200\ k\Omega$

c. Close S_1 and set I = −10 μA. Measure V_{TXO}. Calculate: $V_{TXO(+)} = V_R - V_{TXO}$ where V_R is obtained from Test 1.

d. Close S_1 and set I = +10 μA. Measure V_{TXO}. $V_{TXO(-)} = V_{TXO}$.

3

FIGURE 31 — TEST TWENTY-THREE



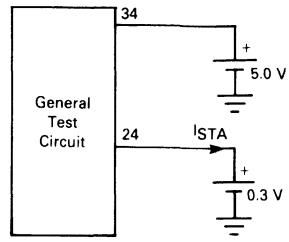
a. Set the generator for v_i = 3.0 mV_{rms}. Measure ac voltage V_{TXO}. Calculate:

$$G_{TX} = \frac{V_{TXO}}{v_i}$$

b. Measure ac voltage V_{STA}. Using V_{TXO} from Test 23a calculate:

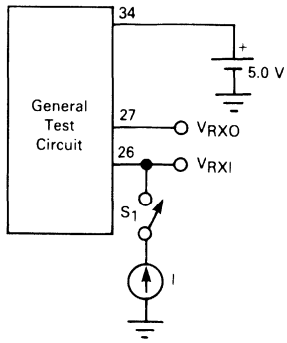
$$G_{STA} = \frac{V_{STA}}{V_{TXO}}$$

FIGURE 32 — TEST TWENTY-FOUR



Measure I_{STA}.

FIGURE 33 — TEST TWENTY-FIVE



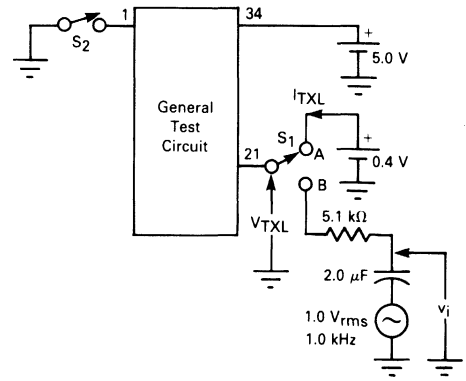
a. With S_1 open, measure V_{RXO}. Using V_R obtained in Test 1, calculate: $B_{RXO} = V_{RXO} \div V_R$.

b. With S_1 open, measure V_{RXO} and V_{RXI}. Calculate: $I_{RXI} = (V_{RXO} - V_{RX1}) \div 100\ k\Omega$

c. Close S_1 and set I = −10 μA. Measure V_{RXO}. Using V_R obtained in Test 1, calculate: $V_{RXO}(+) = V_R - V_{RXO}$.

d. Close S_1 and set I = +10 μA and measure V_{RXO}. $V_{RXO}(-) = V_{RXO}$.

FIGURE 34 — TEST TWENTY-SIX

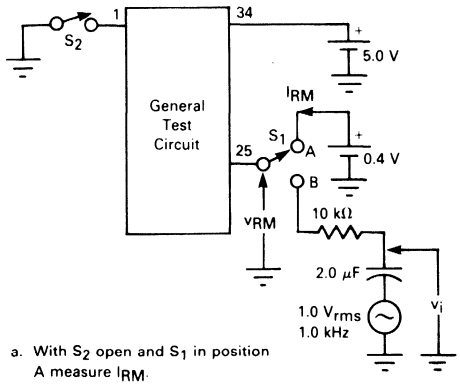


a. Set S_1 to position A with S_2 open. Measure I_{TXL}. Calculate: R_{TXL} (OFF) = 0.4 V ÷ I_{TXL}.

b. Set S_1 to position B and close S_2. Measure ac voltages v_i and V_{TXL}. Calculate:

$$R_{TXL}\ (ON) = \frac{V_{TXL}}{v_i - V_{TXL}} \times 5.1\ k\Omega$$

FIGURE 35 — TEST TWENTY-SEVEN

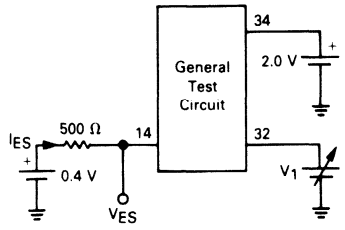


a. With S_2 open and S_1 in position A measure I_{RM}.
Calculate: $R_{RM(OFF)} = 0.4\ V \div I_{RM}$

b. Close S_2 and switch S_1 to position B. Measure ac voltages v_i and V_{RM}.
Calculate:
$$R_{RM(ON)} = \frac{V_{RM}}{v_i - V_{RM}} \times 10\ k\Omega$$

Note: Tests 28–33 intentionally omitted.

FIGURE 36 — TEST THIRTY-FOUR

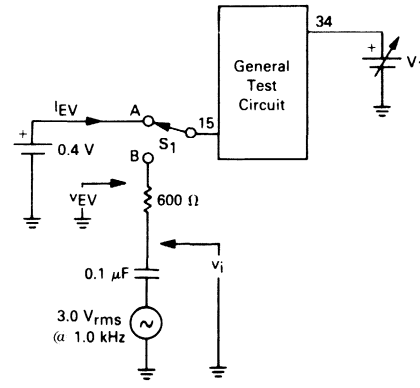


a. Set V_1 = 0 V. Measure I_{ES}. Calculate R (OFF) = 0.4 ÷ I_{ES}.

b. Increase V_1 until V_{ES} SWITCHES low (<200 mV). Measure V_1. $V_E = V_1$.

c. Decrease V_1 from the value in Test 34b until V_{ES} switches high (>200 mV). Measure V_1. Calculate $\Delta V_E = V_1 - V_1$
Test 34b Test 34c

FIGURE 37 — TEST THIRTY-FIVE



a. With S_1 in position A set V_1 = 2.0 V. Measure I_{EV} Calculate $R_{EV(OFF)} = 0.4 \div I_{EV}$.

b. Set V_1 = 5.0 V and Set S_1 to position B. Measure v_i and v_{EV}. Calculate
$$R_{EV(ON)} = \frac{v_{EV}}{v_i - v_{EV}} \times 600\ \Omega$$

APPLICATIONS INFORMATION

Figure 38 specifies a typical application circuit for the MC34011A. Complete listings of external components are provided at the end of this section along with nominal component values.

The hook switch and polarity guard bridge configuration is one of several options. If two bridges are used, one for the tone ringer and the other for speech and dialer circuits, then the hook switch can be simplified. Component values should be varied to optimize telephone performance parameters for each application. The relationships between the application circuit components and certain telephone parameters are briefly described in the following:

3

On-Hook Input Impedance

R1, C17, and Z3 are the significant components for on-hook impedance. C17 dominates at low frequencies, R1 at high frequencies and Z3 provides the non-linearity required for 2.5 V and 10 V impedance signature tests. C17 must generally be $\leq$ 1.0 μF to satisfy 5.0 Hz impedance specifications. (EIA RS-470)

Tone Ringer Output Frequencies

R3 and C13 control the frequency (f_O) of a relaxation oscillator. Typically $f_O = (R3C13 + 8.0\ \mu s)^{-1}$. The output tone frequencies are $f_O/10$ and $f_O/8$. The warble rate is $f_O/640$. The tone ringer will operate with f_O from 1.0 kHz to 10 kHz. R3 should be limited to values between 150 k and 300 k.

Tone Ringer Input Threshold

After R1, C17, and Z3 are chosen to satisfy on-hook impedance specifications, R2 is chosen for the desired ring start threshold. Increasing R2 reduces the ac input voltage required to activate the tone ringer output. R2 should be limited to values between 0.8 k and 2.0 kΩ.

Off-Hook DC Resistance

R4 conducts the dc line current in excess of the speech and dialer bias current. Increasing R4 increases the input resistance of the telephone for line currents above 10 mA. R4 should be selected between 30 Ω and 120 Ω.

Off-Hook AC Impedance

The ac input impedance is equal to the receive amplifier load impedance (at RXO) divided by the receive amplifier gain (voltage gain from V+ to RXO). Increasing the impedance of the receiver increases the impedance of the telephone. Increasing the gain of the receiver amplifier decreases the impedance of the telephone.

DTMF Output Amplitude

R14 controls the amplitude of the row and column DTMF tones. Decreasing R14 increases the level of tones generated at V+. The ratio of the row and column tone amplitudes is internally fixed. R14 should be greater than 20 Ω to avoid excessive current in the DTMF output amplifier.

Transmit Output Level

R10 controls the maximum signal amplitude produced at V+ by the transmit amplifier. Decreasing R10 increases the transmit output signal at V+. R10 should be greater than 220 Ω to limit current in the transmit amplifier output.

Transmit Gain

The gain from the microphone to the telephone line varies directly with R11. Increasing R11 increases the signal applied to R10 and the ac current driven through R10 to the telephone line. The closed loop-gain from the microphone to the TXO terminal should be greater than 10 to prevent transmit amplifier oscillations.

Note: Adjustments to transmit level and gain are complicated by the addition of receiver sidetone current to the transmit amplifier output current at V+. Normally the sidetone current from the receiver will increase the transmit signal (if the current in the receiver is in phase with that in R10). Thus the transmit gain and sidetone levels cannot be adjusted independently.

Receiver Gain

Feedback resistor R6 adjusts the gain at the receiver amplifier. Increasing R6 increases the receiver amplifier gain.

Sidetone Level

Sidetone reduction is achieved by the cancellation of receiver amplifier input signals from R9 and R5. R8, R15, and C6 determine the phase of the sidetone balance signal in R9. The ac voltage at the junction of R8 and R9 should be 180° out of phase with the voltage at V+. R9 is selected such that the signal current in R9 is slightly greater than that in R5. This insures that the sidetone current in the receiver adds to the transmit amplifier output current.

Equalization of Speech Network

Resistors R17 and R18 are switched into the circuit when the voltage at the LR terminal exceeds the equalization threshold voltage (typically 1.65 V). R17 reduces the transmit and receive gains for loop currents greater than the threshold (short loops) by attenuating signals at tip and ring. R18 reduces the sidetone level which would otherwise increase when R17 is switched into the circuit. The voltage V_{LR} at LR terminal is given by

$V_{LR} = (I_L - I_S) \times R4$.

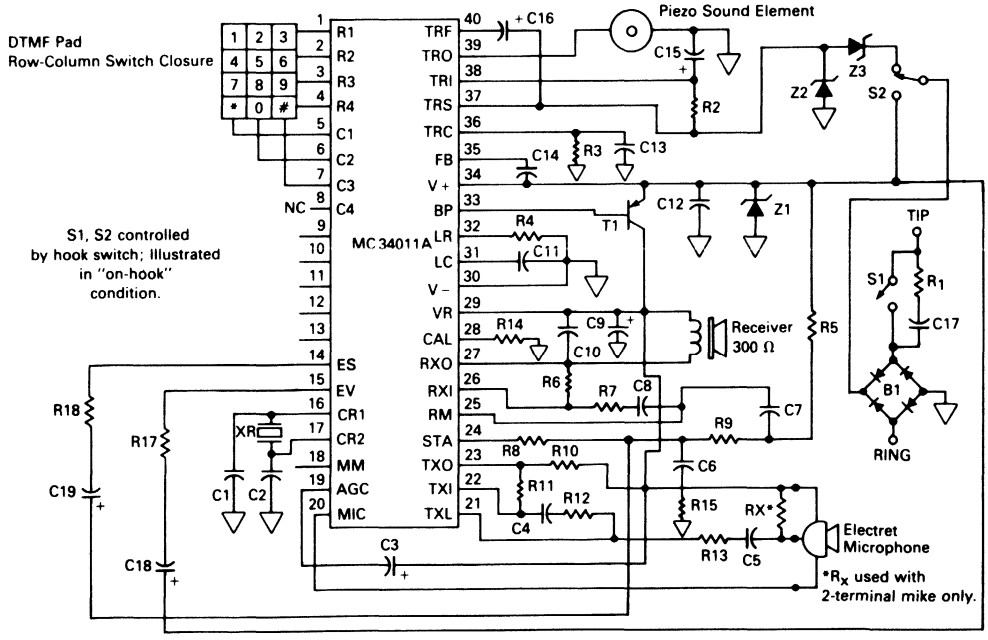
where I_L = loop current

I_S = dummy load current (6.0 mA) + speech network current (4.0 mA).

Thus resistor R4 is selected to activate the equalization circuit at the desired loop current. However, R4 must be selected keeping in mind the fact that it also controls the dc resistance of the telephone. Capacitors C18 and C19 prevent dc current flow into the EV and ES terminals. This reduces clicks and also prevents changes in the dc characteristic of the telephone when the EV and ES terminals are switched to low impedance.

3

FIGURE 38 — ELECTRONIC TELEPHONE APPLICATION CIRCUIT



EXTERNAL COMPONENTS

(Component Labels Referenced to Figure 38)

Capacitors	Nominal Value	Description
C1, C2	100 pF	Ceramic Resonator oscillator capacitors.
C3	1.0 μF, 3.0 V	Transmit limiter low-pass filter capacitor: controls attack and decay time of transmit peak limiter.
C4, C5	0.1 μF	Transmit amplifier input capacitors: prevent dc current flow into TXL pin and attenuate low-frequency noise on microphone lead.
C6	0.05 μF	Sidetone network capacitor: provides phase-shift in sidetone path to match that caused by telephone line reactance.
C7, C8	0.05 μF	Receiver amplifier input capacitors: prevent dc current flow into RM terminal and attenuates low frequency noise on the telephone line.
C9	2.2 μF, 3.0 V	VR regulator capacitor: frequency compensates the VR regulator to prevent oscillation.
C10	0.01 μF	Receiver amplifier output capacitor: frequency compensates the receiver amplifier to prevent oscillation.
C11	0.1 μF	DC load filter capacitor: prevents the dc load circuit from attenuating ac signals on V+.
C12	0.01 μF	Telephone line bypass capacitor: terminates telephone line for high frequency signals and prevents oscillation in the VR regulator.
C13	620 pF	Tone ringer oscillator capacitor: determines clock frequency for tone and warble frequency synthesizers.
C14	0.1 μF	DTMF output feedback capacitor: ac couples feedback around the DTMF output amplifier which reduces output impedance.
C15	4.7 μF, 25 V	Tone ringer input capacitor: filters the rectified tone ringer input signal to smooth the supply potential for oscillator and output buffer.
C16	1.0 μF, 10 V	Tone ringer filter capacitor: integrates the voltage from current sense resistor R2 at the input of the threshold detector.
C17	1.0 μF, 250 Vac Non-polarized	Tone ringer line capacitor: ac couples the tone ringer to the telephone line; partially controls the on-hook input impedance of telephone.
C18	25 μF, 25 V	Speech equalization coupling capacitor. Prevents dc current flow into EV terminal. (optional)
C19	5.0 μF, 3.0 V	Sidetone equalization coupling capacitor. Prevents dc current flow into ES terminal. (optional)

Resistors	Nominal Value	Description
R1	6.8 k	Tone ringer input resistor: limits current into the tone ringer from transients on the telephone line and partially controls the on-hook impedance of the telephone.
R2	1.8 k	Tone ringer current sense resistor: produces a voltage at the input of the threshold detector in proportion to the tone ringer input current.
R3	200 k	Tone ringer oscillator resistor: determines the clock frequency for tone and warble frequency synthesizers.
R4	82, 1.0 W	DC load resistor: conducts all dc line current in excess of the current required for speech or dialing circuits; controls the off-hook dc resistance of the telephone.
R5, R7	150 k, 56 k	Receiver amplifier input resistors: couple ac input signals from the telephone line to the receiver amplifier; signal in R5 subtracts from that in R9 to reduce sidetone in receiver.
R6	200 k	Receiver amplifier feedback resistor: controls the gain of the receiver amplifier.
R8, R9	1.5 k, 30 k	Sidetone network resistors: drive receiver amplifier input with the inverted output signal from the transmitter; phase of signal in R9 should be opposite that in R5.
R10	270	Transmit amplifier load resistor: converts output voltage of transmit amplifier into a current that drives the telephone line; controls the maximum transmit level.
R11	200 k	Transmit amplifier feedback resistor: controls the gain of the transmit amplifier.
R12, R13	4.7 k, 4.7 k	Transmit amplifier input resistors: couple signal from microphone to transmit amplifier; control the dynamic range of the transmit peak limiter.
R14	36	DTMF calibration resistor: controls the output amplitude of the DTMF dialer.
R15	2.0 k	Sidetone network resistor (optional): reduces phase shift in sidetone network at high frequencies.
R17	600	Speech equalization resistor. Reduces transmit and receive gain when EV terminal switches on. (optional)
R18	5.1 k	Sidetone equalization resistor. Reduces sidetone level when ES terminal switches on. (optional)
R_X	3.0 k	Microphone bias resistor: sources current from VR to power a 2-terminal electret microphone; R_X is not used with 3-terminal microphones.

EXTERNAL COMPONENTS (continued)

Semiconductors	Electret Mic	Receiver
B1 = MDA101A, or equivalent, or 4-1N4005 T1 = 2N4126 or equivalent Z1 = 18 V, 1.5 W, 1N5931A Z2 = 30 V, 1.5 W, 1N5936A Z3 = 4.7 V, 1/2 W, 1N750 XR — muRata Erie CSB 500 kHz Resonator, or equivalent Piezo — PBL 5030BC Toko Buzzer or equivalent	2 Terminal, Primo EM-95 (Use R_X) or equivalent 3 Terminal, Primo 07A181P (Remove R_X) or equivalent	Primo Model DH-34 (300 Ω) or equivalent

Motorola Inc. does not endorse or warrant the suppliers referenced.

MOTOROLA

MC34012-1
MC34012-2
MC34012-3

Advance Information

TELEPHONE TONE RINGER

- Complete Telephone Bell Replacement Circuit with Minimum External Components
- On-Chip Diode Bridge and Transient Protection
- Direct Drive for Piezoelectric Transducers
- Base Frequency Options—MC34012-1: 1.0 kHz
  MC34012-2: 2.0 kHz
  MC34012-3: 500 Hz
- Input Impedance Signature Meets Bell and EIA Standards
- Rejects Rotary Dial Transients

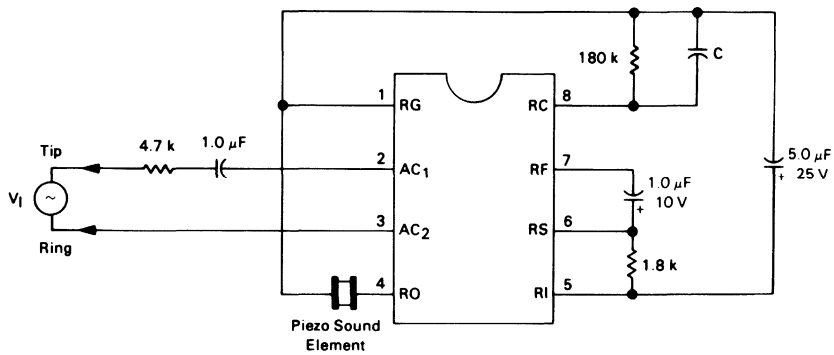
TELEPHONE TONE RINGER

BIPOLAR LINEAR/I^2L

P SUFFIX
PLASTIC PACKAGE
CASE 626-04

D SUFFIX
PLASTIC PACKAGE
CASE 751A-01

APPLICATION CIRCUIT



MC34012-1: C = 1000 pF
MC34012-2: C = 500 pF
MC34012-3: C = 2000 pF

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ADI735

CIRCUIT DESCRIPTION

The MC34012 Tone Ringer derives its power supply by rectifying the ac ringing signal. It uses this power to activate a tone generator and drive a piezo-ceramic transducer. The tone generation circuitry includes a relaxation oscillator and frequency dividers which produce high and low frequency tones as well as the tone warble frequency. The relaxation oscillator frequency f_O is set by resistor R2 and capacitor C2 connected to pin RC. The oscillator will operate with f_O from 1.0 kHz to 10 kHz with the proper choice of external components (See Figure 1).

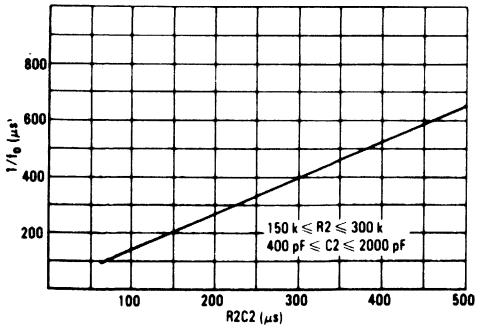
The frequency of the tone ringer output signal at pin RO alternates between $f_O/4$ to $f_O/5$. The warble rate at which the frequency changes is $f_O/320$ for the MC34012-1, $f_O/640$ for the MC34012-2, or $f_O/160$ for the MC34012-3. With a 4.0 kHz oscillator frequency, the MC34012-1 produces 800 Hz and 1000 Hz tones with a 12.5 Hz warble rate. The MC34012-2 generates 1600 Hz and 2000 Hz tones with a similar 12.5 Hz warble frequency from an 8.0 Hz oscillator frequency. The MC34012-3 will produce 400 Hz and 500 Hz tones with a 12.5 Hz warble rate from a 2.0 kHz oscillator frequency. The tone ringer output circuit can source or sink 20 mA with an output voltage swing of 20 volts peak-to-peak. Volume control is readily implemented by adding a variable resistance in series with the piezo transducer.

Input signal detection circuitry activates the tone ringer output when the ac line voltage exceeds programmed threshold level. Resistor R3 determines the ringing signal amplitude at which an output signal will be generated at RO. The ac ringing signal is rectified by the internal diode bridge. The rectified input signal produces a current through R3 which is input at terminal RI. The voltage across resistor R3 is filtered by capacitor C3 at the input to the threshold circuit. When the voltage on capacitor C3 exceeds 1.7 volts, the threshold comparator enables the tone ringer output. Line transients produced by pulse dialing telephones do not charge capacitor C3 sufficiently to activate the tone ringer output.

Capacitors C1 and C4 and resistor R1 determine the 10 volt, 24 Hz signature test impedance. C4 also provides filtering for the output stage power supply to prevent droop in the square wave output signal. Six diodes in series with the rectifying bridge provide the necessary non-linearity for the 2.5 volt, 24 Hz signature tests.

An internal shunt voltage regulator between the RI and RG terminals provides dc voltage to power output stage, oscillator, and frequency dividers. The dc voltage at RI is limited to approximately 22 volts in regulation. To protect the IC from telephone line transients, an SCR is triggered when the regulator current exceeds 50 mA. The SCR diverts current from the shunt regulator and reduces the power dissipation within the IC.

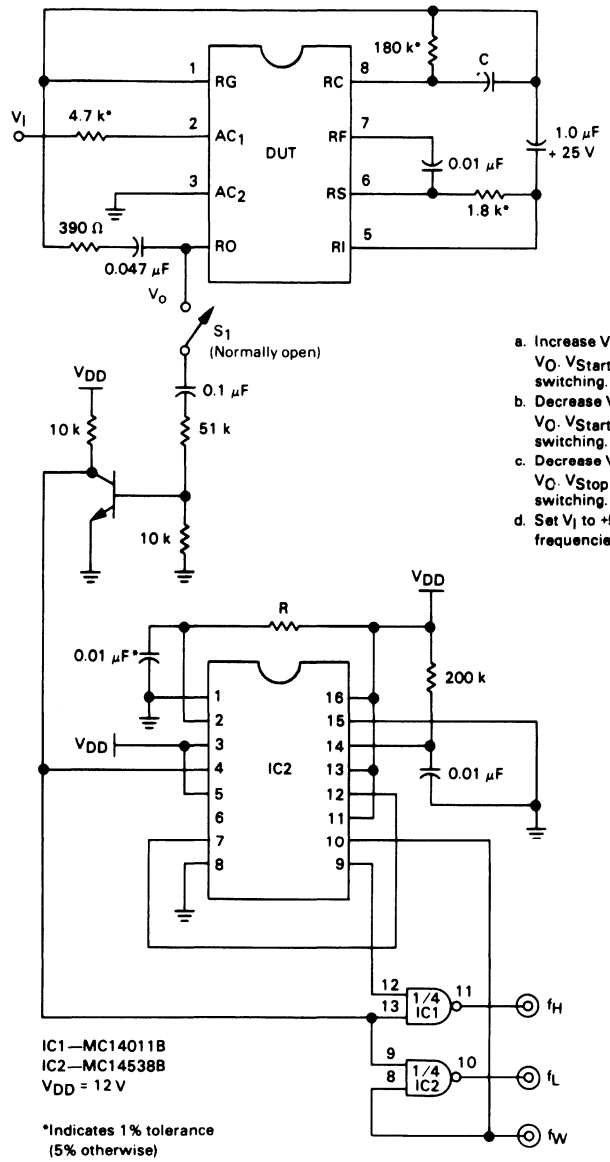
FIGURE 1 — OSCILLATOR PERIOD ($1/f_O$) versus OSCILLATOR R2 C2 PRODUCT



EXTERNAL COMPONENTS

R1	Line input resistor. R1 controls the tone ringer input impedance. It also influences ringing threshold voltage and limits current from line transients. (Range: 2.0 kΩ to 10 kΩ).
C1	Line input capacitor. C1 ac couples the tone ringer to the telephone line and controls ringer input impedance at low frequencies. (Range: 0.4 μF to 2.0 μF).
R2	Oscillator resistor. (Range: 150 kΩ to 300 kΩ).
C2	Oscillator capacitor. (Range: 400 pF to 2000 pF).
R3	Input current sense resistor. R3 controls the ringing threshold voltage. Increasing R3 decreases the ring-start voltage. (Range: 0.8 kΩ to 2.0 kΩ).
C3	Ringing threshold filter capacitor. C3 filters the ac voltage across R3 at the input of the ringing threshold comparator. It also provides dialer transient rejection. (Range: 0.5 μF to 5.0 μF).
C4	Ringer supply capacitor. C4 filters supply voltage for the tone generating circuits. It also provides an ac current path for the 10 V_{rms} ringer signature impedance. (Range: 1.0 μF to 10 μF).

FIGURE 2 — TEST ONE



MC34012-1: C = 1000 pF*
MC34012-2: C = 500 pF*
MC34012-3: C = 1000 pF*

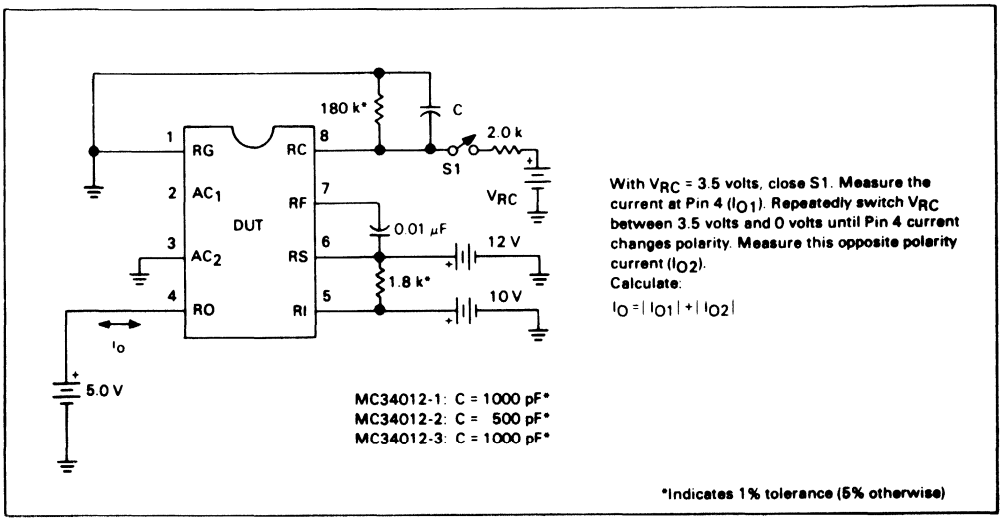
a. Increase V_I from +30 volts while monitoring V_O. $V_{Start(+)}$ equals V_I when V_O commences switching.
b. Decrease V_I from −30 volts while monitoring V_O. $V_{Start(-)}$ equals V_I when V_O commences switching.
c. Decrease V_I from +40 volts while monitoring V_O. V_{Stop} equals V_I when V_O ceases switching.
d. Set V_I to +50 volts. Close S1. Measure frequencies f_H, f_L, and f_W.

IC1—MC14011B
IC2—MC14538B
V_{DD} = 12 V

*Indicates 1% tolerance (5% otherwise)

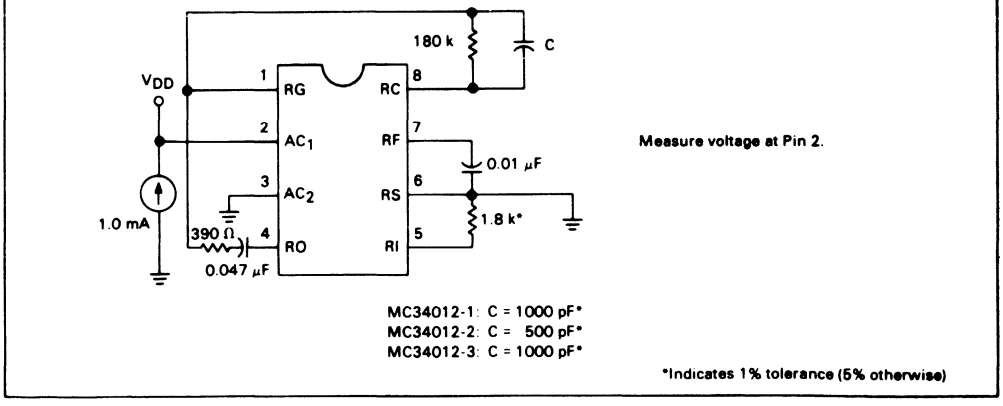
MC34012-1: R = 110 kΩ*
MC34012-2: R = 55 kΩ*
MC34012-3: R = 110 kΩ*

FIGURE 3 — TEST TWO



3

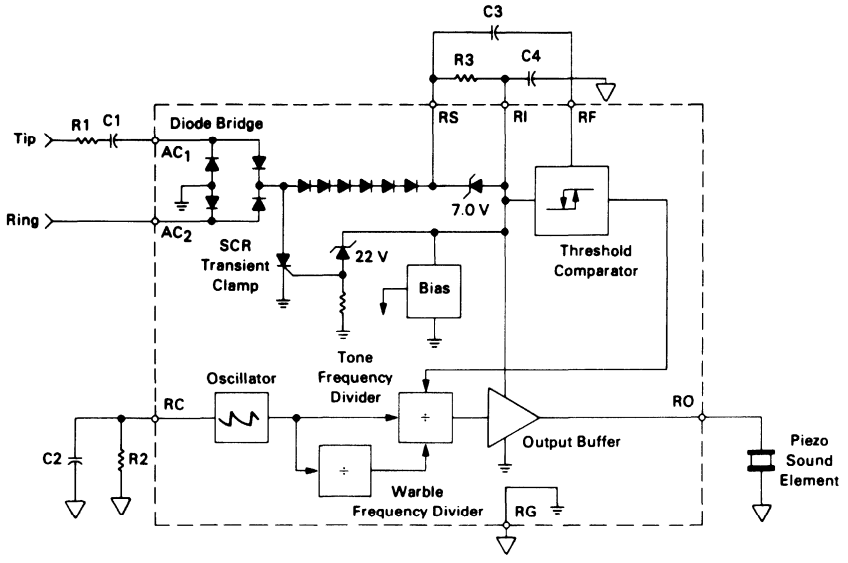
FIGURE 4 — TEST THREE



ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristic	Test	Symbol	Min	Typ	Max	Units
Ringing Start Voltage ($V_{Start} = V_I$ @ Ring Start)						Vdc
$V_I > 0$	1a	$V_{Start(+)}$	31	34.5	38	
$V_I < 0$	1b	$V_{Start(-)}$	-31	-34.5	-38	
Ringing Stop Voltage ($V_{Stop} = V_I$ @ Ring Stop)	1c	V_{Stop}				Vdc
MC34012-1			16	20	25	
MC34012-2			13	18	22	
MC34012-3			16	20	25	
Output Frequencies (V_I = 50 V)	1d					Hz
MC34012-1 High Tone		f_H	967	1040	1113	
Low Tone		f_L	774	832	890	
Warble Tone		f_W	12	13	14	
MC34012-2 High Tone		f_H	1934	2080	2226	
Low Tone		f_L	1548	1664	1780	
Warble Tone		f_W	12	13	14	
MC34012-3 High Tone		f_H	967	1040	1113	
Low Tone		f_L	774	832	890	
Warble Tone		f_W	24	26	28	
Output Voltage (V_I = 50 V)	6	V_O	19	20	23	V_{p-p}
Output Short-Circuit Current	2	I_O	35	50	80	mA_{p-p}
Input Diode Voltage (I_I = 1.0 mA)	3	V_D	4.6	5.1	5.6	Vdc
Input Voltage—SCR Off (I_I = 30 mA)	4a	V_{off}	37	42	47	Vdc
Input Voltage—SCR On (I_I = 100 mA)	4b	V_{on}	3.2	4.2	6.0	Vdc
Threshold Filter Resistance $R_{RF} = 2.0\ V/I_{RF}$	5	R_{RF}	30	50	80	kΩ

BLOCK DIAGRAM



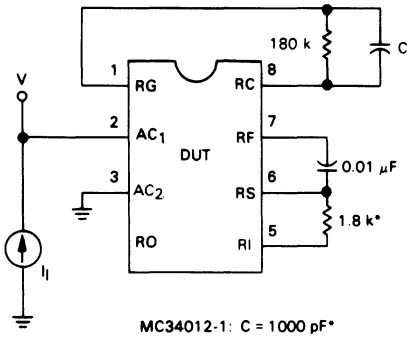
APPLICATION CIRCUIT PERFORMANCE

Characteristic	Typical Value	Units
Output Tone Frequencies MC34012-1 MC34012-2 MC34012-3 Warble Frequency	 832/1040 1664/2080 416/520 13	 Hz
Output Voltage ($V_I \geq 60\ V_{rms}$, 20 Hz)	20	V_{p-p}
Output Duty Cycle	50	%
Ringing Start Input Voltage (20 Hz)	36	V_{rms}
Ringing Stop Input Voltage (20 Hz)	28	V_{rms}
Maximum ac Input Voltage ($\leq$ 68 Hz)	150	V_{rms}
Impedance When Ringing $V_I = 40\ V_{rms}$, 15 Hz $V_I = 130\ V_{rms}$, 23 Hz	 20 10	kΩ
Impedance When Not Ringing $V_I = 10\ V_{rms}$, 24 Hz $V_I = 2.5\ V_{rms}$, 24 Hz $V_I = 10\ V_{rms}$, 5.0 Hz $V_I = 3.0\ V_{rms}$, 200-3200 Hz	 28 >1.0 55 >1.0	 kΩ MΩ kΩ MΩ
Maximum Transient Input Voltage ($T \leq 2.0$ ms)	1500	V

PIN DESCRIPTIONS

Name	Description
AC_1, AC_2	The input terminals to the full-wave diode bridge. The ac ringing signal from the telephone line energizes the ringer through this bridge.
RS	The positive output of diode bridge to which an external current sense resistor is connected.
RI	The positive supply terminal for the oscillator, frequency divider and output buffer circuits.
RF	The terminal for the filter capacitor used in detection of ringing input signals.
RO	The tone ringer output terminal through which the sound element is driven.
RG	The negative output of the diode bridge and the negative supply terminal of the tone generating circuitry.
RC	The oscillator terminal for the external resistor and capacitor which control the tone ringer frequencies.

FIGURE 5 — TEST FOUR

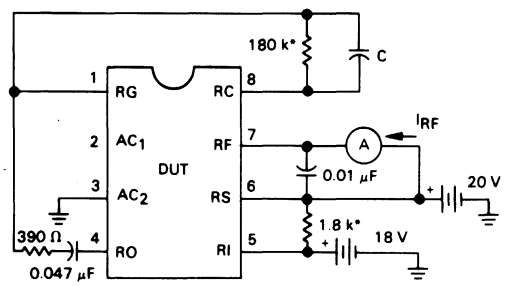


a. Set I_I to 30 mA. Measure voltage at Pin 2 (V_{off}).
b. Set I_I to 100 mA. Measure voltage at Pin 2 (V_{on}).

MC34012-1: C = 1000 pF*
MC34012-2: C = 500 pF*
MC34012-3: C = 1000 pF*

*Indicates 1% tolerance (5% otherwise)

FIGURE 6 — TEST FIVE



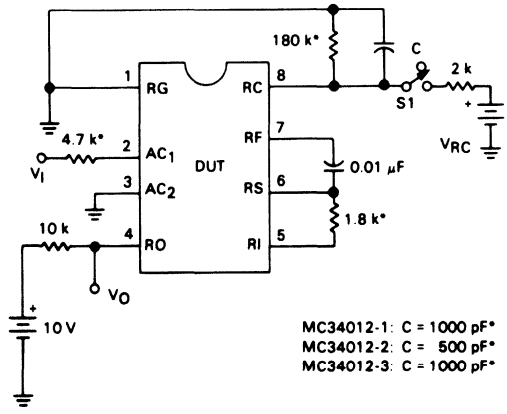
Measure current into Pin 7 (I_{RF}).
Calculate:

R_{RF} = 2 volts ÷ I_{RF}

MC34012-1: C = 1000 pF*
MC34012-2: C = 500 pF*
MC34012-3: C = 1000 pF*

*Indicates 1% tolerance (5% otherwise)

FIGURE 7 — TEST SIX



With V_{RC} = 3.5 volts, close S1. Set V_I to 50 volts. Measure dc voltage at Pin 4 (V_{O1}). Repeatedly change V_{RC} between 3.5 volts and 0 volts until Pin 4 changes state. Measure the new voltage at Pin 4 (V_{O2}). Calculate the peak-to-peak output voltage:

$$V_{Op\text{-}p} = |V_{O2} - V_{O1}|$$

*Indicates 1% tolerance (5% otherwise)

3

MOTOROLA

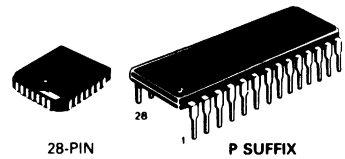
MC34013A

TELEPHONE SPEECH NETWORK AND TONE DIALER

- Linear/I^2L Technology Provides Low 1.4 Volt Operation in Both Speech and Dialing Modes
- Speech Network Provides 2–4 Wire Conversion with Adjustable Sidetone Utilizing an Electret Microphone
- DTMF Generator Uses Low-Cost Ceramic Resonator with Accurate Frequency Synthesis Technique
- On-Chip Regulator Insures Stable Operation Over Wide Range of Loop Lengths
- Dialer Mutes Speech Network with Internal Delay for Click Suppression on DTMF Key Release

SPEECH NETWORK AND TONE DIALER

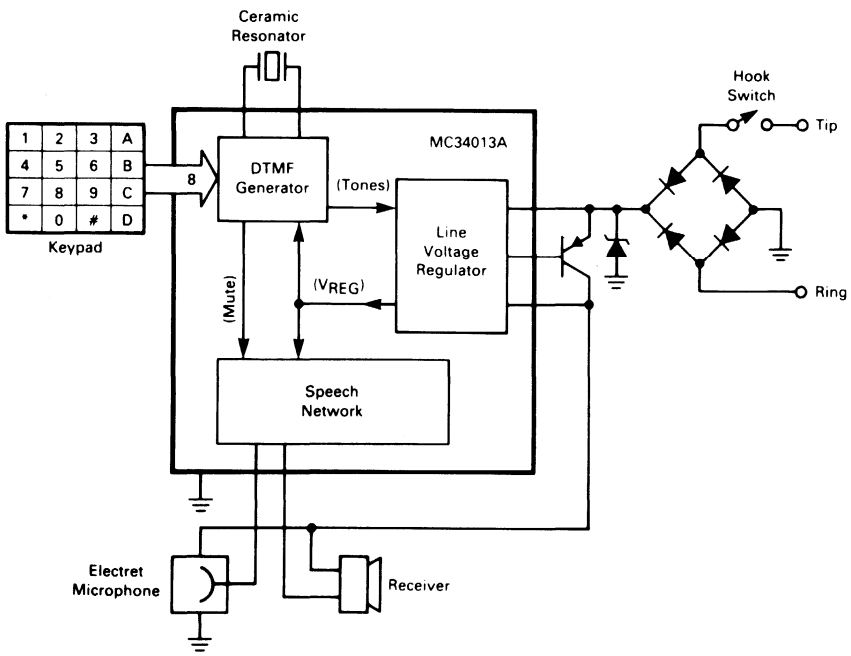
BIPOLAR LINEAR/I^2L



28-PIN
QUAD PACK
CASE 776A-01

P SUFFIX
PLASTIC PACKAGE
CASE 710-02

FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM

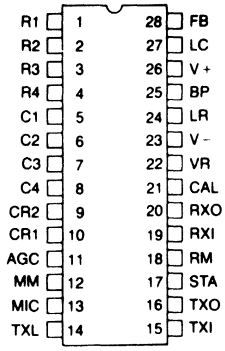


DS9653
(Replacing ADI-792)

MAXIMUM RATINGS (Voltage References to V−)

Parameter	Value	Unit
V+ Terminal Voltage (Pin 26)	+18, −1.0	V
VR Terminal Voltage (Pin 22)	+2.0, −1.0	V
RXO Terminal Voltage (Pin 20)	+2.0, −1.0	V
R1–R4 Terminal Current (Pins 1–4) C1–C4 (Pins 5–8)	±100	mA
Operating Ambient Temperature Range	−20 to +60	°C
Storage Temperature Range	−65 to +150	°C

PIN CONNECTIONS



GENERAL CIRCUIT DESCRIPTION

The MC34013A Electronic Speech Network and Tone Dialer provides a frequency synthesizer for DTMF dialing, analog amplifiers for speech transmission and a dc line interface circuit that terminates the telephone line. When mated with the MC34012 Tone Ringer, a complete tone dialing telephone can be produced with just two ICs.

Low voltage operation is a necessity for telephones in networks where parallel telephone connections are common. An electronic speech network operating in parallel with a conventional telephone may receive line voltages below 2.5 volts. DTMF dialers operate at similarly low-line voltages when signaling through battery powered station carrier equipment. These low voltage requirements have been addressed by realizing the MC34013A in a bipolar/I^2L technology with appropriate circuit techniques. The resulting speech and dialer circuits maintain specified performance with instantaneous input voltage as low as 1.4 volts.

Line Voltage Regulator

The dc line interface circuit (Figure 2) determines the dc input characteristic of the telephone. At low input voltages (less than 3 volts) the IC draws only the speech and dialer bias currents through the VR regulator. As input voltage increases, Q1 conducts the excess dc line current through resistor R12. The 1.5 volt level shift prevents saturation of Q2 with telephone line signals up to 2.0 volts peak (+5.2 dBm). A constant current (dummy load) is switched off when the DTMF dialer is activated to reduce line current transients. Figure 3 illustrates the dc voltage/current characteristic of an MC34013A telephone.

Speech Network

The speech network (Figure 4) provides the two-to-four wire interface between the telephone line and the instrument's transmitter and receiver. An electret microphone biased from VR drives the transmit amplifier. For very loud talkers, the peak limiter circuit reduces the transmit input level to maintain low distortion. The transmit amplifier output signal is inverted at the STA terminal and driven through an external R-C network to control the receiver sidetone level. The switched ac resistance at the RM terminal reduces receiver signal

FIGURE 2 — DC LINE INTERFACE BLOCK DIAGRAM

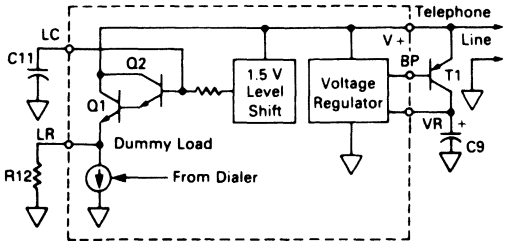
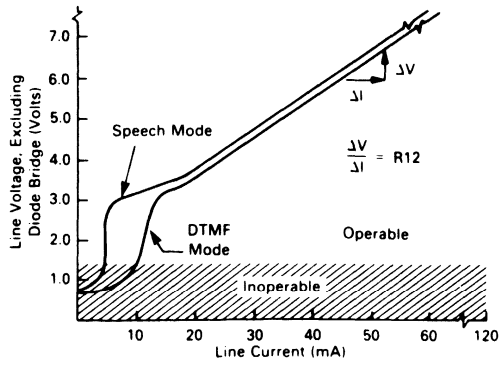
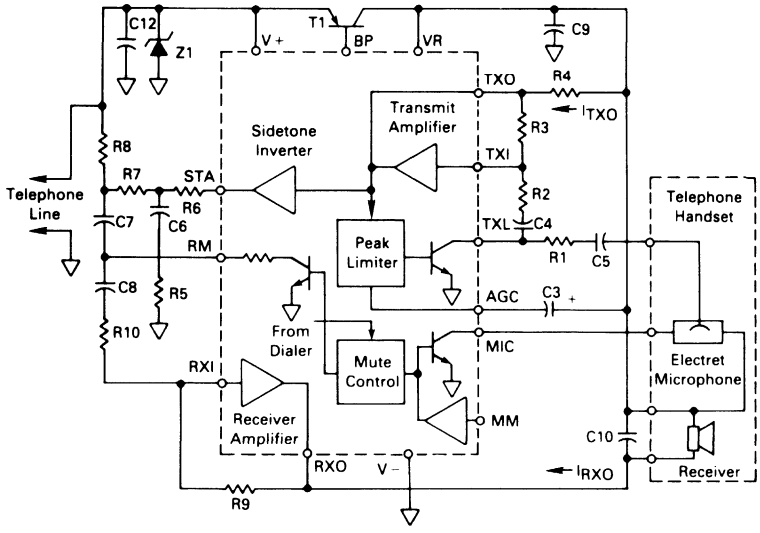


FIGURE 3 — DC V-I CHARACTERISTIC



GENERAL CIRCUIT DESCRIPTION (continued)

FIGURE 4 — SPEECH NETWORK BLOCK DIAGRAM



when dialing and suppresses clicks due to hook or keypad switch transitions. When transmitting, audio signal currents (i_{TXO} and i_{RXO}) flow through the voltage regulator pass transistor (T1) to drive the telephone line. This feature has two consequences: 1) In the transmitting mode the receiver sidetone current i_{RXO} contributes to the total signal on the line along with i_{TXO}; 2) The ac impedance of the telephone is determined by the receiver impedance and the voltage gain from the line to the receiver amplifier output.

DTMF Dialer

Keypad interface comparators activate the DTMF row and column tone generators (Figure 5) when a row and column input are connected through a SPST keypad. The keypad interface is designed to function with contact resistances up to 1.0 kΩ and leakage resistances as low as 150 kΩ. Single tones may be initiated by depressing two keys in the same row or column.

The programmable counters employ a novel design to produce non-integer frequency ratios. The various DTMF tones are synthesized with frequency division errors less than ±0.16% (Table 1). Consequently an inexpensive ceramic resonator can be used instead of a quartz crystal as the DTMF frequency reference. Total frequency error less than ±0.8% can be achieved with ±0.3% ceramic resonator. The row and column D/A converters produce 16-step approximations of sinusoidal waveforms. Feedback through terminal FB reduces the DTMF output impedance to approximately 2.0 kΩ to satisfy return loss specifications. (EIA RS-470)

FIGURE 5 — DTMF DIALER BLOCK DIAGRAM

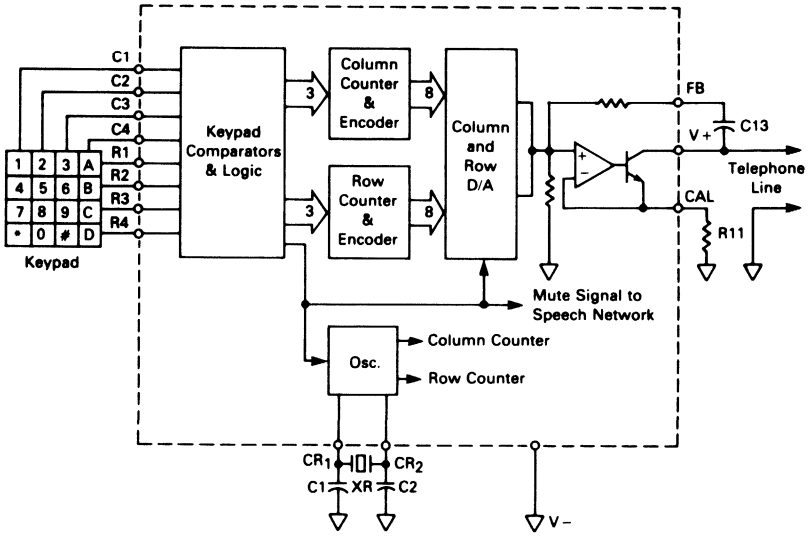


TABLE 1 — FREQUENCY SYNTHESIZER ERRORS

	DTMF Standard (Hz)	Tone Output Frequency with 500 kHz Oscillator	% Deviation from Standard
Row 1	697	696.4	−0.086
Row 2	770	769.2	−0.104
Row 3	852	853.2	+0.141
Row 4	941	939.8	−0.128
Column 1	1209	1207.7	−0.108
Column 2	1336	1336.9	+0.067
Column 3	1477	1479.3	+0.156
Column 4	1633	1634.0	+0.061

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

LINE VOLTAGE REGULATOR

Characteristic	Test Method	Symbol	Min	Typ	Max	Unit
Voltage Regulator Output	1a	V_R	1.0	1.1	1.2	Volts
V+ Current in DTMF Mode	2a	I_{DT}	8.0	12	14.5	mA
Change in I_{DT} with Change in V+ Voltage	2b	ΔI_{DT}	—	0.8	2.0	mA
V+ Current in Speech Mode		I_{SP}				mA
V+ = 1.7 V	1b		3.0	5.0	7.0	
V+ = 5.0 V	1c		8.0	11	15	
Speech to DTMF Mode Current Difference	3	ΔI_{TR}	−2.0	2.0	3.5	mA
LR Level Shift		ΔV_{LR}				Vdc
V+ = 5.0 V, I_{LR} = 10 mA	4a		2.4	2.9	3.5	
V+ = 18 V, I_{LR} = 110 mA	4b		2.6	3.3	4.0	
LC Terminal Resistance	5	R_{LC}	30	50	75	kΩ
Load Regulation	6	ΔV_R	−20	−6.0	20	mVdc

ELECTRICAL CHARACTERISTICS (continued)

KEYPAD INTERFACE CIRCUIT

Characteristic	Test Method	Symbol	Min	Typ	Max	Unit
Row Input Pullup Resistance m^{th} Row Terminal: m = 1,2,3,4	7	R_{Rm}	5.0	8.0	11	kΩ
Column Input Pulldown Resistance n^{th} Column Terminal: n = 1,2,3,4	8	R_{Cn}	5.0	8.0	11	kΩ
Ratio of Row-to-Column Input Resistances $K_{m,n} = \frac{R_{Rm}}{R_{Cn}}$ m = 1,2,3,4 n = 1,2,3,4	7 & 8	$K_{m,n}$	0.88	1.0	1.12	—
Row Terminal Open Circuit Voltage	7a	V_{ROC}	950	1100	1200	mVdc
Row Threshold Voltage for m^{th} Row Terminal: m = 1,2,3,4	9	V_{Rm}	0.70 V_{ROC}	—	—	Vdc
Column Threshold Voltage for n^{th} Column Terminal: n = 1,2,3,4	10	V_{Cn}	—	—	0.30 V_{ROC}	Vdc

DTMF GENERATOR

Row Tone Frequency	Row 1 Row 2 Row 3 Row 4	11a, 11b	f_{Rm}	692.9 765.3 848.9 935.1	696.4 769.2 853.2 939.8	699.9 773.0 857.5 944.5	Hz
Column Tone Frequency	Column 1 Column 2 Column 3 Column 4	11c, 11d	f_{Cn}	1201.6 1330.2 1471.9 1625.2	1207.7 1336.9 1479.3 1633.4	1213.7 1343.6 1486.7 1641.5	Hz
Row Tone Amplitude		11e	V_{Row}	0.38	0.45	0.55	V_{rms}
Column Tone Amplitude		11f	V_{Col}	0.48	0.55	0.67	V_{rms}
Column Tone Pre-emphasis		11g	dB_{CR}	0.5	1.8	3.0	dB
DTMF Distortion		12	% Dis	—	4.0	6.0	%
DTMF Output Resistance		13	R_o	1.0	2.5	3.0	kΩ

SPEECH NETWORK

MIC Terminal Saturation Voltage	14	V_{MIC}	—	60	125	mVdc
MIC Terminal Leakage Current	15a	I_{MIC}	—	0.0	5.0	μA
MM Terminal Input Resistance	15b	R_{MM}	50	100	170	kΩ
TXO Terminal Bias	16a	B_{TXO}	0.48	0.56	0.68	—
TXI Terminal Input Bias Current	16b	I_{TXI}	—	50	400	nA
TXO Terminal Positive Swing	16c	$V_{TXO(+)}$	—	25	60	mVdc
TXO Terminal Negative Swing	16d	$V_{TXO(-)}$	—	130	200	mVdc
Transmit Amplifier Closed-Loop Gain	17a	G_{TX}	16.5	19	20	V/V
Sidetone Amplifier Gain	17b	G_{STA}	0.40	0.45	0.54	V/V
STA Terminal Output Current	18	I_{STA}	50	100	250	μA
RXO Terminal Bias	19a	B_{RXO}	0.48	0.56	0.68	—
RXI Terminal Input Bias Current	19b	I_{RXI}	—	100	400	nA
RXO Terminal Positive Swing	19c	$V_{RXO(+)}$	—	1.0	20	mVdc
RXO Terminal Negative Swing	19d	$V_{RXO(-)}$	—	40	100	mVdc
TXL Terminal OFF Resistance	20a	$R_{TXL(OFF)}$	125	200	300	kΩ
TXL Terminal ON Resistance	20b	$R_{TXL(ON)}$	—	20	100	Ω
RM Terminal OFF Resistance	21a	$R_{RM(OFF)}$	125	180	300	kΩ
RM Terminal ON Resistance	21b	$R_{RM(ON)}$	410	570	770	Ω

PIN DESCRIPTION

(See Figure 28 for external component identifications.)

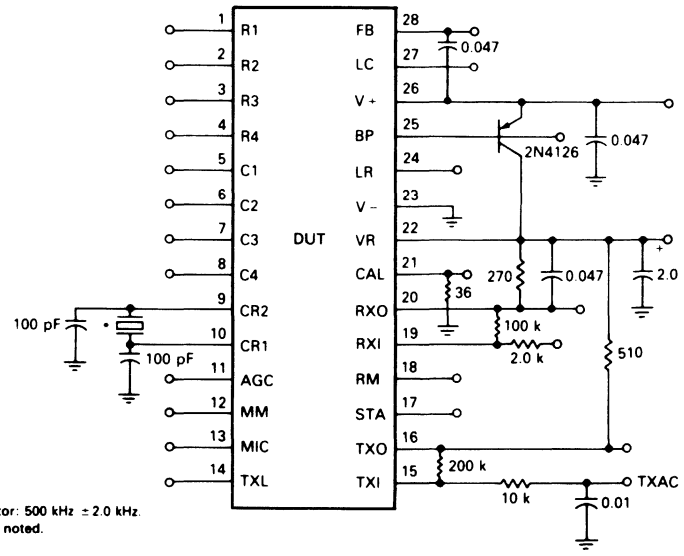
Pin	Designation	Function
1–4	R1–R4	Keypad inputs for Rows 1 through 4. When open, internal 8.0 kΩ resistors pull up the row inputs to a regulated (≈1.1 volt) supply. In normal operation, a row and a column input are connected through a SPST switch by the telephone keypad. Row inputs can also be activated by a Logic "0" (<500 mV) from a microprocessor port.
5–8	C1–C4	Keypad inputs for Columns 1 through 4. When open, internal 8.0 kΩ resistors pull down the column inputs to V–. In normal operation, connecting any column input to any row input produces the respective row and column DTMF tones. In addition to being connected to a row input, column inputs can be activated by a Logic "1" (>500 mV and <3.0 volt).
10,9	CR1, CR2	Ceramic Resonator oscillator input and feedback terminals, respectively. The DTMF dialer is intended to operate with a 500 kHz ceramic resonator from which row and column tones are synthesized.
11	AGC	Automatic Gain Control low-pass filter terminal. Capacitor C3 connected between AGC and VR sets the attack and decay time of the transmit limiter circuit. This capacitor also aids in reducing clicks in the receiver due to hook-switch transients and DTMF on/off transients. In conjunction with internal resistors, C3 (1.0 μF) forms a timer which mutes the receiver amplifier for approximately 20 milliseconds after the user goes off-hook or releases a DTMF Key.
12	MM	Microphone Mute. The MM pin provides a means to mute the microphone and transmit amplifier in response to a digital control signal. When this pin is connected to a Logic "1" (>2.0 V) the microphone dc return path and the transmit amplifier output are disabled.
13	MIC	MICrophone negative supply terminal. The dc current from the electret microphone is returned to V– through the MIC terminal which is connected to the collector of an on-chip NPN transistor. The base of this transistor is controlled either internally by the mute signal from the DTMF generator, or externally by the logic input pin MM.
14	TXL	Transmit Input Limiter. An internal variable resistance element at the TXL terminal controls the transmitter input level to prevent clipping with high signal levels. Coupling capacitors C4 and C5 prevent dc current flow through TXL. The dynamic range of the transmit peak limiter is controlled by resistors R1 and R2.
15	TXI	Transmit Amplifier Input. TXI is the input to the transmit amplifier from an electret microphone. AC coupling capacitors allow the dc offset at TXI to be maintained approximately 0.6 V above V– by feedback through resistor R3 from TXO.
16	TXO	Transmit Amplifier Output. The transmit amplifier output drives ac current through the voltage regulator pass-transistor T1 via resistor R4. The dc bias voltage at TXO is typically 0.6 volts above V–. The transmit amplifier gain is controlled by the R3/(R1 + R2) ratio.
17	STA	SideTone Amplifier output. STA is the output of the sidetone inverter amplifier whose input is driven by the transmit signal at TXO. The inverted transmit signal from STA subtracts from the receiver amplifier input current from V+, thus reducing the receiver sidetone level. Since the transmitted signal at V+ is phase shifted with respect to TXO by the reactive impedance of the phone line, the signal from STA must be similarly phase-shifted in order to provide adequate sidetone reduction. This phase relationship between the transmit signal at TXO and the sidetone cancellation signal from STA is controlled by R5, R6, and C6.
18	RM	Receiver Amplifier Mute. A switched resistance at the RM terminal attenuates the receiver amplifier input signal produced by DTMF dialing tones at V+. RM also mutes clicks at the receiver which result from keypad or hook switch transitions. The ac resistance at RM is typically 540 Ω in the mute mode and 200 kΩ otherwise. Coupling capacitors C7 and C8 prevent dc current flow through RM.
19	RXI	Receiver Amplifier Input. RXI is the input terminal of the receiver amplifier which is driven by ac signals from V+ and STA. Input coupling capacitor C8 allows RXI to be biased approximately 0.6 volts above the V– via feedback resistor R9.
20	RXO	Receiver Amplifier Output. This terminal is connected to the open-collector NPN output transistor of the receiver amplifier. DC bias current for the output device is sourced through the receiver from VR. The bias voltage at RXO is typically 0.6 volts above the V–. Capacitor C10 from RXO to VR provides frequency compensation for the receiver amplifier.

PIN DESCRIPTION (continued)

Pin	Designation	Function
21	CAL	Amplitude CALibration terminal for DTMF dialer. Resistor R11 from the CAL pin to V– controls the DTMF output signal level at Tip and Ring.
22	VR	Voltage Regulator output terminal. VR is the output of a 1.1 volt voltage regulator which supplies power to the speech network amplifiers and DTMF generator during signaling. To improve regulator efficiency at low line current conditions, an external PNP pass-transistor T1 is used in the regulator circuit. Capacitor C9 frequency compensates the VR regulator to prevent oscillation.
23	V–	The dc common (more negative input) connected to Tip and Ring through the polarity guard bridge.
24	LR	DC Load Resistor. Resistor R12 from LR to V– determines the dc input resistance at Tip and Ring. This resistor is external not only to enable programming the dc resistance but also to avoid high on-chip power dissipation with short telephone lines. It acts as a shunt load conducting the excess dc line current. At low line voltages (<3.0 volts), no current flows through LR.
25	BP	Base of a PNP Pass-transistor. Under long-loop conditions where low line voltages would cause VR to fall below 1.1 volts, BP drives the PNP transistor T1 into saturation, thereby minimizing the voltage drop across the pass transistor. At line voltages which maintain VR above 1.1 volts, BP biases T1 in the linear region thereby regulating the VR voltage. Transistor T1 also couples the ac speech signals from the transmit amplifier to Tip and Ring at V+.
26	V+	The more positive input to the regulator, speech, and DTMF sections connected to Tip and Ring through the polarity guard diode bridge.
27	LC	DC Load Capacitor. Capacitor C11 from LC to V– forms a low-pass filter which prevents the resistor at LR from loading ac speech and DTMF signals.
28	FB	FeedBack terminal for DTMF output. Capacitor C13 connected from FB to V+ provides ac feedback to reduce the output impedance to Tip and Ring when tone dialing.

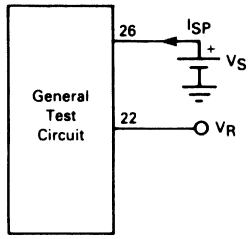
3

FIGURE 6 — GENERAL TEST CIRCUIT



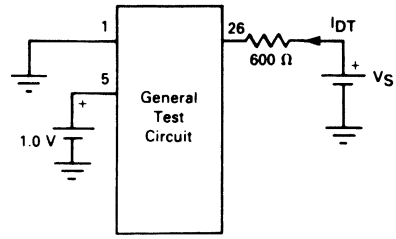
Notes:
1. *Selected ceramic resonator: 500 kHz ± 2.0 kHz.
2. Capacitances in μF unless noted.
3. All resistances in ohms.

FIGURE 7 — TEST ONE



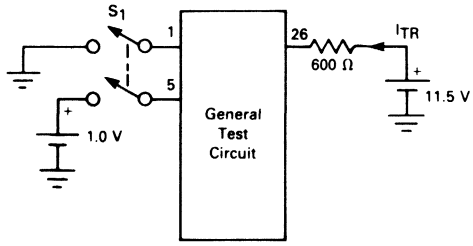
a. Measure V_R with V_S = 1.7 V
b. Measure I_{SP} with V_S = 1.7 V
c. Measure I_{SP} with V_S = 5.0 V

FIGURE 8 — TEST TWO



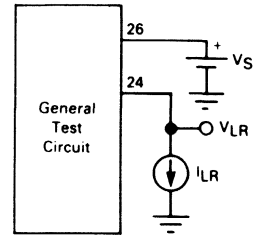
a. Measure I_{DT} with V_S = 11.5 V
b. Measure I_{DT} with V_S = 26 V. Calculate
$\Delta I_{DT} = |I_{DT}|_{26\ V} - |I_{DT}|_{11.5\ V}$

FIGURE 9 — TEST THREE



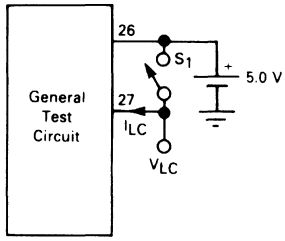
With S_1 open measure I_{TR}. Close S_1 and again measure I_{TR}. Calculate:
$\Delta I_{TR} = |I_{TR}|_{S_1\ Closed} - |I_{TR}|_{S_1\ Open}$

FIGURE 10 — TEST FOUR



a. Set V_S = 5.0 V and I_{LR} = 10 mA. Measure V_{LR}. Calculate $\Delta V_{LR} = V_S - V_{LR}$
b. Repeat Test 4a with V_S = 18 V and I_{LR} = 110 mA

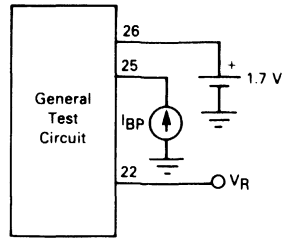
FIGURE 11 — TEST FIVE



With S_1 open measure V_{LC}.
Close S_1 and measure I_{LC}.
Calculate:

$$R_{LC} = \frac{5.0 - V_{LC}}{I_{LC}}$$

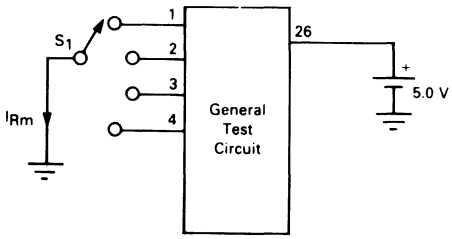
FIGURE 12 — TEST SIX



Set I_{BP} = 0.0 μA and measure V_R.
Set I_{BP} = 150 μA and measure V_R. Calculate:

$$\Delta V_R = |V_R|_{0.0\ \mu A} - |V_R|_{150\ \mu A}$$

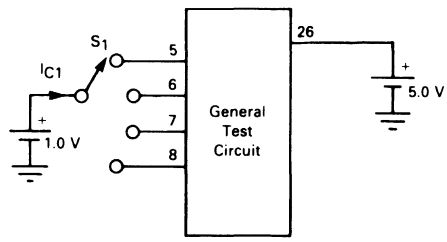
FIGURE 13 — TEST SEVEN



Subscript m corresponds to row number.

a. Set S_1 to Terminal 2 and measure voltage at Terminal 1 (V_{ROC}).
b. Set S_1 to Terminal 1 (m = 1) and measure I_{R1}. Calculate:
$R_{R1} = V_{ROC} \div I_{R1}$
c,d,e. Repeat Test 7b for m = 2,3,4.

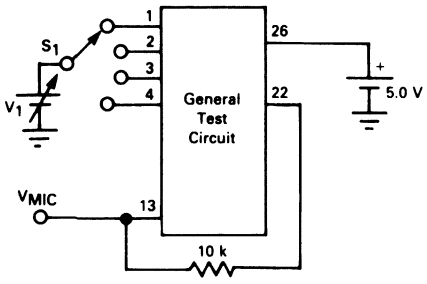
FIGURE 14 — TEST EIGHT



Subscript n corresponds to column number.

a. Set S_1 to Terminal 5 (n = 1) and measure I_{C1}. Calculate:
$R_{C1} = 1.0\ V \div I_{C1}$
b,c,d. Repeat Test 8a for n = 2,3,4.

FIGURE 15 — TEST NINE

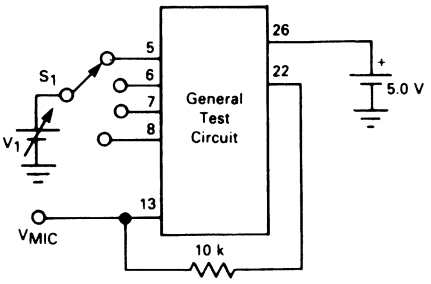


m corresponds to row number.

a. Set S_1 to Terminal 1 (m = 1) with V_1 = 1.0 Vdc. Verify V_{MIC} is Low (V_{MIC} < 0.3 Vdc). Decrease V_1 to 0.70 V_{ROC} and verify V_{MIC} switches high. (V_{MIC} > 0.5 Vdc). V_{ROC} is obtained from Test 7a.

b,c,d. Repeat Test 9a for rows 2,3, and 4. (m = 2,3,4)

FIGURE 16 — TEST TEN

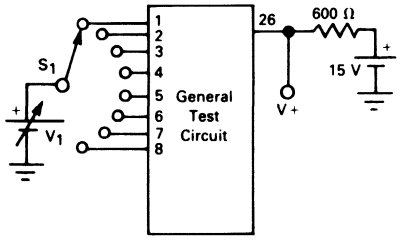


n corresponds to column number.

a. Set S_1 to Terminal 5 (n = 1) with V_1 = 0 Vdc, Verify V_{MIC} is low (V_{MIC} <0.3 Vdc). Increase V_1 to 0.30 V_{ROC} and verify V_{MIC} switches high, (V_{MIC} > 0.5 Vdc). V_{ROC} is obtained from Test 7a.

b,c,d. Repeat Test 10a for columns 2,3, and 4. (n = 2,3,4)

FIGURE 17 — TEST ELEVEN



m corresponds to row number.
n corresponds to column number.

a. With V_1 = 0.0 V set S_1 to Terminal 1 (m = 1) and measure frequency of tone at V+.

b. Repeat Test 11a for rows 2,3 and 4. (m = 2,3,4).

c. With V_1 = 1.0 V set S_1 to Terminal 5. (n = 1) and measure frequency of tone at V+.

d. Repeat Test for columns 2,3, and 4. (n = 2,3,4).

e. Set S_1 to Terminal 4 and V_1 = 0.0 V. Measure row tone amplitude at V+ (V_{ROW}).

f. Set S_1 to Terminal 8 and V_1 = 1.0 V. Measure column tone amplitude at V+. (V_{COL}).

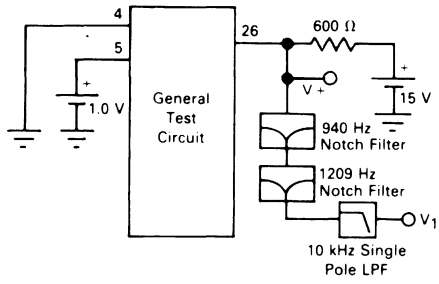
g. Using results of Tests 11e and 11f, calculate:

$$dB_{CR} = 20 \log_{10} \frac{V_{COL}}{V_{ROW}}$$

3

3

FIGURE 18 — TEST TWELVE

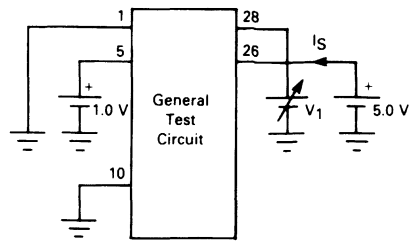


Note: The notch filters must have 50 dB attenuation at their respective center frequencies.

Measure V+ and V_1 with a true rms voltmeter. Calculate:

$$\% \text{ DIS} = \frac{V_1(\text{rms})}{V+(\text{rms})} \times 100$$

FIGURE 19 — TEST THIRTEEN

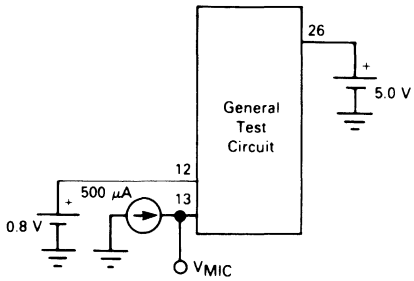


Measure I_S at V_1 = 1.8 V and V_1 = 2.8 V.

Calculate:

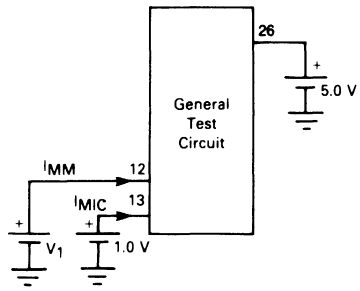
$$R_O = 1.0\text{ V} \div \left[I_S\Big|_{2.8\text{ V}} - I_S\Big|_{1.8\text{ V}} \right]$$

FIGURE 20 — TEST FOURTEEN



Measure V_{MIC}

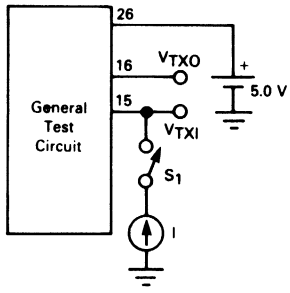
FIGURE 21 — TEST FIFTEEN



a. Set V_1 = 2.0 V and measure I_{MIC}.

b. Set V_1 = 5.0 V and measure I_{MM}.
Calculate: $R_{MM} = 5.0\text{ V} \div I_{MM}$

FIGURE 22 — TEST SIXTEEN



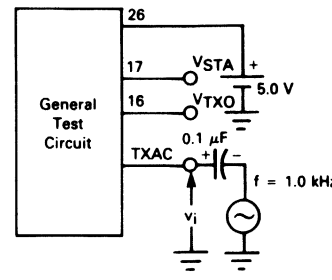
a. With S_1 open, measure V_{TXO}. Using V_R obtained in Test 1 Calculate: $B_{TXO} = V_{TXO} \div V_R$

b. With S_1 open, measure V_{TXO} and V_{TXI}. Calculate: $I_{TXI} = (V_{TXO} - V_{TXI}) \div 200\ k\Omega$

c. Close S_1 and set I = −10 μA. Measure V_{TXO}. Calculate: $V_{TXO}(+) = V_R - V_{TXO}$ where V_R is obtained from Test 1.

d. Close S_1 and set I = +10 μA. Measure V_{TXO}. $V_{TXO}(-) = V_{TXO}$.

FIGURE 23 — TEST SEVENTEEN



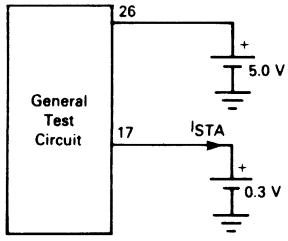
a. Set the generator for v_i = 3.0 mV_{rms}. Measure ac voltage V_{TXO}. Calculate:

$$G_{TX} = \frac{V_{TXO}}{v_i}$$

b. Measure ac voltage V_{STA}. Using V_{TXO} from Test 17a calculate:

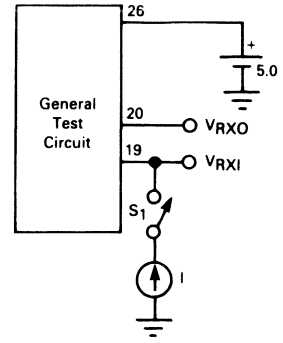
$$G_{STA} = \frac{V_{STA}}{V_{TXO}}$$

FIGURE 24 — TEST EIGHTEEN



Measure I_{STA}.

FIGURE 25 — NINETEEN



a. With S_1 open, measure V_{RXO}. Using V_R obtained in Test 1, calculate: $B_{RXO} = V_{RXO} \div V_R$.

b. With S_1 open, measure V_{RXO} and V_{RXI}. Calculate: $I_{RXI} = (V_{RXO} - V_{RX1}) \div 100\ k\Omega$

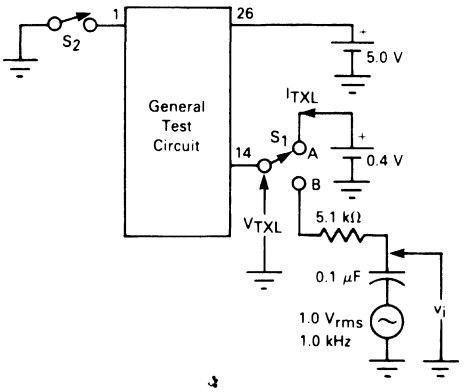
c. Close S_1 and set I = −10 μA. Measure V_{RXO}. Using V_R obtained in Test 1, calculate: $V_{RXO}(+) = V_R - V_{RXO}$.

d. Close S_1 and set I = +10 μA and measure V_{RXO}. $V_{RXO}(-) = V_{RXO}$.

3

3

FIGURE 26 — TEST TWENTY

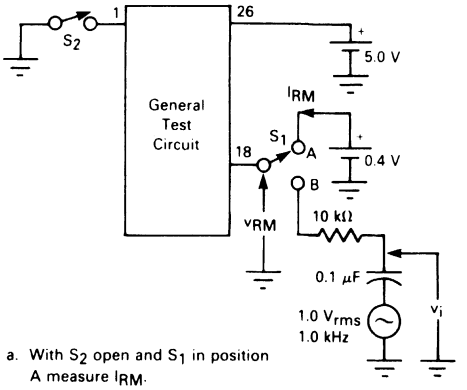


a. Set S_1 to position A with S_2 open. Measure I_{TXL}. Calculate: R_{TXL} (OFF) = 0.4 V ÷ I_{TXL}.

b. Set S_1 to position B and close S_2. Measure ac voltages v_i and V_{TXL}. Calculate:

$$R_{TXL}(ON) = \frac{V_{TXL}}{v_i - V_{TXL}} \times 5.1\ k\Omega$$

FIGURE 27 — TEST TWENTY-ONE



a. With S_2 open and S_1 in position A measure I_{RM}.

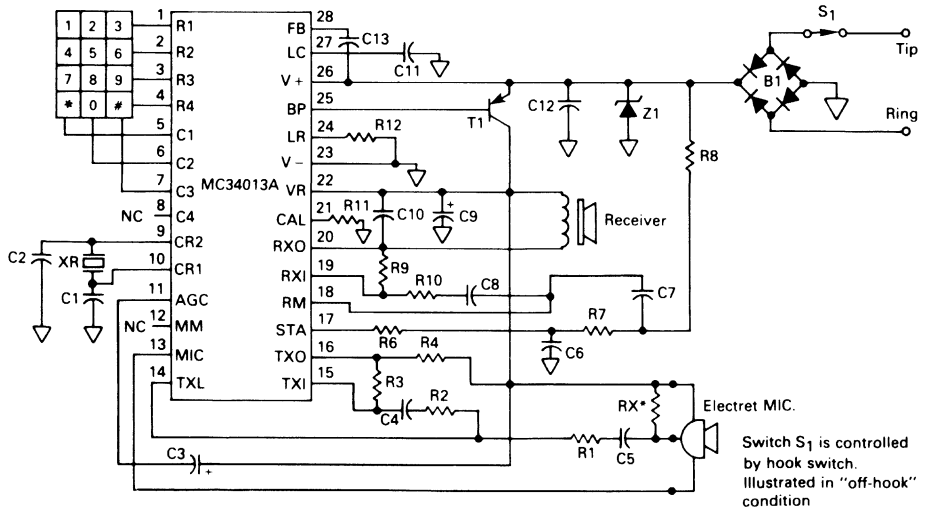
Calculate: $R_{RM}(OFF) = 0.4\ V \div I_{RM}$

b. Close S_2 and switch S_1 to position B. Measure ac voltages v_i and V_{RM}. Calculate:

$$R_{RM}(ON) = \frac{V_{RM}}{v_i - V_{RM}} \times 10\ k\Omega$$

FIGURE 28 — APPLICATION CIRCUIT

DTMF Pad
Row-Column Switch Closure



*RX used with 2-terminal mike only.

APPLICATIONS INFORMATION

Figure 28 specifies a typical application circuit for the MC34013A. Complete listings of external components are provided at the end of this section along with nominal component values. Component values should be varied to optimize telephone performance parameters for each application. The relationships between the application circuit components and certain telephone parameters are briefly described in the following:

Off-Hook DC Resistance

R12 conducts the dc line current in excess of the speech and dialer bias current. Increasing R12 increases the input resistance of the telephone for line currents above 10 mA. R12 should be selected between 30 Ω and 120 Ω.

Off-Hook AC Impedance

The ac input impedance is equal to the receive amplifier load impedance (at RXO) divided by the receive amplifier gain (voltage gain from V+ to RXO). Increasing the impedance of the receiver increases the impedance of the telephone. Increasing the gain of the receiver amplifier decreases the impedance of the telephone.

DTMF Output Amplitude

R11 controls the amplitude of the row and column DTMF tones. Decreasing R11 increases the level of tones generated at V+. The ratio of the row and column tone amplitudes is internally fixed. R11 should be greater than 20 Ω to avoid excessive current in the DTMF output amplifier.

Transmit Output Level

R4 controls the maximum signal amplitude produced at V+ by the transmit amplifier. Decreasing R4 increases the transmit output signal at V+. R4 should be greater than 220 Ω to limit current in the transmit amplifier output.

Transmit Gain

The gain from the microphone to the telephone line varies directly with R3. Increasing R3 increases the signal applied to R4 and the ac current driven through R4 to the telephone line. The closed loop-gain from the microphone to the TXO terminal should be greater than 10 to prevent transmit amplifier oscillations.

Note: Adjustments to transmit level and gain are complicated by the addition of receiver sidetone current to the transmit amplifier output current at V+. Normally the sidetone current from the receiver will increase the transmit signal (if the current in the receiver is in phase with that in R4). Thus the transmit gain and sidetone levels cannot be adjusted independently.

Receiver Gain

Feedback resistor R9 adjusts the gain at the receiver amplifier. Increasing R9 increases the receiver amplifier gain.

Sidetone Level

Sidetone reduction is achieved by the cancellation of receiver amplifier input signals from R8. R6, R7 and C6 determine the phase of the sidetone balance. The ac voltage at the junction of R6 and R7 should be 180° out of phase with the voltage at V+. R7 is selected such that the signal current in R7 is slightly greater than that in R8. This insures that the sidetone current in the receiver adds to the transmit amplifier output current.

EXTERNAL COMPONENTS

(Component Labels Referenced to Figure 28)

Capacitors	Nominal Value	Description
C1, C2	100 pF	Ceramic Resonator oscillator capacitors.
C3	1.0 μF, 3.0 V	Transmit limiter low-pass filter capacitor: controls attack and decay time of transmit peak limiter.
C4, C5	0.1 μF	Transmit amplifier input capacitors: prevent dc current flow into TXL pin and attenuate low-frequency noise on microphone lead.
C6	0.05 μF	Sidetone network capacitor: provides phase-shift in sidetone path to match that caused by telephone line reactance.
C7, C8	0.05 μF	Receiver amplifier input capacitors: prevent dc current flow into RM terminal and attenuates low frequency noise on the telephone line.
C9	2.2 μF, 3.0 V	VR regulator capacitor: frequency compensates the VR regulator to prevent oscillation.
C10	0.01 μF	Receiver amplifier output capacitor: frequency compensates the receiver amplifier to prevent oscillation.
C11	0.1 μF	DC load filter capacitor: prevents the dc load circuit from attenuating ac signals on V+.
C12	0.01 μF	Telephone line bypass capacitor: terminates telephone line for high frequency signals and prevents oscillation in the VR regulator.
C13	0.1 μF	DTMF output feedback capacitor: ac couples feedback around the DTMF output amplifier which reduces output impedance.

Resistors	Nominal Value	Description
R12	82, 1.0 W	DC load resistor: conducts all dc line current in excess of the current required for speech or dialing circuits; controls the off-hook dc resistance of the telephone.
R8, R10	150 k, 56 k	Receiver amplifier input resistors: couple ac input signals from the telephone line to the receiver amplifier; signal in R8 subtracts from that in R7 to reduce sidetone in receiver.
R9	200 k	Receiver amplifier feedback resistor: controls the gain of the receiver amplifier.
R6, R7	1.5 k, 30 k	Sidetone network resistors: drive receiver amplifier input with the inverted output signal from the transmitter; phase of signal in R7 should be opposite that in R8.
R4	270	Transmit amplifier load resistor: converts output voltage of transmit amplifier into a current that drives the telephone line; controls the maximum transmit level.
R3	200 k	Transmit amplifier feedback resistor: controls the gain of the transmit amplifier.
R1, R2	4.7 k, 4.7 k	Transmit amplifier input resistors: couple signal from microphone to transmit amplifier; control the dynamic range of the transmit peak limiter.
R11	36	DTMF calibration resistor: controls the output amplitude of the DTMF dialer.
R_X	3.0 k	Microphone bias resistor: sources current from VR to power a 2-terminal electret microphone; R_X is not used with 3-terminal microphones.

Semiconductors	Electret Mic	Receiver
B1 = MDA106A, or equivalent, or 4-1N4005 T1 = 2N4126 or equivalent Z1 = 18 V, 1.5 W, 1N5931A XR — muRata CSB500 or equivalent	2 Terminal, Primo EM-95 (Use R_X) or equivalent 3 Terminal, Primo 07A181P (Remove R_X) or equivalent	Primo Model DH-34 (300 Ω) or equivalent

MOTOROLA

MC34014

Specifications and Applications Information

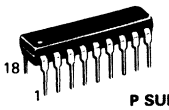
TELEPHONE SPEECH NETWORK WITH DIALER INTERFACE

The MC34014 is a Telephone Speech Network integrated circuit which incorporates adjustable transmit, receive, and sidetone functions, a dc loop interface circuit, tone dialer interface, and a regulated output voltage for a pulse/tone dialer. Also included is an equalization circuit which compensates gains for line length variations. The conversion from 2-to-4 wire is accomplished with a supply voltage as low as 1.5 volts. The MC34014 is packaged in a standard 18-pin (0.3" wide) plastic DIP, and a 20-pin surface mount PLCC package.

- Transmit, Receive, and Sidetone Gains Set by External Resistors
- Loop Length Equalization for Transmit, Receive, and Sidetone Functions
- Operates Down to 1.5 volts (V+) in Speech Mode
- Provides Regulated Voltage for CMOS Dialer
- Speech Amplifiers Muted During Pulse and Tone Dialing
- DTMF Output Level Adjustable with a Single Resistor
- Compatible with 2-Terminal Electret Microphones
- Compatible with Receiver Impedances of 150 Ω and Higher

TELEPHONE SPEECH NETWORK WITH DIALER INTERFACE

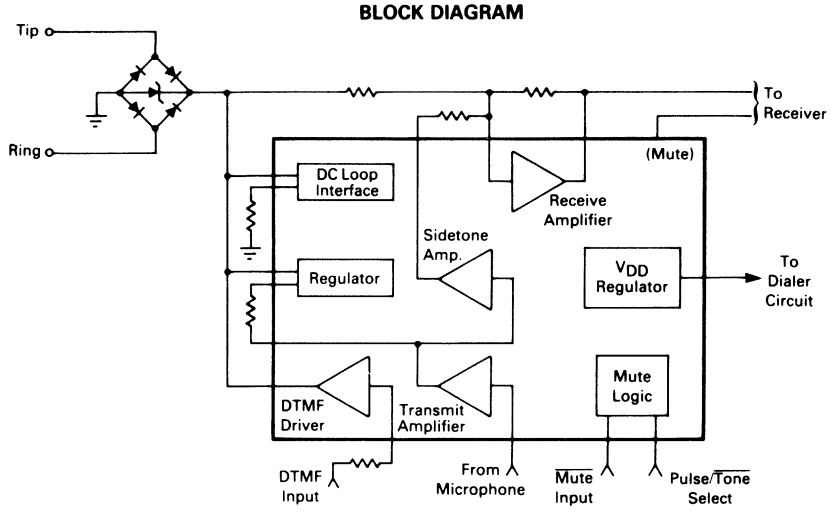
SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 707-02

FN SUFFIX
PLASTIC PACKAGE
CASE 775-01
PLCC-20

BLOCK DIAGRAM



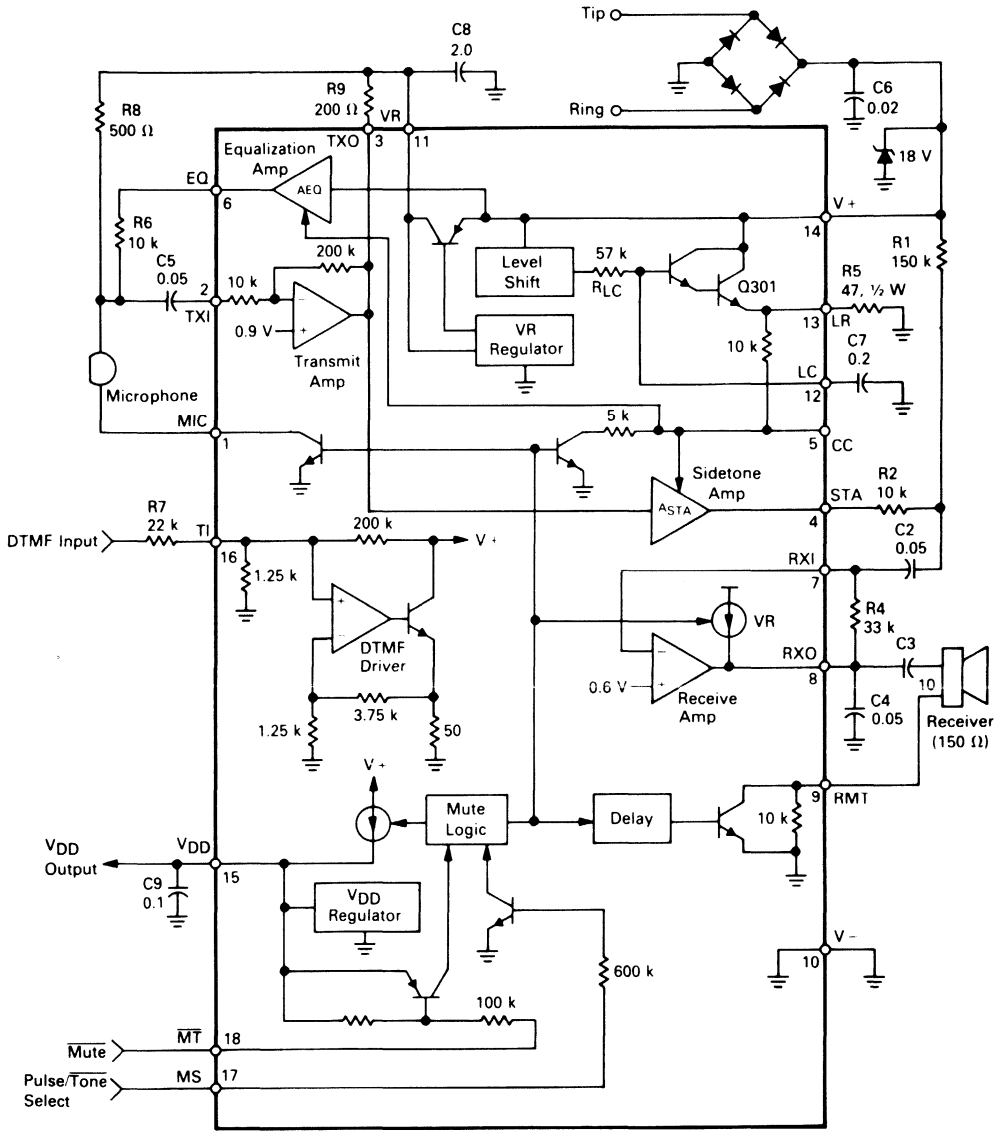
MO-sorb is a trademark of Motorola.

DS9668
(Replacing ADI1148)

PIN DESCRIPTION (See Figure 1)

Pin # PLCC	Pin # DIP	Name	Description
2	1	MIC	Microphone negative supply. Bias current from the electret microphone is returned to V− through this pin, through an open collector NPN transistor whose base is controlled by an internal mute signal. During dialing, the transistor is off, disabling the microphone.
3	2	TXI	Transmit amplifier input. Input impedance is 10 kΩ. Signals from the microphone are input through capacitor C5 to TXI.
4	3	TXO	Transmit amplifier output. The ac signal current from this output flows through the V_R series pass transistor via R9 to drive the line at V+. Increasing R9 will decrease the signal at V+. The output is biased at ≈0.65 V to allow for maximum swing of ac signals. The closed loop gain from TXI to TXO is internally set at 26 dB.
6	4	STA	Sidetone amplifier output. Input to this amplifier is TXO. The signal at STA cancels the sidetone signals in the receive amplifier. The signal level at STA increases with loop length.
7	5	CC	Compensation Capacitor. A capacitor from CC to ground will compensate the loop length equalization circuit when additional stability is required. In most applications, CC remains open.
8	6	EQ	Equalization amplifier output. A portion of the V+ signal is present on this pin to provide negative feedback around the transmit amplifier. The feedback decreases with increasing loop length, causing the ac impedance of the circuit to increase.
9	7	RXI	Receive amplifier input. Input impedance is >100 kΩ. Signals from the line and sidetone amplifier are summed at RXI.
10	8	RXO	Receive Amplifier output. RXO is biased by a 2.5 mA current source. Feedback maintains the dc bias voltage at ≈0.65 V. Increasing R4 (between RXO and RXI) will increase the receive gain. C4 stabilizes the amplifier. C3 couples the signals to the receiver. The 2.5 mA current source is reduced to 0.4 mA when dialing.
11	9	RMT	Receiver Mute. The ac receiver current is returned to V− through an open collector NPN transistor and a parallel 10 kΩ resistor. The base of the NPN is controlled by an internal mute signal. During dialing the transistor is off, leaving the 10 kΩ resistor in series with the receiver.
12	10	V−	Negative supply. The most negative input connected to Tip and Ring through the polarity guard diode bridge.
13	11	VR	Regulated voltage output. The VR voltage is regulated at 1.2 V and biases the microphone and the speech circuits. An internal series pass PNP transistor allows for regulation with a line voltage as low as 1.5 V. Capacitor C8 stabilizes the regulator.
14	12	LC	DC load capacitor. An external capacitor C7 and an internal resistor form a low pass filter between V+ and LR to prevent ac signals from being loaded by the dc load resistor R5. Forcing LC to V− will turn off the dc load current and increase the V+ voltage.
15	13	LR	DC load resistor. Resistor R5 from LR to V− determines the dc resistance of the telephone, and removes power dissipation from the chip. The LR pin is biased 2.8 volts below the V+ voltage (4.5 volts in the tone dialing mode).
16	14	V+	Positive supply. V+ is the positive line voltage (from Tip & Ring) through the polarity guard bridge. All sections of the MC34014 are powered by V+.
18	15	V_{DD}	V_{DD} regulator. V_{DD} is the output of a shunt type regulator with a nominal voltage of 3.3 V. The nominal output current is increased from 550 μA to 2 mA when dialing. Capacitor C9 stabilizes the regulator and sustains the V_{DD} voltage during pulse dialing.
19	16	TI	Tone input. The DTMF signal from a dialer circuit is input at TI through an external resistor R7. The current at TI is amplified to drive the line at V+. Increasing R7 will reduce the DTMF output levels. The input impedance at TI is nominally 1.25 kΩ.
20	17	MS	Mode select. This pin is connected through an internal 600 kΩ resistor to the base of an NPN transistor. A Logic "1" (>2.0 V) selects the pulse dialing mode. A Logic "0" (<0.3 V) selects the tone dialing mode.
1	18	$\overline{MT}$	Mute input. $\overline{MT}$ is connected through an internal 100 kΩ resistor to the base of a PNP transistor, with the emitter at V_{DD}. A Logic "0" (<1.0 V) will mute the network for either pulse or tone dialing. A Logic "1" (>V_{DD} − 0.3 V) puts the MC34014 into the speech mode.

FIGURE 1 — TEST CIRCUIT



NOTE: Pin numbers are for 18 pin DIP.

ABSOLUTE MAXIMUM RATINGS (Voltages referred to V−, T_A = 25°C) (See Note 1.)

Parameter	Value	Units
V+ Voltage	−1.0, +18	Vdc
V_{DD} (externally applied, V+ = 0)	−1.0, +6	Vdc
V_{LR}	−1.0, V+ − 3.0	Vdc
$\overline{MT}$, MS Inputs	−1.0, V_{DD} +1.0	Vdc
Storage Temperature	−65, +150	°C

NOTE 1: Devices should not be operated at these values. The "Recommended Operating Conditions" provide conditions for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Parameter	Value	Units
V+ Voltage (Speech Mode) (Tone Dialing Mode)	+1.5 to +15 +3.3 to +15	Vdc Vdc
I_{TXO} (Instantaneous)	0 to 10	mA
Ambient Temperature	−20 to +60	°C

ELECTRICAL CHARACTERISTICS (Refer to Figure 1) (T_A = 25°C)

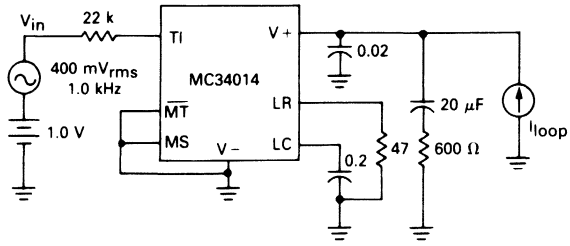
Parameter	Symbol	Min	Typ	Max	Units
LINE INTERFACE					
V+ Voltage	V+				Vdc
I_{loop} = 20 mA (Speech/Pulse Mode)		2.6	3.2	3.8	
I_{loop} = 30 mA (Speech/Pulse Mode)		3.0	3.7	4.4	
I_{loop} = 120 mA (Speech/Pulse Mode)		7.0	8.2	9.5	
I_{loop} = 20 mA (Tone Mode)		4.1	4.9	5.7	
I_{loop} = 30 mA (Tone Mode)		4.6	5.4	6.2	
V+ Current (Pin 12 Grounded)	I+				mA
V+ = 1.7 V (Speech Mode)		4.0	6.6	8.5	
V+ = 12 V (Speech/Pulse Modes)		5.5	8.4	12.5	
V+ = 12 V (Tone Mode)		6.0	8.8	14.0	
LR Level Shift (V+ − V_{LR})	ΔV_{LR}				Vdc
(Speech/Pulse Mode)		—	2.7	—	
(Tone Mode)		—	4.3	—	
LC Terminal Resistance	R_{LC}	36	57	94	kΩ
VOLTAGE REGULATORS					
VR Voltage (V+ = 1.7 V)	V_R	1.1	1.2	1.3	Vdc
Load Regulation (0 mA < I_R < 6.0 mA)	ΔV_{RLD}	—	20	—	mV
Line Regulation (2.0 V < V+ < 6.5 V)	ΔV_{RLN}	—	25	—	mV
V_{DD} Voltage (V+ = 4.5 V)	V_{DD}	3.0	3.3	3.8	Vdc
Load Regulation (0 < I_{DD} < 1.6 mA) (Dialing Mode)	ΔV_{DDLD}	—	0.25	—	Vdc
Line Regulation (All Modes) (4.0 V < V+ < 9.0 V)	ΔV_{DDLN}	—	50	—	mV
Max. Output Current (Speech Mode)	I_{DDSP}	375	550	1000	μA
Max. Output Current (Dialing Mode)	I_{DDDL}	1.6	2.0	3.6	mA
V_{DD} Leakage Current (V+ = 0, V_{DD} = 3.0 V)	I_{DDLK}	—	—	1.5	μA
SPEECH AMPLIFIERS					
Transmit Amplifier					
Gain (TXI to TXO)	A_{TXO}	—	20	—	V/V
TXO Bias Voltage (Speech/Pulse Mode)	V_{TXOSP}	0.45	0.52	0.60	x V_R
TXO Bias Voltage (Tone Mode Mode)	V_{TXODL}	VR − 25	VR − 5.0	—	mV
TXO High Voltage (Speech/Pulse Mode)	V_{TXOH}	VR − 25	VR − 5.0	—	mV
TXO Low Voltage (Speech/Pulse Mode)	V_{TXOL}	—	125	250	mV
TXI Input Resistance	R_{TXI}	—	10	—	kΩ
Receive Amplifier					
RXO Bias Voltage (All Modes)	V_{RXO}	0.45	0.52	0.60	x VR
RXO Source Current (Speech Mode)	I_{RXOSP}	1.5	2.0	—	mA
RXO Source Current (Pulse/Tone Mode)	I_{RXODL}	200	400	—	μA
RXO High Voltage (All Modes)	V_{RXOH}	VR − 100	VR − 50	—	mV
RXO Low Voltage (All Modes)	V_{RXOL}	—	50	150	mV

ELECTRICAL CHARACTERISTICS — (continued) (T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Units
MICROPHONE, RECEIVER CONTROLS					
MIC Saturation Voltage (Speech Mode, I = 500 μA)	$V_{OL_{MIC}}$	—	50	125	mV
MIC Leakage Current (Dialing Mode, Pin 1 = 3.0 V)	$I_{MIC_{LK}}$	—	0	5.0	μA
RMT Resistance (Speech Mode) (Dialing Mode)	$R_{RMT_{SP}}$ $R_{RMT_{DL}}$	— 5.0	8.0 10	15 18	Ω kΩ
RMT Delay (Dialing to Speech)	t_{RMT}	2.0	4.0	20	ms
DIALING INTERFACE					
$\overline{MT}$ Input Resistance	R_{MT}	58	100	—	kΩ
$\overline{MT}$ Input High Voltage	V_{IHMT}	V_{DD} - 0.3	—	—	Vdc
$\overline{MT}$ Input Low Voltage	V_{ILMT}	—	—	1.0	Vdc
MS Input Resistance	R_{MS}	280	600	—	kΩ
MS Input High Voltage	V_{IHMS}	2.0	—	—	Vdc
MS Input Low Voltage	V_{ILMS}	—	—	0.3	Vdc
TI Input Resistance	R_{TI}	—	1.25	—	kΩ
DTMF Gain (See Figure 2) ($V+/V_{in}$)	A_{DTMF}	3.2	4.8	6.2	dB
SIDETONE AMPLIFIER					
Gain (TXO to STA)	A_{STA}				dB
(Speech Mode) @ V_{LR} = 0.5 V		—	- 15	—	
(Speech Mode) @ V_{LR} = 2.5 V		—	- 21	—	
(Pulse Mode) @ V_{LR} = 0.2 V		—	- 15	—	
(Pulse Mode) @ V_{LR} = 1.0 V		—	- 21	—	
STA Bias Voltage (All Modes)	V_{STA}	0.65	0.8	0.9	x V_R
EQUALIZATION AMPLIFIER					
Gain (V+ to EQ)	A_{EQ}				dB
(Speech Mode) @ V_{LR} = 0.5 V		—	- 12	—	
(Speech Mode) @ V_{LR} = 2.5 V		—	- 2.5	—	
(Pulse Mode) @ V_{LR} = 0.2 V		—	- 12	—	
(Pulse Mode) @ V_{LR} = 1.0 V		—	- 2.5	—	
EQ Bias Voltage	V_{EQ}				Vdc
(Speech Mode) @ V_{LR} = 0.5 V		—	0.66	—	
(Pulse Mode) @ V_{LR} = 0.5 V		—	1.3	—	
(Speech, Pulse) @ V_{LR} = 2.5 V		—	3.3	—	

NOTE: Typical values are not tested or guaranteed.

FIGURE 2 — DTMF DRIVER TEST



SYSTEM SPECIFICATIONS (T_A = 25°C) (See Figures 1–4)

Parameter		Min	Typ	Max	Unit
Tip-Ring Voltage (including polarity guard bridge drop of 1.4 V)					Vdc
(Speech Mode)	I_{loop} = 5.0 mA	—	2.4	—	
	I_{loop} = 10 mA	—	3.9	—	
	I_{loop} = 20 mA	—	4.6	—	
	I_{loop} = 40 mA	—	5.6	—	
	I_{loop} = 60 mA	—	6.6	—	
Transmit					
Gain from V_S to V+ (Figure 3) (I_{loop} = 20 mA)		28	30	31	dB
Gain change as I_{loop} is increased to 60 mA		−6.0	−4.5	−3.6	dB
Distortion		—	2.0	—	%
Output noise		—	11	—	dBrnc
Receive					
V_{RXO}/V_S (f = 1.0 kHz, I_{loop} = 20 mA) (See Figure 4)		−16	−15	−13	dB
Receive gain change as I_{loop} is increased to 60 mA		−5.0	−3.0	−2.0	dB
Distortion		—	2.0	—	%
Sidetone Level					dB
$V_{RXO}/V+$ (Figure 3)					
	I_{loop} = 20 mA	—	−36	—	
	I_{loop} = 60 mA	—	−21	—	
Sidetone Cancellation		20	26	—	dB
$\left[\frac{V_{RXO}}{V+}\text{ (Figure 4)}\right]$ dB − $\left[\frac{V_{RXO}}{V+}\text{ (Figure 3)}\right]$ dB	I_{loop} = 20 mA				
DTMF Driver		3.2	4.8	6.2	dB
$V+/V_{in}$ (Figure 2)	I_{loop} = 20 mA				
AC Impedance					Ω
Speech mode (incl. C_6, See Figure 4)	I_{loop} = 20 mA	—	750	—	
Z_{ac} = (600)V+/(V_S − V+)	I_{loop} = 60 mA	—	300	—	
Tone mode (including C_6)	20 mA < I_{loop} < 60 mA	—	1650	—	

NOTE: Typicals are not tested or guaranteed.

FIGURE 3 — TRANSMIT AND SIDETONE LEVEL TEST

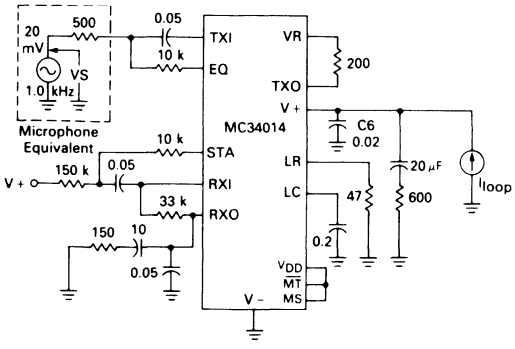
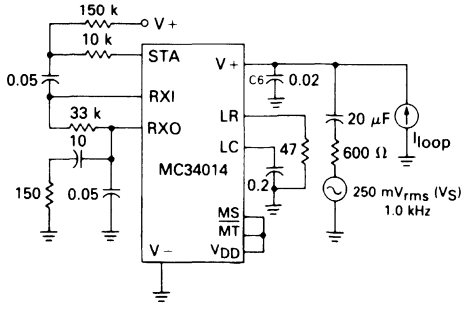


FIGURE 4 — AC IMPEDANCE, RECEIVE AND SIDETONE CANCELLATION TEST



DESIGN GUIDELINES (Refer to Figure 1)

INTRODUCTION

The MC34014 is a speech network meant for connection to the Tip & Ring lines through a polarity guard bridge. The circuit incorporates four amplifiers: transmit, receive, sidetone, and equalization. Some parameters of each amplifier are set by external components, and in addition, the gains of the sidetone and equalization amplifiers vary with loop current.

The line interface portion determines the dc voltage versus loop current characteristics, and provides the required regulated voltages for internal and external use.

The dialer interface provides three modes of operation: speech (non-dialing), pulse dialing, and tone (DTMF) dialing. When switching to either dialing mode some parameters of the various sections are changed in order to optimize the circuit operation for that mode. The following table summarizes those changes:

TABLE 1 — OPERATING PARAMETERS AS A FUNCTION OF OPERATING MODE

Function	Speech	Pulse	Tone
LR Level Shift (V+ − V_{LR})	2.7 V	2.7 V	4.3 V
V_{DD} Source Current	550 μA	2.0 mA	2.0 mA
Transmit Amplifier	Functional	Functional	Inoperative
MIC Switch (Pin 1)	On	Off	Off
Equalization Amplifier	See Transfer Curves — Figure 8		
Sidetone Amplifier	See Transfer Curves — Figure 6		
Receive Amplifier Output Current	2.5 mA	400 μA	400 μA
RMT (Pin 9) Impedance	8.0 Ω	10 kΩ	10 kΩ
DTMF Amplifier	Inoperative	Inoperative	Functional
CC Voltage	$V_{LR}/3$	V_{LR}	V_{LR}

DC LINE INTERFACE (Figure 5)

The dc line interface circuit (Pins 10, 12–14) sets the dc voltage characteristics with respect to the loop current. The loop current enters at Pin 14 where the internal circuitry of the MC34014 draws 5–6 mA. Pin 3 sinks (typically) 3 mA through R_9. The remainder of the loop current is passed through Q_{301} and R_5. The resulting voltage across the entire circuit is therefore equal to the voltage across R_5, plus the level shift voltage from Pin 13 (LR) to Pin 14 (V+), nominally 2.7 volts in the speech and pulse modes. In the tone mode, the level shift increases to 4.3 volts, the internal current changes slightly (Figure 6), and the current required at Pin 3 decreases to near zero. These changes increase the equivalent dc resistance of the circuit, raising the voltage at V+ to ensure adequate voltage at V_{DD} for the external tone dialer. See Figure 7 for typical voltage versus loop current characteristics.

Capacitor C_7 at Pin 12 provides high frequency rolloff (above 10 Hz) so that R_5 does not load down the speech and DTMF signals.

The voltage at V_R is an internally regulated 1.2 volt supply which provides the bias currents for the microphone and the transmit amplifier output (Pin 3), as well as internal bias for the various amplifiers. Capacitor C_8 stabilizes the regulator. The use of an (internal) PNP transistor allows V_R to be regulated with a V+ voltage as low as 1.5 volts.

FIGURE 5 — DC LINE INTERFACE

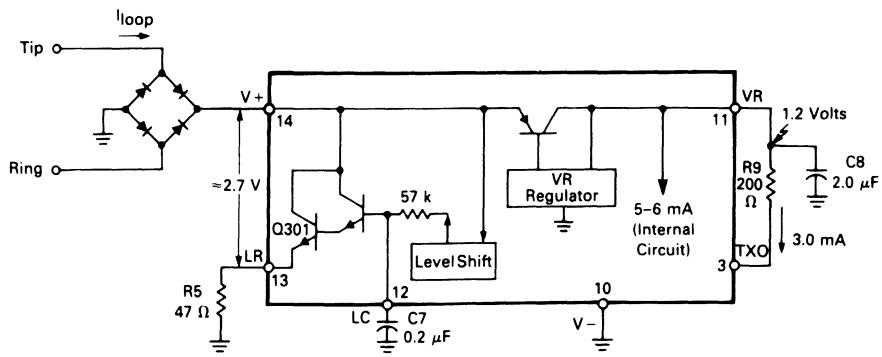


FIGURE 6 — INTERNAL CURRENT versus VOLTAGE

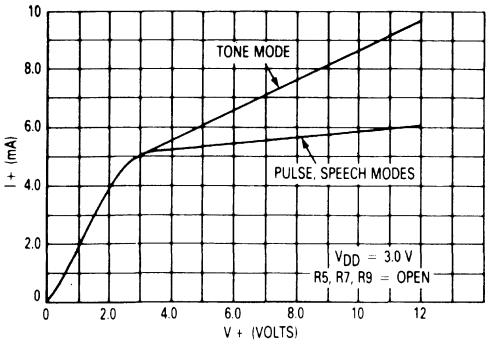
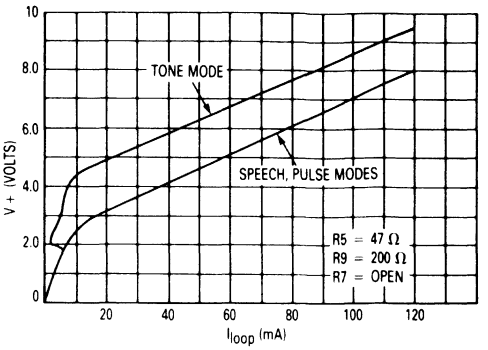


FIGURE 7 — CIRCUIT VOLTAGE versus LOOP CURRENT



3

TRANSMIT AMPLIFIER

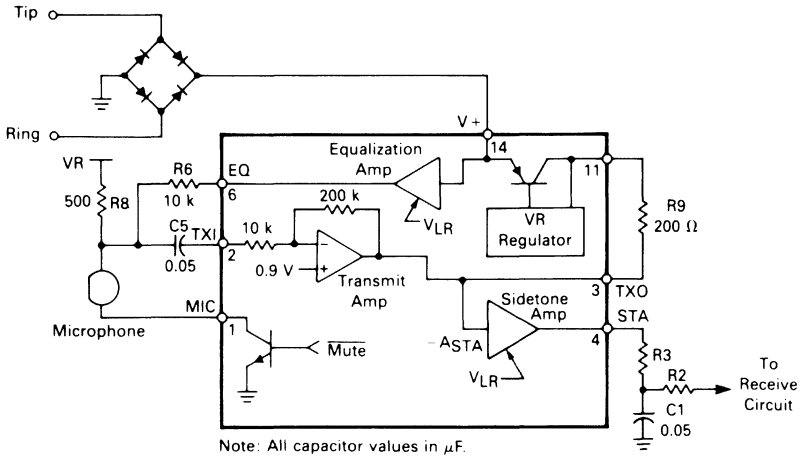
The transmit amplifier (from TXI to TXO) is inverting, with a fixed internal gain of 20 V/V (26 dB), and a typical input impedance of 10 kΩ (Figure 8). The input bias currents are internally supplied, allowing capacitive coupling of the microphone signals to the amplifier.

In the speech and pulse modes, the dc bias level at TXO is typically 0.52 x VR (≈0.63 V), which permits the output to swing 0.55 volts in both positive and negative directions without clipping. The ac voltage signal at TXO (the amplified speech signal) is converted to an ac current by R_9. The ac current passes through the VR series pass transistor to V+, modulating the loop current. The voltage signal at V+ is out of phase with the signal at TXI.

In the tone dialing mode, the TXO dc bias level is clamped at approximately VR-10 mV, rendering the amplifier inoperative. This action also reduces the TXO bias current from 3.0 mA to less than 125 μA.

MIC (Pin 1) is connected to an open-collector NPN transistor, and provides the ground path for the microphone bias current. In either dialing mode, the transistor is off, disabling the microphone.

FIGURE 8 — TRANSMIT SECTION



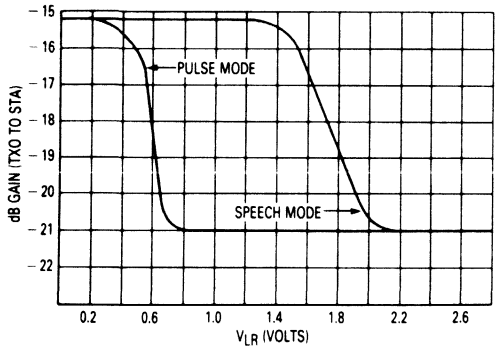
Note: All capacitor values in μF.

SIDETONE AMPLIFIER

The sidetone amplifier provides inversion of the TXO signal for the reduction of the sidetone signal at the receive amplifier (Figure 8). Resistors R_2 and R_3 determine the amount of sidetone cancellation. Capacitor C_1 provides phase shift to compensate for the phase shift created by the complex impedance of the Tip & Ring lines.

The gain of the sidetone amplifier varies with the voltage at LR (Pin 13), in effect making it a function of the loop current. The maximum gain is −15 dB (0.17 V/V) at low loop currents, and the minimum gain is −21 dB (0.09 V/V) at high loop current (see Figure 9 for transfer curves). For example, using 47 Ω for R_5, the gain would begin to decrease at ≈30 mA, and would stop decreasing at ≈57 mA (speech mode). The dc bias voltage at STA (Pin 4) changes slightly (≈50 mV) with variations in loop current. The output is inverted from TXO, which is the input to this amplifier. Since the transmit amplifier is inoperative in the tone dialing mode, the sidetone amplifier is also inoperative in that mode.

FIGURE 9 — SIDETONE AMPLIFIER GAIN



RECEIVE AMPLIFIER

The gain of the receive amplifier (from V+ to RXO) is determined according to the following equation (refer to Figure 10):

$$\frac{V_{RXO}}{V+} = \frac{R_4}{R_1} + \frac{(X_C/\!/R_2)\,(A_{EQ})\,(A_{TXO})\,(A_{STA}) \times R_A \times R_4}{((X_C/\!/R_2)+R_3)\,(R_A+R_6) \times R_2}$$

Where $R_A = R_8/\!/10\ k\Omega$ (10 kΩ = R_{in} of T_x Amp)
A_{EQ} = Gain of Equalization Amp
A_{TXO} = Gain of Transmit Amp (20 V/V)
A_{STA} = Gain of sidetone Amp
X_C = Impedance of C_1 at frequency of interest

The waveform at STA (Pin 4) is in phase with that at V+ (for receive signals), hence the plus sign between the terms. Due to the variations of A_{EQ} and A_{STA} with loop current, the receive gain will vary by ≈1.5 dB. If capacitor C_1 is not used, the above equation is simplified by deleting the terms containing X_C.

The output at RXO is inverted from V+ in the receive mode. In the transmit mode, the V+-to-RXO phase relationship depends on the amount of sidetone cancellation (determined by R_2 and R_3 and C_1), and can vary from 0° to 180°.

In the speech mode, the output current capability (at RXO) is typically 2.0 mA. In either dialing mode, the current capability is reduced to 400 μA in order to reduce internal current consumption. This feature is beneficial when this device is used in conjunction with a line-powered speakerphone circuit, such as the MC34018, where the majority of the loop current is needed for the speakerphone.

RMT (Pin 9) is the return path for the receiver's ac current. This pin is internally connected to an open collector NPN transistor, paralleled by a 10 kΩ resistor. In the speech mode, the transistor is on, providing a low impedance from RMT to ground. In either dialing mode, the transistor is off, muting the receive signal. This prevents loud "clicks" or loud DTMF tones from being heard in the receiver during dialing. When switching from either dialing mode to the speech mode ($\overline{MT}$ switches from low to high), the RMT pin switches back to a low impedance after a delay of 2–20 ms. The delay reduces clicks in the receiver associated with switching from the dialing to speech mode.

EQUILIZATION AMPLIFIER

The equalization amplifier gain varies with loop current, and is configured in the circuit so as to cause a variation of the network ac impedance (when looking in from the Tip & Ring lines). The gain varies with the voltage at LR (Pin 13), in effect making it a function of the loop current. The maximum gain is −2.5 dB (0.75 V/V) at high loop current, and the minimum gain is −12 dB (0.25 V/V) and low loop current (see Figure 11 for transfer curve). For example, using 47 Ω for R_5, the gain would begin to increase at ≈30 mA, and would stop increasing at ≈57 mA (speech mode). The output signal is in phase with the signal at V+, which is the input to this amplifier.

The dc bias level at EQ (Pin 6) varies with the voltage at LR (Pin 13) according to the curve of Figure 12. In most applications, this level shift is of little consequence, and may be ignored. If a particular circuit configuration should be sensitive to the shift, however, the output signal at EQ may be ac coupled to the rest of the circuit.

The equalization amplifier remains functional in all three modes, although in the tone mode, its function has no consequence when the circuit is configured as shown in Figure 1.

V_{DD} REGULATOR

The V_{DD} regulator is a shunt type regulator which supplies a nominal 3.3 volts for external dialers, and/or

other circuitry. In the speech mode, the output current capability at Pin 15 is typically 550 μA. In either dialing mode, the current capacity is increased to 2.0 mA.

V_{DD} will be regulated whenever V+ is >300 mV above the regulated value. As V+ is lowered, and the internal pass transistor becomes saturated, the circuit steers current away from the external load through an internal current source, in order that the V_{DD} capacitor (C9) does not load down speech and DTMF signals at V+. As V+ is lowered below 1 volt, Pin 15 switches to a high impedance state to prevent discharging of any storage capacitors, or batteries used for memory retention.

The V_{DD} voltage is unaffected by the choice of operating mode.

3

DIALER INTERFACE

The dialer interface consists of the mode control pins, $\overline{MT}$ and MS (Pins 18 and 17), and the DTMF current amplifier.

The $\overline{MT}$ pin, when at a Logic "1" (> V_{DD} – 0.3 V), sets the circuit into the speech mode, independent of the state of the MS pin. When the $\overline{MT}$ pin is at a Logic "0" (< 1.0 V), the dialing mode is determined by the MS pin. When MS is at a Logic "1" (> 2.0 V), the circuit is in the pulse dialing mode, and when at a Logic "0" (< 0.3 V) the tone (DTMF) mode is in effect.

The input impedance of the $\overline{MT}$ pin is typically 100 kΩ, with the input current flowing out of the pin (from V_{DD}). The input impedance of the MS pin is typically 600 kΩ, and the input current flows into the pin (Figure 1).

The DTMF amplifier (Figure 13) is a current amplifier which transmits DTMF signals to the V+ pin, and consequently onto the Tip & Ring lines. Waveforms from a DTMF dialer are input at TI (Pin 16) through a current limiting resistor (R_7). Negative feedback around the amplifier reduces the overall gain so that return loss specifications may be met. The voltage gain is calculated using the following equation:

$$\frac{V+}{V_i} = \frac{80\ R_E}{(1\ +\ 0.795R_7\ +\ 0.4R_ER_7)}$$

(R_E, R_7 in kΩ)
where R_E = R_L//2 kΩ (2 kΩ = internal dynamic impedance)

Using 22 kΩ for R_7, and 600 Ω for R_L, the voltage gain is a nominal 4.3 dB. The minimum loop current at which the circuit of Figure 1 will operate without distortion is 12 mA.

The DTMF amplifier is functional only in the tone dialing mode, and the waveform at V+ is inverted from that at TI. The TI pin requires a dc bias current (into the pin) of 20–50 μA, which may be supplied by the Tone dialer circuit, or by using the biasing scheme of Figure 14.

CC (PIN 5)

The CC pin (Compensation Capacitor) has two functions: 1) to provide equalization loop stability where the normal stabilizing components are ineffective; and 2) to allow optional control of the equalization functions.

In most applications, the capacitor at LC (Pin 12) provides the required stability, and no further compensation is required. In applications where changes are forced at Pin 12 and/or 13 (e.g., see Figure 23), the LC capacitor's effectiveness may be lost. The addition of a 10 μF capacitor to Pin 5 will provide the required additional compensation.

The CC pin may be used to force the loop length compensation circuits to specific modes. Grounding CC will set the sidetone and equalization amplifiers at the low loop current values. Connecting CC to V_R will set the amplifiers at the high loop current values.

Variations in the curves of Figures 9 and 11 may be obtained by using external resistors from LR to CC, and from CC to V–.

FIGURE 10 — RECEIVE CIRCUIT

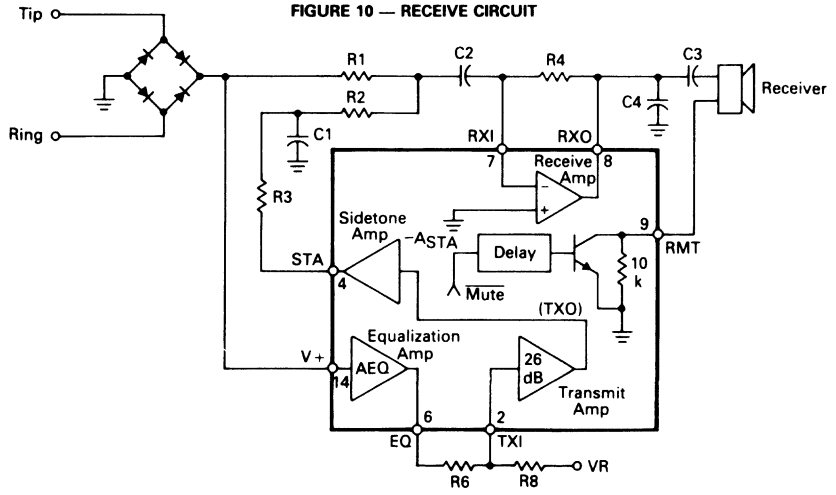


FIGURE 11 — EQUALIZATION AMPLIFIER GAIN

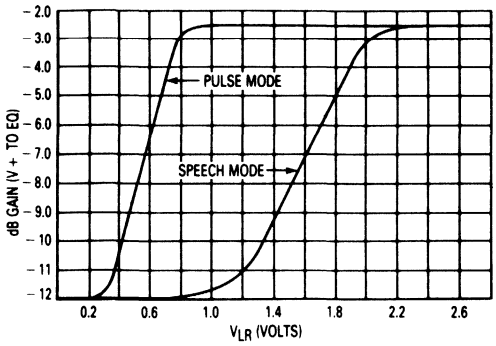
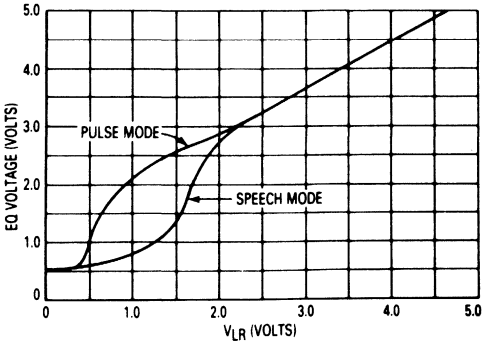


FIGURE 12 — EQ (PIN 6) DC VOLTAGE



3

FIGURE 13 — DTMF TONE DIALER

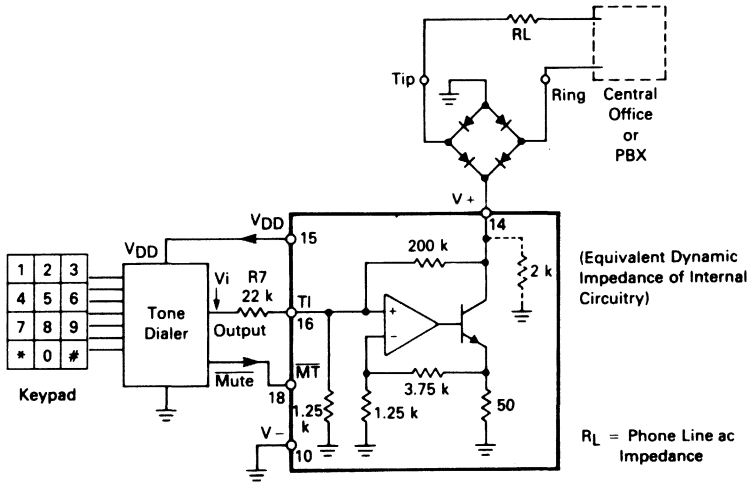
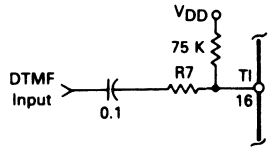


FIGURE 14 — INPUT BIASING



APPLICATIONS INFORMATION

AC IMPEDANCE

One of the basic problems with early telephones is that the performance varied with different line lengths (distance from the Central Office to the telephone). If a particular phone were optimized for short loops and then connected to a long loop, both the transmitted and receive signals would be difficult to hear. On the other hand, phones optimized for long loops would then be annoyingly loud on short loops. The process of equalization is one whereby the performance is forced to vary with loop length inversly to the expected variations. Monitoring of loop length is accomplished by monitoring the loop current at the telephone. In the MC34014, loop length equalization is provided by varying the ac impedance of the telephone circuit. In this manner the MC34014 mimics a passive network, with varistors providing the equalization.

Figure 15 depicts the situation in the receive mode. The receive signal coming from the Central Office is V_S and is independent of the loop length. Z_R is the ac impedance of the Central Office, nominally 900 Ω. Z_L is the characteristic impedance of the phone line, and is a nominal 600 Ω. The signal applied to the line (V_1) is therefore a portion of V_S. That signal is attenuated by the distributive impedance of the phone line, with a resulting signal V_2 at the telephone. The amplitude of V_2 depends on the amount of attenuation, the impedance of the phone line at the telephone and the ac impedance of the telephone (Z_{ac}), according to:

$$V_2 = \frac{V_1' \times Z_{ac}}{Z_{ac} + Z_L}$$

where V_1' is the equivalent signal source at the receive end of the phone line, providing the signal V_2 through the impedance equal to the characteristic impedance of the line (Z_L). The value of V_1' depends on how much V_1 has been attenuated by the length of phone line. By increasing Z_{ac} on long loops, V_2 is a greater portion of V_1', resulting in a stronger receive signal at the telephone.

FIGURE 15 — RECEIVE MODE

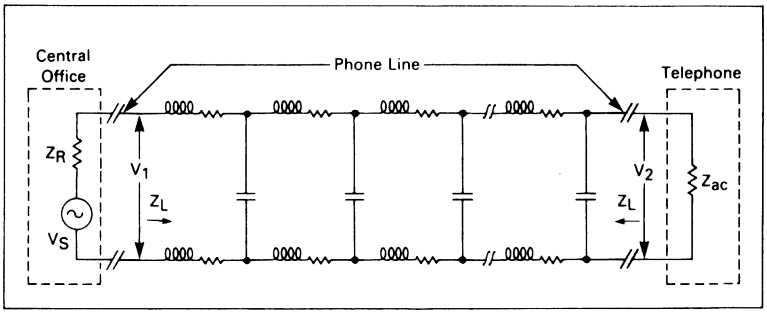
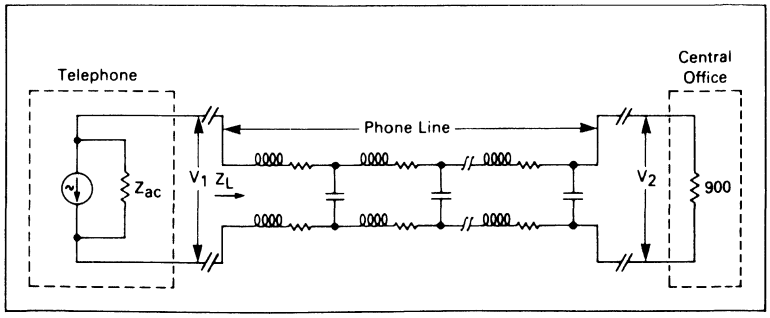


Figure 16 depicts the situation in the transmit mode. In this mode, the MC34014 is an ac current source, with a finite output impedance, modulating the loop current. The voltage signal V_1 is therefore equal to the ac signal current acting on Z_{ac} in parallel with the characteristic impedance of the phone line (Z_L). The signal is attenuated by the distributive impedance of the phone line, and so only a portion of that signal (V_2) appears at the Central Office. By increasing Z_{ac} on long loops, V_1 is increased, resulting in a higher signal level at V_2.

FIGURE 16 — TRANSMIT MODE



The ac impedance of the telephone circuit is determined by the transmit amplifier, equalization amplifier, and external resistors R_6, R_8, and R_9. In Figure 17, a portion of the receive signal at V+ appears at EQ. That signal is reduced at TXI by the R_8-R_6 divider (the electret microphone is a high impedance). The signal at TXI is then amplified by 20, and that signal (at TXO) is converted to an ac current by R9. The ac impedance of the circuit is therefore $V+/I_{TXO}$, and is defined by the following equation:

$$Z_{ac} = \frac{(1 + R_8/R_6)(R_9)}{20 \times A \times (R_8/R_6)}$$

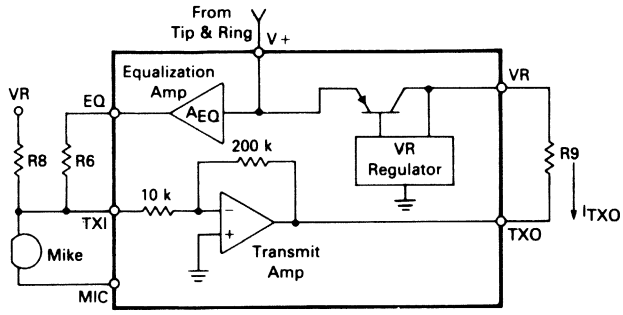
where A = the gain of the equalization amplifier (0.25 to 0.75)

Since the gain of the equalization amplifier varies by a factor of 3, the ac impedance will vary the same amount. Using the resistor values indicated in Figure 1, the ac impedance will vary from 280 Ω (short loop) to 840 Ω (long loop).

When calculating or measuring the ac impedance, capacitor C_6 (≈8.0 kΩ at 1.0 kHz) and the dynamic impedance of the MC34014 (≈10 kΩ) must be taken into account. If the microphone has an impedance lower than that of a typical electret, then its dynamic impedance must be accounted for in the above equation.

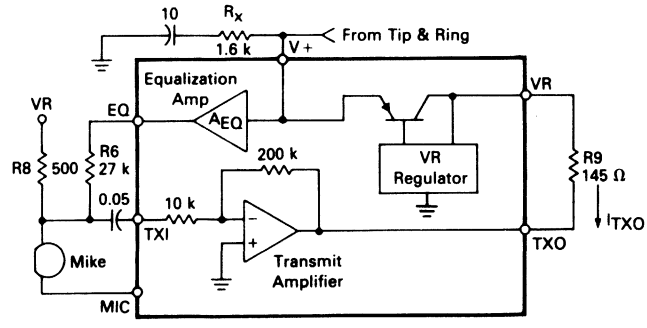
3

FIGURE 17 — DETERMINING AC IMPEDANCE



If a variation in Z_{ac} of less than 3:1 is desired, the circuit configuration of Figure 18 may be used. The ac impedance is the parallel combination of R_x and the impedance presented by the remainder of the circuit. With the values shown in Figure 18, the ac impedance varies from 400 Ω to 800 Ω.

FIGURE 18 — REDUCED AC IMPEDANCE VARIATION



TRANSMIT DESIGN PROCEDURE

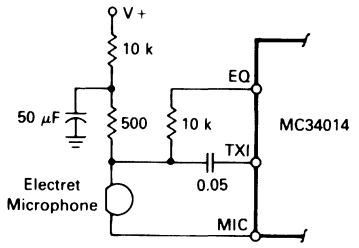
Referring to Figure 17, first select R_9 for the desired maximum output level at Tip & Ring, assuming a signal level at TXO of 1.0 V p-p. The maximum signal level at Tip & Ring will be approximately:

$$\frac{(V_{TXO})\ (Z_L)}{R_9}$$

where Z_L is the characteristic ac impedance of the phone line. Capacitor C_6 and the ≈10 kΩ dynamic impedance of the MC34014 must also be considered in the above computation, since they are in parallel with Z_L.

The next step is to select the R_6/R_8 ratio, according to the required Z_{ac}, using the equation on the previous page. Then R_8 is selected to set the microphone sensitivity. R_8 is typically in the range of 0.5 k to 1.5 kΩ, and is dependent on the characteristics of the microphone. R_6 is then calculated from the above mentioned ratio.

FIGURE 19 — ALTERNATE MICROPHONE BIAS



The overall gain from the microphone to V+ will vary with loop current due to the influence of the equalization amplifier on TXI. The signal at EQ is out of phase with that at TXI, therefore the signal at V+ decreases as loop current (and the EQ signal) increases. Variations are typically 2.0 to 5.0 dB and depend largely on the impedance characteristics of the microphone.

ALTERNATE MICROPHONE BIASING

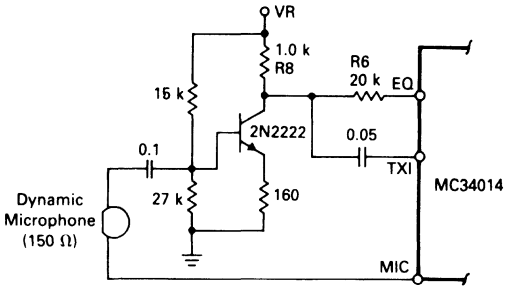
In the event that the microphone cannot be properly biased from the 1.2 volt VR supply, a higher voltage can be obtained by biasing from the V+ supply. The configuration shown in Figure 19, provides a higher voltage to the microphone, and also filters the speech signals at V+ from reaching it, preventing an oscillatory loop from forming. The maximum voltage limit of the microphone must be considered when biasing this way.

If a dynamic microphone is to be used in place of an electret unit, the circuit in Figure 20 will buffer its low impedance from the MC34014 circuit, maintaining the high impedance required at the junction of R_8 and R_6. The circuit shown provides a gain of ≈2.6 for the microphone signals, and can be adjusted by varying the 160 Ω resistor.

HANDSET/HANDS-FREE TELEPHONE

Figure 23 indicates a circuit using the MC34014 speech network, MC34018 speakerphone circuit, and the MC34017 tone ringer to provide a complete telephone/speakerphone. Switch HS (containing one normally open and one normally closed contact) is the hook switch actuated by the handset, shown in the on-hook position. When the handset is off-hook (HS1 open, HS2 closed), power is applied to the MC34014, and consequently the handset, and the $\overline{CS}$ pin of the MC34018 is held high so as to disable it. Upon closing the two poles of switch SS, and placing switch HS in the on-hook position, power is then applied to both the MC34014 and the MC34018, and $\overline{CS}$ is held low, enabling the speakerphone function. Anytime the handset is removed from switch HS, the circuit reverts to the handset mode. The diode circuitry sets the MC34014 to the pulse dialing mode to mute the handset microphone and receiver when using the speakerphone. To compensate for the different equalization response of the MC34014 when in

FIGURE 20 — INTERFACING A DYNAMIC MICROPHONE



the pulse dialing mode (Figures 9 and 11), the 47 Ω resistor normally found at Pin 13 of the MC34014 is instead divided into two resistors (33 Ω and 15 Ω). This arrangement provides similar equalization response in both the handset and in the speakerphone modes. Since the LC capacitor (Pin 12) is ineffective in the speakerphone mode, a capacitor is added at Pin 5 (CC) to provide compensation for the equalization loop when the speakerphone mode is in effect.

SWITCHABLE TONE/PULSE TELEPHONE

Figure 21 indicates a switchable tone/pulse telephone circuit using the MC145412 tone/pulse dialer, MC34014 speech network, and the MC34017 tone ringer. The dialer is programmable, and can store up to 10 phone numbers. As can be seen, the interface to the MC34014 is straightforward.

PULSE ONLY TELEPHONE

Figure 22 indicates a pulse only telephone circuit using the MC145409 pulse dialer, MC34014 speech network, and the MC34017 tone ringer. The dialer has last number redial, and provides a pacifier tone to the receiver during dialing.

FIGURE 21 — COMPLETE TELEPHONE WITH PULSE/TONE DIALING

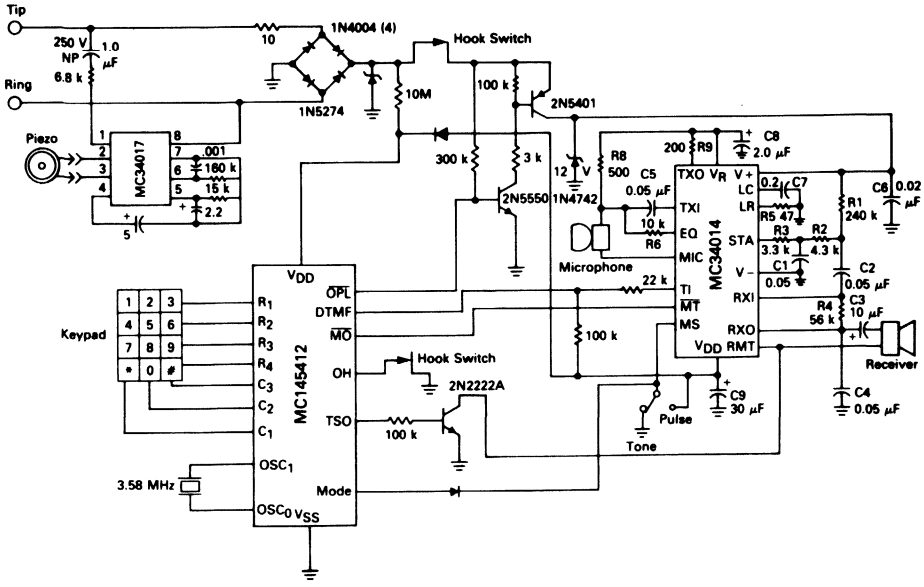
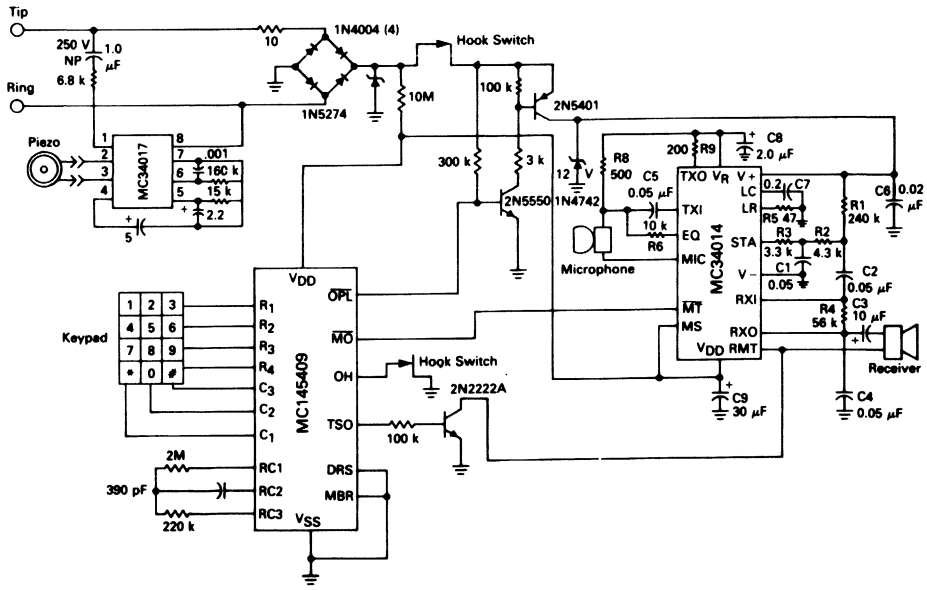


FIGURE 22 — COMPLETE TELEPHONE WITH PULSE DIALING



3

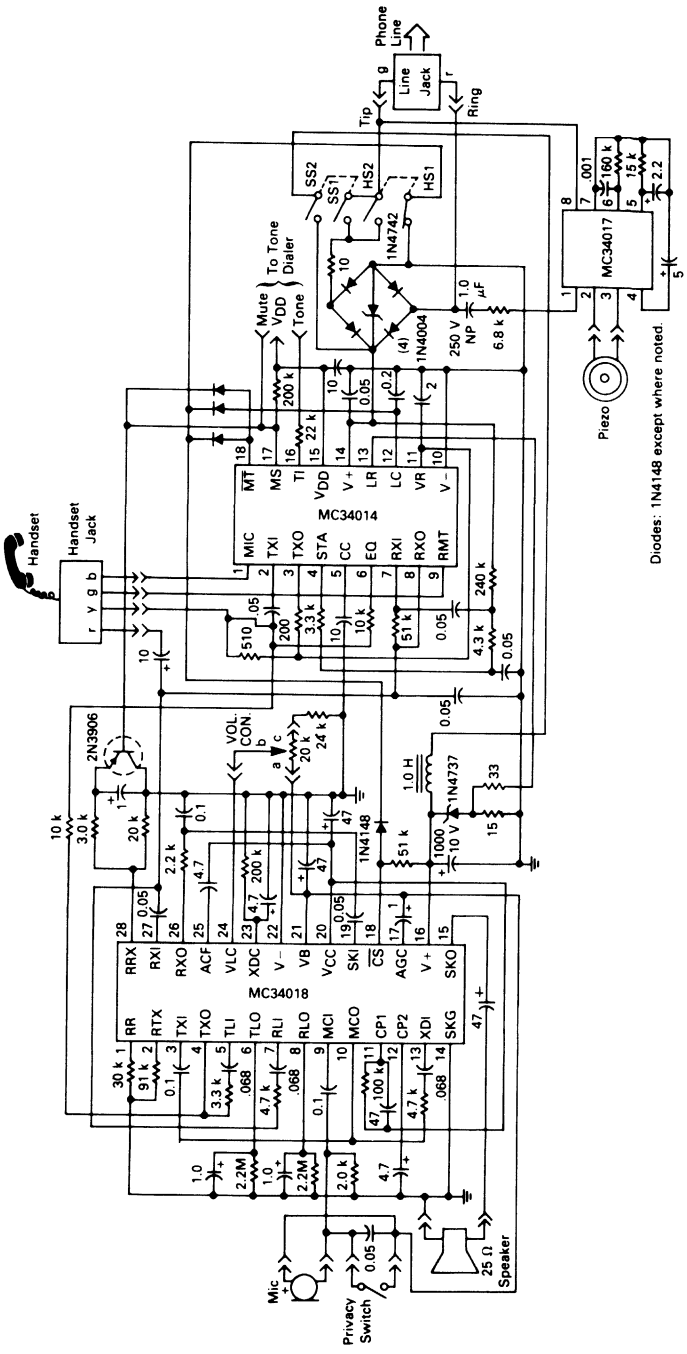


FIGURE 23 — SWITCHABLE HANDSET/HANDSFREE SYSTEM

Recommended External Components

Piezo Sounder
Models KSN 1113-1116
Motorola, Inc.
Albuquerque, N.M.
505-822-8801

Microhone/Receiver
Microphone model EM-95
Receiver model DH-34
Primo Microphone, Inc.
Elk Grove Village, Ill.
312-595-1022

Microphone Model KUC2123
Hosiden Electronics
Chicago, Ill.
312-956-7707

TRANSIENT PROTECTION & RFI SUPPRESSION

Protection from voltage transients is necessary in most telephone circuits, and may take the form of zener diodes, RC or LC filters, transient suppressors (MO•sorb), or a combination of the above.

Potential radio frequency interference problems should be addressed early in the electrical and mechanical design of the telephone. RFI may enter the circuitry through the Tip & Ring lines, through the microphone and/or receiver leads in the handset cord, or through any of the wiring or PC board traces. Ceramic decoupling capacitors, ferrite beads, and other RFI suppression techniques may be needed. Good PC board design techniques, such as the avoidance of loops, should be used. Long tracks on high impedance nodes should be avoided.

MOTOROLA

MC34017

Advance Information

TELEPHONE TONE RINGER

- Complete Telephone Bell Replacement Circuit with Minimum External Components
- On-Chip Diode Bridge and Transient Protection
- Direct Drive for Piezoelectric Transducers
- Push Pull Output Stage for Greater Output Power Capability
- Base Frequency Options — MC34017-1: 1.0 kHz
  MC34017-2: 2.0 kHz
  MC34017-3: 500 Hz
- Input Impedance Signature Meets Bell and EIA Standards
- Rejects Rotary Dial Transients

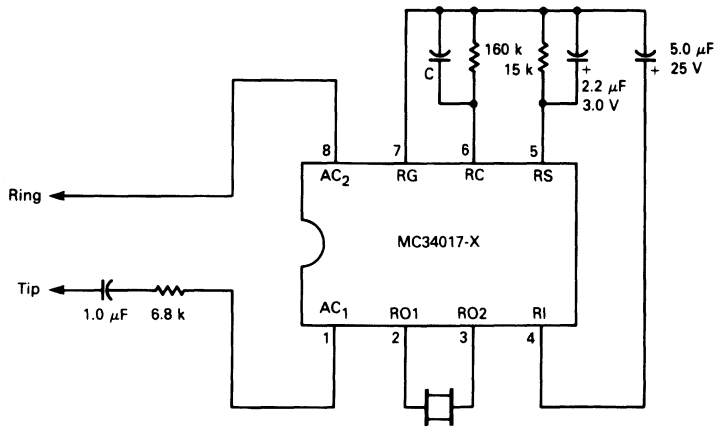
TELEPHONE TONE RINGER

BIPOLAR LINEAR/I²L

P SUFFIX
PLASTIC PACKAGE
CASE 626-04

D SUFFIX
PLASTIC PACKAGE
CASE 751A-01

APPLICATION CIRCUIT



MC34017-1: C = 1000 pF
MC34017-2: C = 500 pF
MC34017-3: C = 2000 pF

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ADI795

APPLICATION CIRCUIT PERFORMANCE (Refer to Circuit on First Page.)

Characteristic	Typical Value	Units
Output Tone Frequencies MC34017-1 MC34017-2 MC34017-3 Warble Frequency	 808/1010 1616/2020 404/505 12.5	Hz
Output Voltage ($V_I \geq 60\ V_{rms}$, 20 Hz)	37	V_{p-p}
Output Duty Cycle	50	%
Ringing Start Input Voltage (20 Hz)	36	V_{rms}
Ringing Stop Input Voltage (20 Hz)	21	V_{rms}
Maximum ac Input Voltage ($\leq$ 68 Hz)	150	V_{rms}
Impedance When Ringing $V_I = 40\ V_{rms}$, 15 Hz $V_I = 130\ V_{rms}$, 23 Hz	 >16 12	kΩ
Impedance When Not Ringing $V_I = 10\ V_{rms}$, 24 Hz $V_I = 2.5\ V_{rms}$, 24 Hz $V_I = 10\ V_{rms}$, 5.0 Hz $V_I = 3.0\ V_{rms}$, 200–3200 Hz	 28 >1.0 55 >200	 kΩ MΩ kΩ kΩ
Maximum Transient Input Voltage (T $\leq$ 2.0 ms)	1500	V
Ringer Equivalence: Class A Class B	0.5 0.9	— —

PIN DESCRIPTIONS

Name	Description
AC_1, AC_2	The input terminals to the full-wave diode bridge. The ac ringing signal from the telephone line energizes the ringer through this bridge.
RS	The input of the threshold comparator to which diode bridge current is mirrored and sensed through an external resistor (R3). Nominal threshold is 1.2 volts. This pin internally clamps at 1.5 volts.
RI	The positive supply terminal for the oscillator, frequency divider and output buffer circuits.
RO1, RO2	The tone ringer output terminals through which the sound element is driven.
RG	The negative terminal of the diode bridge and the negative supply terminal of the tone generating circuitry.
RC	The oscillator terminal for the external resistor and capacitor which control the tone ringer frequencies (R2, C2).

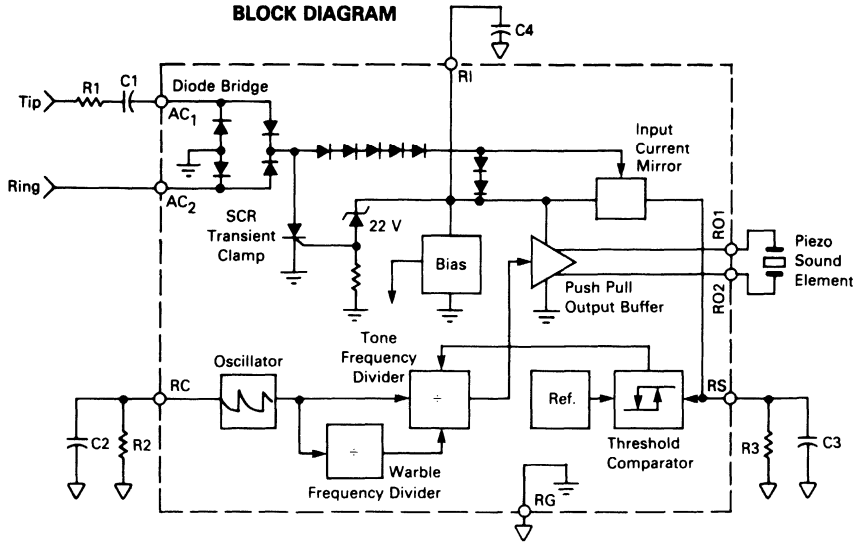
MAXIMUM RATINGS (Voltages Referenced to RG, Pin 7)

Parameter	Value	Unit
Operating AC Input Current (Pins 1, 8)	20	mA, RMS
Transient Input Current (Pins 1, 8) (T<2.0 ms)	±300	mA, peak
Voltage Applied at RC (Pin 6)	5.0	V
Voltage Applied at RS (Pin 5)	5.0	V
Voltage Applied to Outputs (Pins 2, 3)	−2.0 to V_{RI}	V
Power Dissipation (@ 25°C)	1.0	W
Operating Temperature Range	−20 to +60	°C
Storage Temperature Range	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristic	Test	Symbol	Min	Typ	Max	Units
Ringing Start Voltage (V_{Start} = V_I @ Ring Start)						Vdc
V_I>0	1a	$V_{Start}(+)$	34	37.5	41	
V_I<0	1b	$V_{Start}(-)$	−34	−37.5	−41	
Ringing Stop Voltage (V_{Stop} = V_I @ Ring Stop)	1c	V_{Stop}				Vdc
MC34017-1			14	16	22	
MC34017-2			12	14	20	
MC34017-3			14	16	22	
Output Frequencies (V_I = 50 V)	1d					Hz
MC34017-1 High Tone		f_H	937	1010	1083	
Low Tone		f_L	752	808	868	
Warble Tone		f_W	11.5	12.5	14	
MC34017-2 High Tone		f_H	1874	2020	2166	
Low Tone		f_L	1504	1616	1736	
Warble Tone		f_W	11.5	12.5	14	
MC34017-3 High Tone		f_H	937	1010	1083	
Low Tone		f_L	752	808	868	
Warble Tone		f_W	23	25	28	
Output Voltage (V_I = 50 V)	6	V_O	34	37	43	V_{p-p}
Output Short-Circuit Current	2	I_{RO1}, I_{RO2}	35	60	80	mA_{p-p}
Input Diode Voltage (I_I = 5.0 mA)	3	V_D	5.6	6.2	6.8	Vdc
Input Voltage — SCR Off (I_I = 30 mA)	4a	V_{off}	33	38	43	Vdc
Input Voltage — SCR On (I_I = 100 mA)	4b	V_{on}	3.2	4.1	6.0	Vdc
RS Clamp Voltage (V_I = 50 V)	5	V_{clamp}	1.3	1.5	1.8	Vdc

BLOCK DIAGRAM



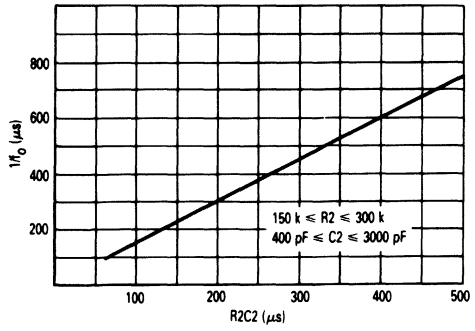
CIRCUIT DESCRIPTION

The MC34017 Tone Ringer derives its power supply by rectifying the ac ringing signal. It uses this power to activate a tone generator and drive a piezo-ceramic transducer. The tone generation circuitry includes a relaxation oscillator and frequency dividers which produce high and low frequency tones as well as the tone warble frequency. The relaxation oscillator frequency f_O is set by resistor R2 and capacitor C2 connected to pin RC. The oscillator will operate with f_O from 1.0 kHz to 10 kHz with the proper choice of external components (See Figure 1).

The frequency of the tone ringer output signal at RO1 and RO2 alternates between $f_O/4$ to $f_O/5$. The warble rate at which the frequency changes is $f_O/320$ for the MC34017-1, $f_O/640$ for the MC34017-2, and $f_O/160$ for the MC34017-3. With a 4.0 kHz oscillator frequency, the MC34017-1 produces 800 Hz and 1000 Hz tones with a 12.5 Hz warble rate. The MC34017-2 generates 1600 Hz and 2000 Hz tones with a similar 12.5 Hz warble frequency from an 8.0 kHz oscillator frequency. The MC34017-3 will produce 400 Hz and 500 Hz tones with a 12.5 Hz warble rate from a 2.0 kHz oscillator frequency. The tone ringer output circuit can source or sink 20 mA with an output voltage swing of 37 volts peak-to-peak. Volume control is readily implemented by adding a variable resistance in series with the piezo transducer.

Input signal detection circuitry activates the tone ringer output when the ac line voltage exceeds programmed threshold level. Resistor R3 determines the ringing signal amplitude at which an output signal at RO1 and RO2 will be generated. The ac ringing signal is rectified by the internal diode bridge. The rectified input signal produces a voltage across R3 which is referenced to RG. The voltage across resistor R3 is filtered by capacitor C3 at the input to the threshold circuit.

FIGURE 1 — OSCILLATOR PERIOD ($1/f_O$) versus OSCILLATOR R2 C2 PRODUCT



($1/f_O$ = 1.45 R2C2 + 10 μs)

When the voltage on capacitor C3 exceeds 1.2 volts, the threshold comparator enables the tone ringer output. Line transients produced by pulse dialing telephones do not charge capacitor C3 sufficiently to activate the tone ringer output.

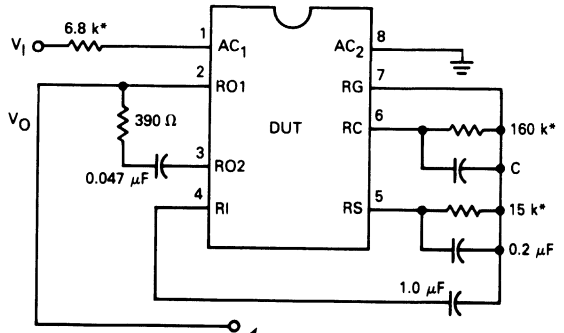
Capacitors C1 and C4 and resistor R1 determine the 10 volt, 24 Hz signature test impedance. C4 also provides filtering for the output stage power supply to prevent droop in the square wave output signal. Six diodes in series with the rectifying bridge provide the necessary non-linearity for the 2.5 volt, 24 Hz signature tests.

An internal shunt voltge regulator between the RI and RG terminals provides dc voltage to power output stage, oscillator, and frequency dividers. The dc voltage at RI is limited to approximately 22 volts in regulation. To protect the IC from telephone line transients, an SCR is triggered when the regulator current exceeds 50 mA. The SCR diverts current from the shunt regulator and reduces the power dissipation within the IC.

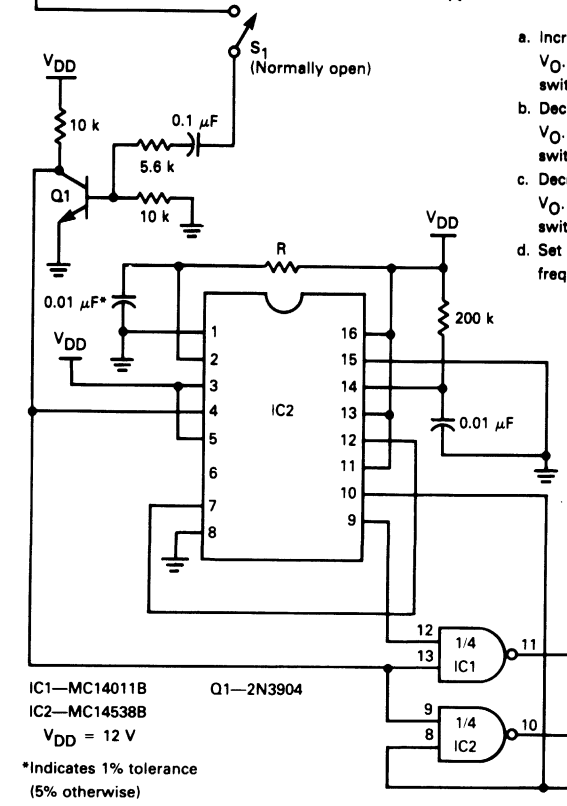
EXTERNAL COMPONENTS

R1	Line input resistor. R1 affects the tone ringer input impedance. It also influences ringing threshold voltage and limits current from line transients. (Range: 2.0 kΩ to 10 kΩ).
C1	Line input capacitor. C1 ac couples the tone ringer to the telephone line and controls ringer input impedance at low frequencies. (Range: 0.4 μF to 2.0 μF).
R2	Oscillator resistor. (Range: 150 kΩ to 300 kΩ).
C2	Oscillator capacitor. (Range: 400 pF to 3000 pF).
R3	Input current sense resistor. R3 controls the ringing threshold voltage. Increasing R3 decreases the ring-start voltage. (Range: 5.0 kΩ to 18 kΩ).
C3	Ringing threshold filter capacitor. C3 filters the ac voltage across R3 at the input of the ringing threshold comparator. It also provides dialer transient rejection. (Range: 0.5 μF to 5.0 μF).
C4	Ringer supply capacitor. C4 filters supply voltage for the tone generating circuits. It also provides an ac current path for the 10 V_{rms} ringer signature impedance. (Range: 1.0 μF to 10 μF).

FIGURE 2 — TEST ONE



MC34017-1: C = 1000 pF*
MC34017-2: C = 500 pF*
MC34017-3: C = 1000 pF*



a. Increase V_I from +33 volts while monitoring V_O. $V_{Start}(+)$ equals V_I when V_O commences switching.

b. Decrease V_I from −33 volts while monitoring V_O. $V_{Start}(-)$ equals V_I when V_O commences switching.

c. Decrease V_I from +40 volts while monitoring V_O. V_{Stop} equals V_I when V_O ceases switching.

d. Set V_I to +50 volts. Close S1. Measure frequencies f_H, f_L, and f_W.

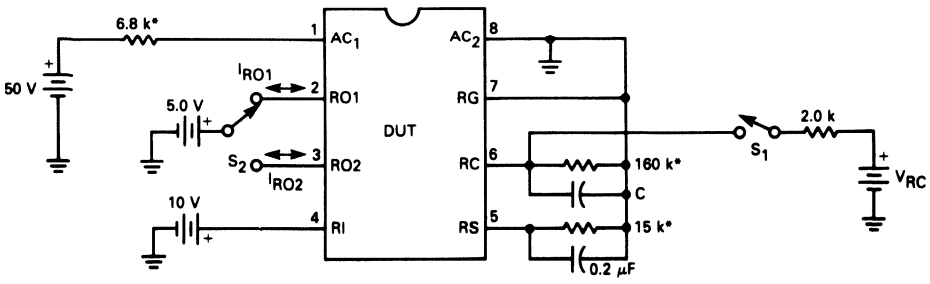
IC1—MC14011B
IC2—MC14538B
V_{DD} = 12 V

Q1—2N3904

*Indicates 1% tolerance (5% otherwise)

MC34017-1: R = 110 kΩ*
MC34017-2: R = 55 kΩ*
MC34017-3: R = 110 kΩ*

FIGURE 3 — TEST TWO



With V_{RC} = 4.0 volts, close S_1. Switch S_2 to Pin 2 and measure current at Pin 2 (Io1). Repeatedly switch V_{RC} between 4.0 volts and 0 volts until Pin 2 current changes polarity. Measure the opposite polarity current (Io2). Calculate:

$I_{RO1} = |Io1| + |Io2|$

Switch S2 to Pin 3 and repeat.

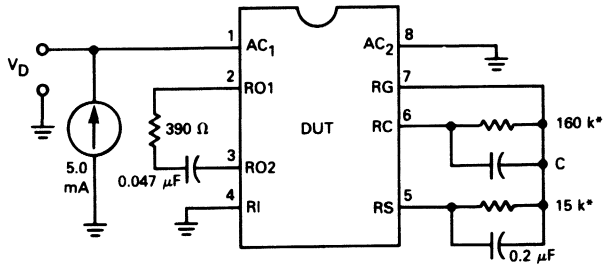
Calculate:

$I_{RO2} = |Io1| + |Io2|$

MC34017-1: C = 1000 pF*
MC34017-2: C = 500 pF*
MC34017-3: C = 1000 pF*

*Indicates 1% tolerance (5% otherwise)

FIGURE 4 — TEST THREE

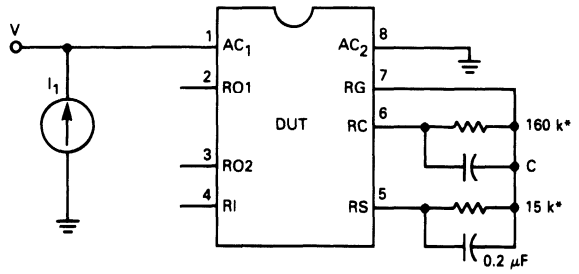


Measure voltage at Pin 1.

MC34017-1: C = 1000 pF*
MC34017-2: C = 500 pF*
MC34017-3: C = 1000 pF*

*Indicates 1% tolerance (5% otherwise)

FIGURE 5 — TEST FOUR



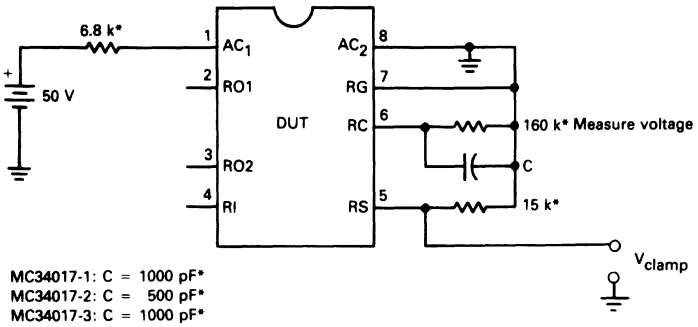
MC34017-1: C = 1000 pF*
MC34017-2: C = 500 pF*
MC34017-3: C = 1000 pF*

*Indicates 1% tolerance (5% otherwise)

a. Set I_I to 30 mA. Measure voltage at Pin 1 (V_{off}).
b. Set I_I to 100 mA. Measure voltage at Pin 1 (V_{on}).

(Each test < 30 ms)

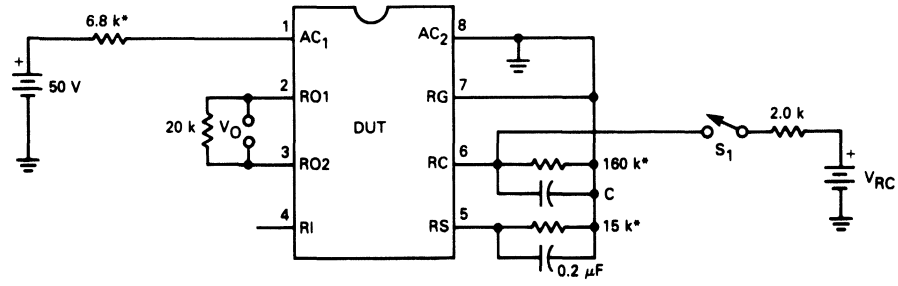
FIGURE 6 — TEST FIVE



MC34017-1: C = 1000 pF*
MC34017-2: C = 500 pF*
MC34017-3: C = 1000 pF*

*Indicates 1% tolerance (5% otherwise)

FIGURE 7 — TEST SIX



MC34017-1: C = 1000 pF*
MC34017-2: C = 500 pF*
MC34017-3: C = 1000 pF*

*Indicates 1% tolerance (5% otherwise)

With V_{RC} = 4.0 volts, close S_1. Measure dc voltage between Pins 2 and 3 (Vo1). Repeatedly switch V_{RC} between 4.0 volts and 0 volts until Pins 2 and 3 change state. Measure the new voltage between Pins 2 and 3 (Vo2).
Calculate:
$V_O = |Vo1| + |Vo2|$

3

MOTOROLA

MC34018

Specifications and Applications Information

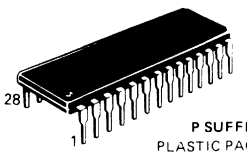
VOICE SWITCHED SPEAKERPHONE CIRCUIT

The MC34018 Speakerphone integrated circuit incorporates the necessary amplifiers, attenuators, and control functions to produce a high quality hands-free speakerphone system. Included are a microphone amplifier, a power audio amplifier for the speaker, transmit and receive attenuators, a monitoring system for background sound level, and an attenuation control system which responds to the relative transmit and receive levels as well as the background level. Also included are all necessary regulated voltages for both internal and external circuitry, allowing line-powered operation (no additional power supplies required). A Chip Select pin allows the chip to be powered down when not in use. A volume control function may be implemented with an external potentiometer. MC34018 applications include speakerphones for household and business use, intercom systems, automotive telephones, and others.

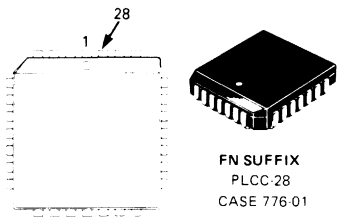
- All necessary level detection and attenuation controls for a hands-free telephone in a single integrated circuit
- Background noise level monitoring with long time constant
- Wide operating dynamic range through signal compression
- On-chip supply and reference voltage regulation
- Typical 100 mW output power (into 25 Ohms) with peak limiting to minimize distortion
- Chip Select pin for active/standby operation
- Linear Volume Control Function
- Standard 28-pin plastic DIP package (0.600 inch wide) and PLCC package

VOICE SWITCHED SPEAKERPHONE CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

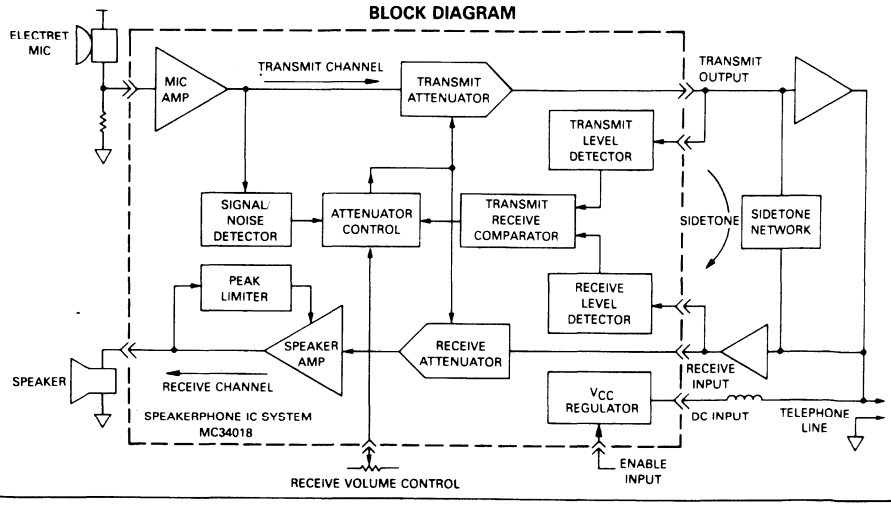


P SUFFIX
PLASTIC PACKAGE
CASE 710-02



FN SUFFIX
PLCC-28
CASE 776-01

BLOCK DIAGRAM



DS9664R1

PIN DESCRIPTION

Pin	Name	Description
1	RR	A resistor to ground provides a reference current for the transmit and receive attenuators.
2	RTX	A resistor to ground determines the nominal gain of the transmit attenuator. The transmit channel gain is inversely proportional to the RTX resistance.
3	TXI	Input to the transmit attenuator. Input resistance is nominally 5.0 k ohms.
4	TXO	Output of the transmit attenuator. The TXO output signal drives the input of the transmit level detector, as well as the external circuit which drives the telephone line.
5	TLI	Input of the transmit level detector. An external resistor ac coupled to the TLI pin sets the detection level. Decreasing this resistor increases the sensitivity to transmit channel signals.
6	TLO	Output of the transmit level detector. The external resistor and capacitor set the time the comparator will hold the system in the transmit mode after speech ceases.
7	RLI	Input of the receive level detector. An external resistor ac coupled to the RLI pin sets the detection level. Decreasing this resistor increases the sensitivity to receive channel signals.
8	RLO	Output of the receive level detector. The external resistor and capacitor set the time the comparator will hold the system in the receive mode after the receive signal ceases.
9	MCI	Microphone amplifier input. Input impedance is nominally 10 k ohms and the dc bias voltage is approximately equal to VB.
10	MCO	Microphone amplifier output. The mic amp gain is internally set at 34 dB (50 V/V).
11	CP1	A parallel resistor and capacitor connected between this pin and V_{CC} holds a voltage corresponding to the background noise level. The transmit detector compares the CP1 voltage with the speech signal from CP2.
12	CP2	A capacitor at this pin peak detects the speech signals for comparison with the background noise level held at CP1.
13	XDI	Input to the transmit detector system. The microphone amplifier output is ac coupled to the XDI pin through an external resistor.
14	SKG	High current ground pin for the speaker amp output stage. The SKG voltage should be within 10 mV of the ground voltage at Pin 22.
15	SKO	Speaker amplifier output. The SKO pin will source and sink up to 100 mA when ac coupled to the speaker. The speaker amp gain is internally set at 34 dB (50 V/V).
16	V+	Input dc supply voltage. V+ can be powered from Tip and Ring if an ac decoupling inductor is used to prevent loading ac line signals. The required V+ voltage is 6.0 to 11 V (7.5 V nominal) at 7.0 mA.
17	AGC	A capacitor from this pin to VB stabilizes the speaker amp gain control loop, and additionally controls the attack and decay time of this circuit. The gain control loop limits the speaker amp input to prevent clipping at SKO. The internal resistance at the AGC pin is nominally 110 k ohms.
18	$\overline{CS}$	Digital chip select input. When at a Logic "0" (<0.7 V) the V_{CC} regulator is enabled. When at a Logic "1" (>1.6 V), the chip is in the standby mode drawing 0.5 mA. An open $\overline{CS}$ pin is a Logic "0". Input impedance is nominally 140 k ohms. The input voltage should not exceed 11 V.
19	SKI	Input to the speaker amplifier. Input impedance is nominally 20 k ohms.
20	V_{CC}	A 5.4 V regulated output which powers all circuits except the speaker amplifier output stage. V_{CC} can be used to power external circuitry such as a microprocessor (3.0 mA max). A filter capacitor is required. The MC34018 can be powered by a separate regulated supply by connecting V+ and V_{CC} to a voltage between 4.5 V and 6.5 V while maintaining $\overline{CS}$ at a Logic "1".
21	VB	An output voltage equal to approximately $V_{CC}/2$ which serves as an analog ground for the speakerphone system. Up to 1.5 mA of external load current may be sourced from VB. Output impedance is 250 ohms. A filter capacitor is required.
22	Gnd	Ground pin for the IC (except the speaker amplifier).
23	XDC	Transmit detector output. A resistor and capacitor at this pin hold the system in the transmit mode during pauses between words or phrases. When the XDC pin voltage decays to ground, the attenuators switch from the transmit mode to the idle mode. The internal resistor at XDC is nominally 2.6 k ohms (see Figure 1).
24	VLC	Volume control input. Connecting this pin to the slider of a variable resistor provides receive mode volume control. The VLC pin voltage should be less than or equal to VB.
25	ACF	Attenuator control filter. A capacitor connected to this pin reduces noise transients as the attenuator control switches levels of attenuation.
26	RXO	Output of the receive attenuator. Normally this pin is ac coupled to the input of the speaker amplifier.
27	RXI	Input of the receive attenuator. Input resistance is nominally 5.0 k ohms.
28	RRX	A resistor to ground determines the nominal gain of the receive attenuator. The receive channel gain is directly proportional to the RRX resistance.

Note: Pin numbers are identical for the DIP and PLCC packages.

3

ABSOLUTE MAXIMUM RATINGS

(Voltages referred to Pin 22) (T_A = 25°C)

Parameter	Value	Units
V+ Terminal Voltage (Pin 16)	+12, −1.0	V
$\overline{CS}$ (Pin 18)	+12, −1.0	V
Speaker Amp Ground (Pin 14)	+3.0, −1.0	V
VLC (Pin 24)	V_{CC}, −1.0	V
Storage Temperature	−65 to +150	°C

"Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The "Electrical Characteristics" tables provide conditions for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Parameter	Value	Units
V+ Terminal Voltage (Pin 16)	+6.0 to +11	V
$\overline{CS}$ (Pin 18)	0 to +11	V
I_{CC} (Pin 20)	0 to 3.0	mA
VLC (Pin 24)	0.55VB to VB	V
Receive Signal (Pin 27)	0 to 250	mV_{rms}
Microphone Signal (Pin 9)	0 to 5.0	mV_{rms}
Speaker Amp Ground (Pin 14)	−10 to +10	mVdc
Ambient Temperature	−20 to +60	°C

ELECTRICAL CHARACTERISTICS (Refer to Figure 1)

Parameter	Symbol	Pin	Min	Typ	Max	Units
SUPPLY VOLTAGES						
V+ Supply Current	I_{V+}	16				
V+ = 11 V, Pin 18 = 0.7 V			—	—	9.0	mA
V+ = 11 V, Pin 18 = 1.6 V			—	—	800	μA
V_{CC} Voltage (V+ = 7.5 V)	V_{CC}	20	4.9	5.4	5.9	Vdc
Line Regulation (6.5 V < V+ < 11 V)	$\Delta V_{CC\ LN}$		—	65	150	mV
Output Resistance (I_{CC} = 3.0 mA)	R_{OVCC}		—	6.0	20	ohms
Dropout Voltage (V+ = 5.0 V)	$V_{CC\ SAT}$		—	80	300	mV
VB Voltage (V+ = 7.5 V)	V_B	21	2.5	2.9	3.3	Vdc
Output Resistance (IB = 1.7 mA)	R_{OVB}		—	250	—	ohms
ATTENUATORS						
Receive Attenuator Gain (@ 1.0 kHz)		26,				
Rx Mode, Pin 24 = VB; Pin 27 = 250 mV_{rms}	G_{RX}	27	2.0	6.0	10	dB
Range (Rx to Tx Modes)	ΔG_{RX}		40	44	48	dB
Idle Mode, Pin 27 = 250 mV_{rms}	G_{RXI}		−20	−16	−12	dB
RXO Voltage (Rx Mode)	V_{RXO}		1.8	2.3	3.2	Vdc
Delta RXO Voltage (Switch from RX to TX Mode)	ΔV_{RXO}		—	—	100	mV
RXO Sink Current (Rx Mode)	I_{RXOL}		75	—	—	μA
RXO Source Current (Rx Mode)	I_{RXOH}		1.0	—	3.0	mA
RXI Input Resistance	R_{RXI}		3.5	5.0	8.0	kΩ
Volume Control Range (Rx Attenuator Gain, Rx Mode, 0.6 VB < Pin 24 < VB)	V_{CR}		24.5	—	32.5	dB

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Symbol	Pin	Min	Typ	Max	Units
ATTENUATORS						
Transmit Attenuator Gain (@ 1.0 kHz)		3,				
Tx Mode, Pin 3 = 250 mV_{rms}	G_{TX}	4	4.0	6.0	8.0	dB
Range, (Tx to Rx Mode)	ΔG_{TX}		40	44	48	dB
Idle Mode, Pin 3 = 250 mV_{rms}	G_{TXI}		−16.5	−13	−8.5	dB
TXO Voltage (Tx Mode)	V_{TXO}		1.8	2.3	3.2	Vdc
Delta TXO Voltage (Switch from Tx to Rx Mode)	ΔV_{TXO}		—	—	100	mV
TXO Sink Current (Tx Mode)	I_{TXOL}		75	—	—	μA
TXO Source Current (Tx Mode)	I_{TXOH}		1.0	—	3.0	mA
TXI Input Resistance	R_{TXI}		3.5	5.0	8.0	kΩ
ACF Voltage (V_{CC} − Pin 25 Voltage)	ΔV_{ACF}	20,				
Rx Mode		25	—	150	—	mV
Rx Mode			—	6.0	—	mV
Idle Mode			—	75	—	mV
SPEAKER AMPLIFIER						
Speaker Amp Gain (Pin 19 = 20 mV_{rms})	G_{SPK}	15, 19	33	34	35	dB
SKI Input Resistance	R_{SKI}		15	22	37	kΩ
SKO Voltage (Pin 19 = Cap Couple to GND)	V_{SKO}		2.4	3.0	3.6	Vdc
SKO High Voltage (Pin 19 = 0.1 V, −100 mA load at Pin 15)	V_{SKOH}		5.5	—	—	Vdc
SKO Low Voltage (Pin 19 = −0.1 V, +100 mA load at Pin 15)	V_{SKOL}		—	—	600	mV
MICROPHONE AMPLIFIER						
Mike Amp Gain (Pin 9 = 10 mV_{rms}, 1.0 kHz)	G_{MCI}	9, 10	32.5	34	35	dB
Mike Amp Input Resistance	R_{MCI}		6.5	10	16	kΩ
LOGAMPS						
RLO Leakage Current (Pin 8 = VB + 1.0 V)	I_{LKRLO}	8	—	—	2.0	μA
TLO Leakage Current (Pin 6 = VB + 1.0 V)	I_{LKTLO}	6	—	—	2.0	μA
Transmit-Receive Switching Threshold (Ratio of ITLI to IRLI — at 20 μA — to switch Tx-Rx Comparator)	I_{TH}	5,7 25	0.8	—	1.2	
TRANSMIT DETECTOR						
XDC Voltage — Idle Mode	V_{XDC}	23	—	0	—	Vdc
Tx Mode			—	4.0	—	Vdc
CP2 Current Source	I_{CP2}	12	5.0	10	13	μA
DISTORTION						
Rx Mode — RXI to SKO (Pin 27 = 10 mV_{rms}, 1.0 kHz)	R_{XD}	27, 15	—	1.5	—	%
Tx Mode — MCI to TXO (Pin 9 = 5.0 mV_{rms}, 1.0 kHz)	T_{XD}	4,9	—	2.0	—	%

NOTES: 1. V+ = 7.5 V, $\overline{CS}$ = 0.7 V except where noted.
2. Rx Mode: Pin 7 = −100 μA, Pin 5 = +100 μA, except where noted.
Tx Mode: Pin 5, 13 = −100 μA, Pin 7 = +100 μA, Pin 11 = 0 volts.
Idle Mode: Pin 5 = −100 μA, Pin 7, 13 = +100 μA.
3. Current into a pin designated as +; current out of a pin designated as −.
4. Voltages referred to Pin 22. T_A = +25°C.

TEMPERATURE CHARACTERISTICS (−20 to +60°C)

Parameter	Pin	Typical Change	Units
V+ Supply Current (V+ = 11 V, Pin 18 = 0.7 V)	16	−0.2	%/°C
V+ Supply Current (V+ = 11 V, Pin 18 = 1.6 V)	16	−0.4	%/°C
V_{CC} Voltage (V+ = 7.5 V)	20	+0.1	%/°C
Attenuator Gain (Max and Min Settings)		±0.003	dB/°C
Delta RXO, TXO Voltages	4,26	±0.24	%/°C
Speaker Amp Gain	15,19	±0.003	dB/°C
Microphone Amp Gain	9,10	±0.001	dB/°C
Microphone Amp Input Resistance	9	−0.4	%/°C
Tx-Rx Switching Threshold (@ 20 μA)	5,7	±0.2	nA/°C

DESIGN GUIDELINES (Refer to Figure 1)

ATTENUATORS

The transmit and receive attenuators are complementary in function, i.e., when one is at maximum gain the other is at maximum attenuation, and vice versa. They are never both on or both off. Their main purpose is to control the transmit and receive paths to provide the half-duplex operation required of a speakerphone. The attenuators are controlled solely by the voltage at the ACF pin (Pin 25). The ACF voltage is provided by the Attenuator Control block, which receives 3 inputs: a) the Rx-Tx Comparator, b) the Transmit Detector Comparator, and c) the Volume Control. The response of the attenuators is based on the difference of the ACF voltage from V_{CC}, and therefore a simple method for monitoring the circuit operation is to monitor this voltage difference (referred to as ΔVacf). If ΔVacf is approximately 6 millivolts the transmit attenuator is fully on and the receive attenuator is fully off (transmit mode). If ΔVacf is approximately 150 millivolts the circuit is in the receive mode. If ΔVacf is approximately 75 millivolts, the circuit is in the idle mode, and the two attenuators are at gain settings approximately half way (in dB) between their fully on and fully off positions.

The maximum gain and attenuation values are determined by the three resistors RR, RTX, and RRX (Refer to Figures 2, 3 and 4). RR affects both attenuators according to its value RELATIVE to RTX and RRX, which is why Figure 4 indicates the variations versus the ratio of the other resistors to RR. (GRX and GTX are the maximum gains, and ARX and ATX are the maximum attenuations). RTX affects the gain and attenuation of only the transmit attenuator according to the curves of Figure 2, while RRX affects only the receive attenuator according to Figure 3. As can be seen from the figures, the gain difference (from on to off) is a reasonably constant 45 dB until the upper gain limit is approached. A value of 30 k is recommended for RR as a starting point, and then RTX and RRX selected to suit the particular design goals.

The input impedance of the attenuators (at TXI and RXI) is typically 5.0 kΩ, and the maximum input signal which will not cause output distortion is 250 mV_{rms} (707 mVp-p). The 4300 ohm resistor and 0.01 μF capacitor at RXO (in Figure 1) filters out high frequency components in the receive path. This helps minimize high frequency acoustic feedback problems which may occur if the filter were not present. The filter's insertion loss is 1.5 dB at 1.0 kHz. The outputs of the attenuators are inverted from their inputs.

Referring to the attenuator control block, the ΔVacf voltage at its output is determined by three inputs. The relationship of the inputs and output is summarized in the following truth table:

Tx-Rx Comp	Transmit Det Comp	Volume Control	ΔVacf	Mode
Transmit	Transmit	No Effect	6.0 mV	Transmit
Transmit	Idle	No Effect	75 mV	Idle
Receive	Transmit	Affects ΔVacf	50–150 mV	Receive
Receive	Idle	Affects ΔVacf	50–150 mV	Receive

As can be seen from the truth table, the Tx-Rx comparator dominates. The Transmit Detector Comparator is effective only in the transmit mode, and the Volume Control is effective only in the receive mode.

The Tx-Rx comparator is in the transmit position when there is sufficient transmit signal present over and above any receive signal. The Transmit Detector Comparator then determines whether the transmit signal is a result of background noise (a relatively stable signal), or speech which consists of bursts. If the signal is due to background noise, the attenuators will be put into the idle mode (ΔVacf = 75 mV). If the signal consists of speech, the attenuators will be switched to the transmit mode (ΔVacf = 6.0 mV.) A further explanation of this function will be found in the section on the Transmit Detector Circuit.

The Tx-Rx comparator is in the receive position when there is sufficient receive signal to overcome the background noise **AND** any speech signals. The ΔVacf voltage will now be 150 mV **IF** the volume control is at the maximum position, i.e. VLC (Pin 24) = VB. IF VLC is less than VB, the gain of the receive attenuator, and the attenuation of the transmit attenuator, will vary in a complementary manner as shown in Figure 5. It can be seen that at the minimum recommended operating level (VLC = 0.55 VB) the gain of the transmit attenuator is actually greater than that of the receive attenuator. The effect of varying VLC is to vary ΔVacf, with a resulting variation in the gains of the attenuators. Figure 6 shows the gain variations with ΔVacf.

The capacitor at ACF (Pin 25) smooths the transition between operating modes. This keeps down any "clicks" in the speaker or transmit signal when the ACF voltage switches.

The gain separation of the two attenuators can be reduced from the typical 45 dB by adding a resistor between Pins 20 (V_{CC}) and 25 (ACF). The effect is a reduction of the maximum ΔVacf voltage in the receive mode, while not affecting ΔVacf in the transmit mode. As an example, adding a 12 kΩ resistor will reduce ΔVacf by approximately 15 mV (to 135 mV), decrease the gain of the receive attenuator by approximately 5.0 dB, and increase the gain of the transmit attenuator by a similar amount. If the circuit requires the receive attenuator gain to be +6.0 dB in the receive mode, RRX must be adjusted (to ≈ 27 k) to re-establish this value. This change will also increase the receive attenuator gain in the transmit mode by a similar amount. The resistor at TLI may also require changing to reset the sensitivity of the transmit level detector.

LOG AMPLIFIERS
(Transmit and Receive Level Detectors)

The log amps monitor the levels of the transmit and receive signals, so as to tell the Tx-Rx comparator which mode should be in effect. The input signals are applied to the amplifiers (at TLI and RLI) through AC coupling capacitors and current limiting resistors. The value of these components determines the sensitivity of the respective amplifiers, and has an effect on the switching times between transmit and receive modes. The feedback elements for the amplifiers are back-to-back diodes which provide a logarithmic gain curve, thus allowing operation over a wide range of signal levels. The outputs of the amplifiers are rectified, having a quick rise time and a slow decay time. The rise time is determined primarily by the external capacitor (at TLO or RLO) and an internal 500 ohm resistor, and is on the order of a fraction of a millisecond. The decay time is determined by the external resistor and capacitor, and is on the order of a fraction of a second. The switching time is not fixed, but depends on the relative values of the transmit and receive signals, as well as these external components. Figure 7 indicates the dc transfer characteristics of the log amps, and Figure 8 indicates the transfer characteristics with respect to an ac input signal. The dc level at TLI, RLI, TLO, and RLO is approximately VB.

The Tx-Rx comparator responds to the voltages at TLO and RLO, which in turn are functions of the currents sourced out of TLI and RLI, respectively. If an offset at the comparator input is desired, e.g., to prevent noise from switching the system, or to give preference to either the transmit or receive channel, this may be achieved by biasing the appropriate input (TLI or RLI). A resistor to ground will cause a DC current to flow out of that input, thus forcing the output of that amplifier to be biased slightly higher than normal. This amplifier then becomes the preferred one in the system operation. Resistor values from 500 k to 10 M ohms are recommended for this purpose.

SPEAKER AMPLIFIER

The speaker amplifier has a fixed gain of 34 dB (50 V/V), and is noninverting. The input impedance is nominally 22 kΩ as long as the output signal is below that required to activate the Peak Limiter. Figure 9 indicates the typical output swing available at SKO (Pin 15). Since the output current capability is 100 mA, the lower curve is limited to a 5.0 volt swing. The output impedance depends on the output signal level and is relatively low as long as the signal level is not near the maximum limits. At 3 volts p-p the output impedance is <0.5 ohms, and at 4.5 volts p-p it is <3 ohms. The output is short circuit protected at approximately 300 mA.

When the amplifier is overdriven, the peak limiter causes a portion of the input signal to be shunted to ground, in order to maintain a constant output level. The effect is that of a gain reduction caused by a reduction of the input impedance (at SKI) to a value not less than 2.0 kΩ.

The capacitor at Pin 17 (AGC) determines the response time of the peak limiter circuit. When a large input signal is applied to SKI, the voltage at AGC (Pin 17) will drop quickly as a current source is applied to the external capacitor. When the large input signal is reduced, the current source is turned off, and an internal 110 kΩ resistor discharges the capacitor so the voltage at AGC can return to its normal value (1.9 Vdc). The capacitor additionally stabilizes the peak limiting feedback loop.

If there is a need to mute the speaker amplifier without disabling the rest of the circuit, this may be accomplished by connecting a resistor from the AGC pin to ground. A 100 kΩ resistor will reduce the gain by 34 dB (0 dB from SKI to SKO), and a 10 k resistor will reduce the gain by almost 50 dB.

TRANSMIT DETECTOR CIRCUIT

The transmit detector circuit, also known as the background noise monitor, distinguishes speech (which consists of bursts) from the background noise (a relatively constant signal). It does this by storing a voltage level, representative of the average background noise, in the capacitor at CP1 (Pin 11). The resistor and capacitor at this pin have a time constant of approximately 5 seconds (in Figure 1). The voltage at Pin 11 is applied to the inverting input of the Transmit Detector Comparator. In the absence of speech signals, the noninverting input receives the same voltage level minus an offset of 36 mV. In this condition, the output of the comparator will be low, the output transistor turned off, and the voltage at XDC (Pin 23) will be at ground. If the Tx-Rx comparator is in the transmit position, the attenuators will be in the idle mode (ΔVacf = 75 mV). When speech is presented to the microphone, the signal burst appearing at XDI reaches the noninverting input of the transmit detector comparator before the voltage at the inverting input can change, causing the output to switch high, driving the voltage at XDC up to approximately 4 volts. This high level causes the attenuator control block to switch the attenuators from the idle mode to the transmit mode (assuming the Tx-Rx comparator is in

the transmit mode). As long as the speech continues to arrive, and is maintained at a level above the background, the voltage at XDC will be maintained at a high level, and the circuit will remain in the transmit mode. The time constant of the components at XDC will determine how much time the circuit requires to return to the idle mode after the cessation of microphone speech signals, such as occurs during the normal pauses in speech.

The series resistor and capacitor at XDI (Pin 13) determine the sensitivity of the transmit detector circuit. Figure 10 indicates the change in DC voltage levels at CP2 and CP1 in response to a steady state sine wave applied at the input of the 0.068 μF capacitor and 4700 ohm resistor (the voltage change at CP1 is 2.7 times greater than the change at CP2). Increasing the resistor, or lowering the capacitor, will reduce the response at these pins. The first amplifier (between XDI and CP2) is logarithmic in order that this circuit be able to handle a wide range of signal levels (or in other words, it responds equally well to people who talk quietly and to people who shout). Figure 7 indicates the dc transfer characteristics of the log amp.

Figure 11 indicates the response at Pins 11, 12, and 23 to a varying signal at the microphone. The series of events in Figure 11 is as follows:

1) CP2 (Pin 12) follows the peaks of the speech signals, and decays at a rate determined by the 10 μA current source and the capacitor at this pin.

2) CP1 (Pin 11) increases at a rate determined by the RC at this pin after CP2 has made a positive transition. It will follow the decay pattern of CP2.

3) The noninverting input of the Transmit Detector Comparator follows CP2, gained up by 2.7, and reduced by an offset of 36 mV. This voltage, compared to CP1, determines the output of the comparator.

4) XDC (Pin 23) will rise quickly to 4 Vdc in response to a positive transition at CP2, but will decay at a rate determined by the RC at this pin. When XDC is above 3.25 Vdc, the circuit will be in the transmit mode. As it decays towards ground, the attenuators are taken to the idle mode.

MICROPHONE AMPLIFIER

The microphone amplifier is noninverting, has an internal gain of 34 dB (50 V/V), and a nominal input impedance of 10 kΩ. The output impedance is typically <15 ohms. The maximum p-p voltage swing available at the output is approximately 2.0 volts less than V_{CC}, which is substantially more than what is required in most applications. The input at MCI (Pin 9) should be ac coupled to the microphone so as to not upset the bias voltage. Generally, microphone sensitivity may be adjusted by varying the 2 k microphone bias resistor, rather than by attempting to vary the gain of the amplifier.

POWER SUPPLY

The voltage supply for the MC34018 at V+ (Pin 16) should be in the range of 6.0 to 11 volts, although the circuit will operate down to 4.0 volts. The voltage can be supplied either from Tip and Ring, or from a separate supply. The required supply current, with no signal to the speaker, is shown in Figure 12. The upper curve indicates the normal operating current when $\overline{\text{Chip Select}}$ (Pin 18) is at a Logic "0". Figure 13 indicates the average dc current required when supplying various power levels to a 25 ohm speaker. Figure 13 also indicates the minimum supply voltage required to provide the indicated power levels. The peak in the power supply current at 5.0–5.4 volts occurs as the V_{CC} circuit comes into regulation.

It is imperative that the V+ supply (Pin 16) be a good ac ground for stability reasons. If this pin is not well filtered (by a 1000 μF capacitor AT THE IC), any variation at V+ caused by the required speaker current flowing through this pin can cause a low frequency oscillation. The result is usually that the circuit will cut the speaker signal on and off at the rate of a few hertz. Experiments have shown that only a few inches of wire between the supply and the IC can cause the problem if the filter capacitor is not physically adjacent to the IC. It is equally imperative that both ground pins (Pins 14 and 22) have a low loss connection to the power supply ground.

V_{CC}

V_{CC} (Pin 20) is a regulated output voltage of 5.4 volts, +/−0.5 V. Regulation will be maintained as long as V+ is (typically) 80 mV greater than the regulated value of V_{CC}. Up to 3 milliamps can be sourced from this supply for external use. The output impedance is <20 ohms.

The 47 μF capacitor indicated for connection to Pin 20 is essential for stability reasons. It must be located adjacent to the IC.

If the circuit is deselected (see section on Chip Select), the V_{CC} voltage will go to 0 volts.

If the MC34018 is to be powered from a regulated supply (not the Tip and Ring lines) of less than 6.5 volts, the configuration of Figure 14 may be used so as to ensure that V_{CC} is regulated. The regulated voltage is applied to both V+ and V_{CC}, with $\overline{CS}$ held at a Logic "1" so as to turn off the internal regulator (the Chip Select function is not available when the circuit is used in this manner). Figure 15 indicates the supply current used by this configuration, with no signal at the speaker. When a signal is sent to the speaker, the curves of Figure 13 apply.

VB

VB is a regulated output voltage with a nominal value of 2.9 volts, +/−0.4 volts. It is derived from V_{CC} and tracks it, holding a value of approximately 54% of V_{CC}. 1.5 milliamps can be sourced from this supply at a typical output impedance of 250 ohms.

The 47 μF capacitor indicated for connection to the VB pin is required for stability reasons, and must be adjacent to the IC.

If the circuit is deselected (see section on Chip Select), the VB voltage will go to 0 volts.

CHIP SELECT

The Chip Select pin (Pin 18) allows the chip to be powered down anytime its functions are not required. A Logic "1" level in the range of 1.6 V to 11 V deselects the chip, and the resulting supply current (at V+) is shown in Figure 12. The input resistance at Pin 18 is >75 kΩ. The V_{CC} and VB regulated voltages go to 0.0 when the chip is deselected. Leaving Pin 18 open is equivalent to a Logic "0" (chip enabled).

FIGURE 1 — TEST CIRCUIT

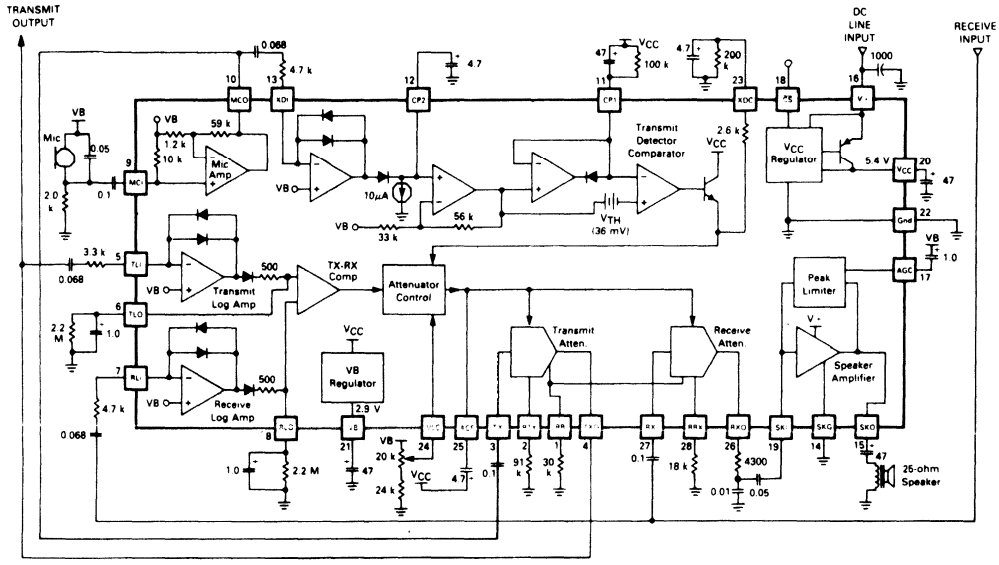


FIGURE 2 — TRANSMIT ATTENUATOR versus RTX

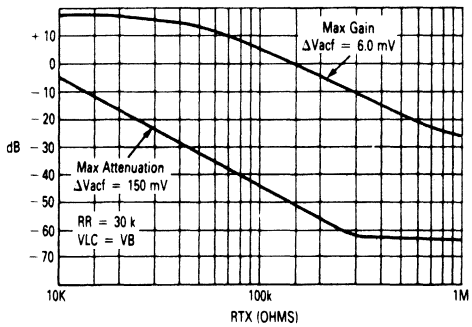


FIGURE 3 — RECEIVE ATTENUATOR versus RRX

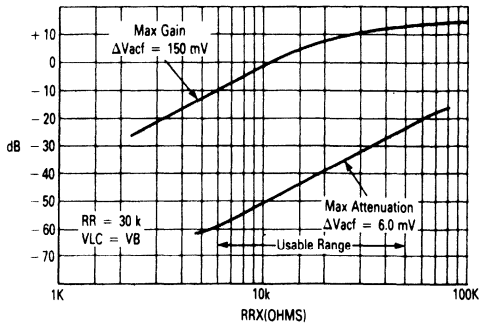


FIGURE 4 — GAIN AND ATTENUATION versus RESISTOR RATIOS

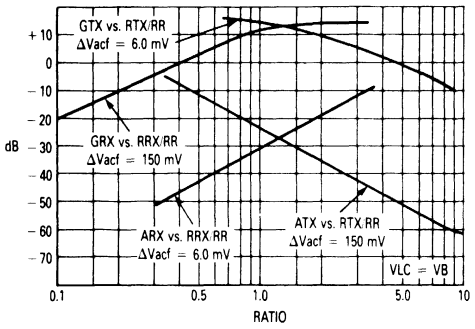


FIGURE 5 — ATTENUATOR GAIN versus VLC

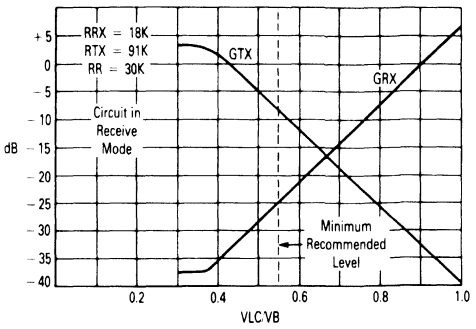


FIGURE 6 — ATTENUATOR GAIN versus ΔVacf

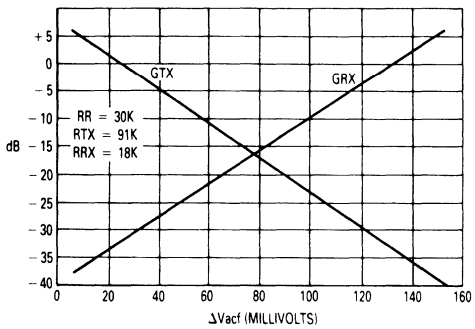


FIGURE 7 — LOG AMP TRANSFER CHARACTERISTICS

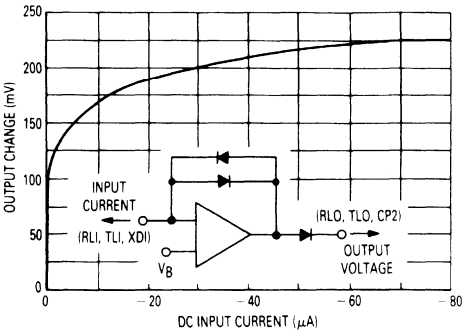


FIGURE 8 — LOG AMP TRANSFER CHARACTERISTICS

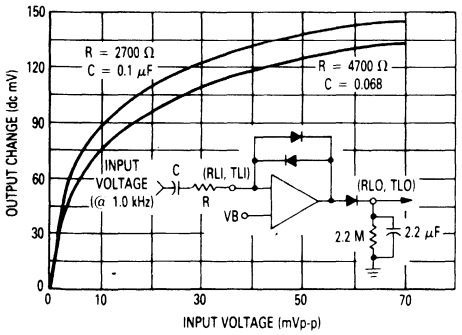


FIGURE 9 — SPEAKER AMP OUTPUT versus SUPPLY VOLTAGE

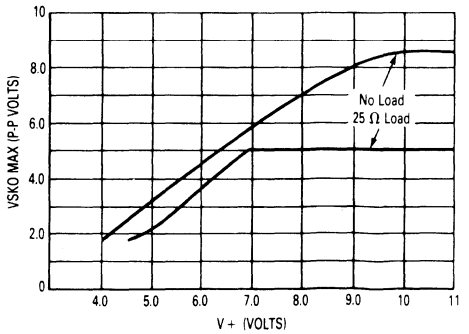


FIGURE 10 — RESPONSE AT CP2 AND CP1

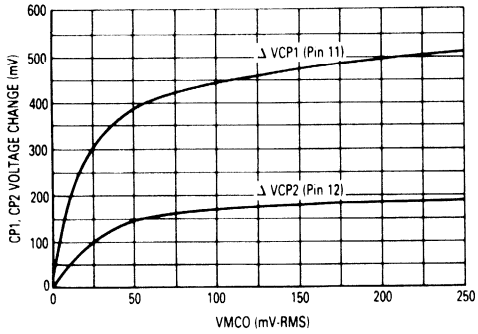


FIGURE 11 — TRANSMIT DETECTOR OPERATION

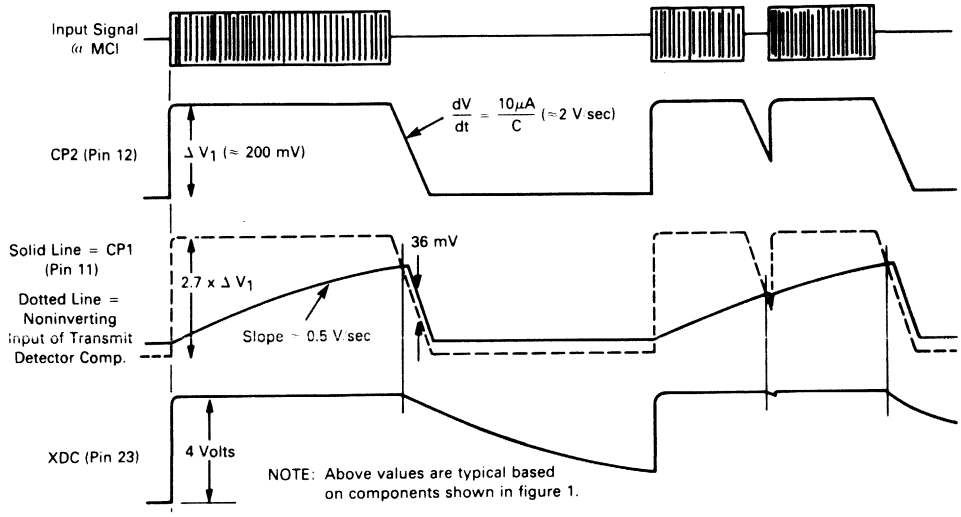


FIGURE 12 — SUPPLY CURRENT versus SUPPLY VOLTAGE

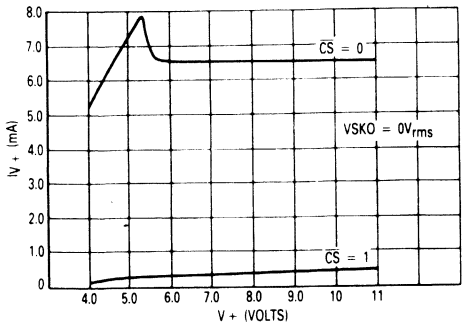


FIGURE 13 — SUPPLY CURRENT versus SUPPLY VOLTAGE versus SPEAKER POWER

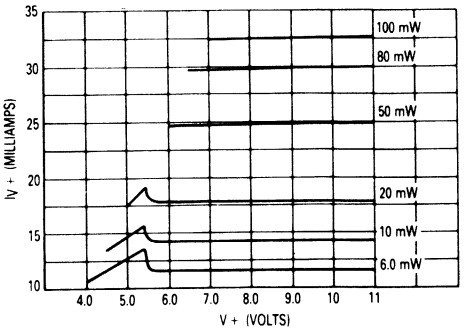


FIGURE 14 — ALTERNATE POWER SUPPLY CONFIGURATION

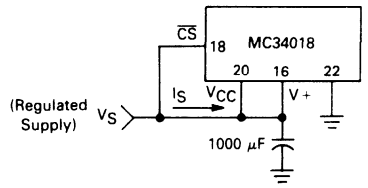
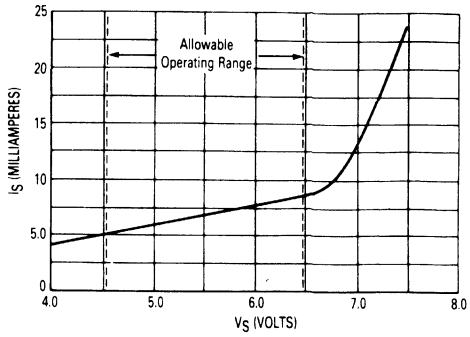


FIGURE 15 — SUPPLY CURRENT versus SUPPLY VOLTAGE (SEE FIGURE 14)



3

SWITCHING TIME

The switching times of the speakerphone circuit depend not only on the various external components, but also on the operating condition of the circuit at the time a change is to take effect. For example, the switching time from idle to transmit is generally quicker than the switching time from receive to transmit (or transmit to receive).

The components which most significantly affect the timing between the transmit and receive modes are those at Pins 5 (transmit turn-on), 6 (transmit turn-off), 7 (receive turn-on), and 8 (receive turn-off). These four timing functions are not independent, but interact since the Tx-Rx comparator operates on a RELATIVE Tx-Rx comparison, rather than on absolute values. The components at Pins 11, 12, 13, and 23 affect the timing from the transmit to the idle mode. Timing from the idle mode to transmit mode is relatively quick (due to the quick charging of the various capacitors), and is not greatly affected by the component values. Pins 5–8 do not affect the idle-to-transmit timing since the Tx-Rx comparator must already be in the transmit mode for this to occur.

The following table provides a summary of the effect on the switching time of the various components, including the volume control:

Additionally, the following should be noted:

1) The RCs at Pins 5 and 7 have a dual function in that they affect the sensitivity of the respective log amplifiers, or in other words, how loud the speech must be in order to gain control of the speakerphone circuit.

2) The RC at Pin 13 also has a dual function in that it determines the sensitivity of the transmit detector circuit.

3) The volume control affects the switching speed, and the relative response to transmit signals, in the following manner: When the circuit is in the receive mode, reducing the volume control setting increases the signal at TXO, and consequently the signal to the TLI pin. Therefore a given signal at TXI will switch the circuit into the transmit mode quicker at low volume settings.

The photographs of Figures 16 and 17 indicate experimentally obtained switching response times for the circuit of Figure 1. In Figure 16, the circuit is provided a continuous receive signal of 1.1 mVp-p at RXI (trace #3). A repetitive burst signal of 7.2 mVp-p, lasting 120

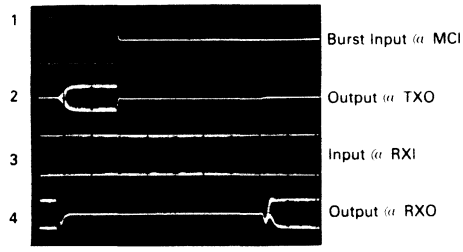
Components	Tx to Rx	Rx to Tx	Tx to Idle
RC @ Pin 5	Moderate	Significant	No effect
RC @ Pin 6	Significant	Moderate	No effect
RC @ Pin 7	Significant	Moderate	No effect
RC @ Pin 8	Moderate	Significant	No effect
RC @ Pin 11	No effect	Slight	Moderate
C @ Pin 12	No effect	Slight	Significant
RC @ Pin 13	No effect	Slight	Slight
RC @ Pin 23	No effect	Slight	Significant
V @ Pin 24	No effect	Moderate	No effect
C @ Pin 25	Moderate	Moderate	Slight

milliseconds, and repeated every 1 second, is applied to MCI (Trace #1). Trace #2 is the output at TXO, and is approximately 650 mVp-p at its maximum. Trace #4 is the output at RXO, and is approximately 2.2 mVp-p at its maximum. The time to switch from the receive mode to the transmit mode is approximately 40 ms, as indicated by the time required for TXO to turn on, and for RXO to turn off. After the signal at MCI is shut off, the switching time back to the receive mode is approximately 210 ms.

In Figure 17, a continuous signal of 7.6 mVp-p is applied to MCI (Trace #1), and a repetitive burst signal of 100 mVp-p is applied to RXI (Trace #3), lasting approximately 120 ms, and repeated every 1 second. Trace #2 is the output at TXO and is approximately 90 mVp-p at its maximum, and Trace #4 indicates the output at RXO, and is approximately 150 mVp-p at its maximum. In this sequence, the circuit switches between the idle and receive modes. The time required to switch from idle to receive is approximately 70 ms, as indicated by the first part of Traces 2 and 4. After the receive signal is shut off, the time to switch back to the idle mode is approximately 100 ms.

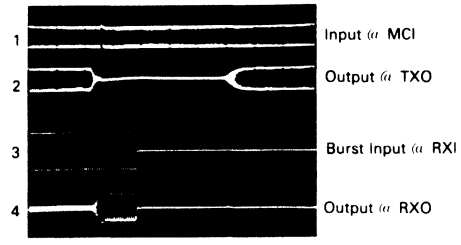
All of the above mentioned times will change significantly by varying the amplitude of the input signals, as well as by varying the external components.

FIGURE 16 — TRANSMIT-RECEIVE SWITCHING



Time Base = 40 ms/Div

FIGURE 17 — IDLE-RECEIVE SWITCHING



Time Base = 30 ms/Div

APPLICATIONS INFORMATION

The MC34018 Speakerphone IC is designed to provide the functions additionally required when a speakerphone is added to a standard telephone. The IC provides the necessary relative level detection and comparison of the speech signals provided by the talkers at the speakerphone (near end speaker) and at the distant telephone (far end speaker).

The MC34018 is designed for use with an electret type microphone, a 25 ohm speaker, and has an output power capability of (typically) 100 mW. All external components surrounding this device are passive, however, this IC does require additional circuitry to interface to the Tip and Ring telephone lines. Two suggested circuits are shown in this data sheet.

Figure 18 depicts a circuit using the MC34014 Speech Network (to provide the line interface), as well as the circuitry necessary to switch between the handset mode and the speakerphone mode. Switch HS (containing one normally open and one normally closed contact) is the hook switch actuated by the handset, shown in the on-hook position. When the handset is off-hook (HS1 open, HS2 closed), power is applied to the MC34014 speech network, and consequently the handset, and the $\overline{CS}$ pin of the MC34018 is held high so as to disable it. Upon closing the two poles of switch SS, **AND** placing switch HS in the on-hook position, power is then applied to both the MC34014 and the MC34018, and $\overline{CS}$ is held low, enabling the speakerphone function. Anytime the handset is removed from switch HS, the circuit reverts to the handset mode. The diode circuitry sets the operational mode of the MC34014 so as to optimize the speakerphone operation (see the MC34014 data sheet for further details). The tone dialer interface is meant for connection to a DTMF dialer with an active low MUTE signal. The V_{DD} supply from the MC34014 is a nominal 3.3 volts. The MC34017 and piezo sounder provide the ringing function.

Figure 19 depicts a configuration which does not include a handset, dialer, or ringer. The only controls are S1 (to make the connection to the line), S2 (a "privacy" switch), and the volume control. It is meant to be used in parallel with a normal telephone which has the dialing and ringing functions.

Figure 20 depicts a means of providing logic level signals that indicate which mode of operation the MC34018 is in. Comparator A indicates whether the circuit is in the receive or transmit/idle mode, and comparator B indicates (when in the transmit/idle mode) whether the circuit is in the transmit or idle mode. The LM393 dual comparator was chosen because of its low current requirement (<1.0 mA), low voltage requirement (as low as 2.0 volts), and low cost.

3

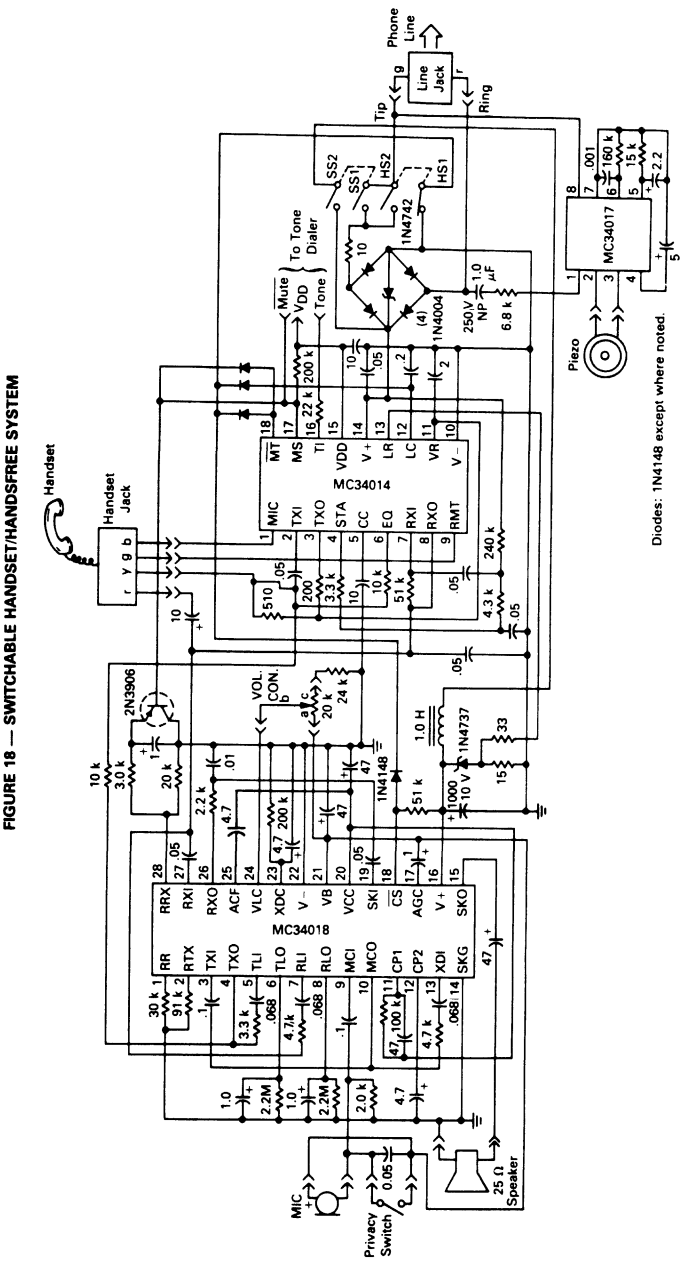
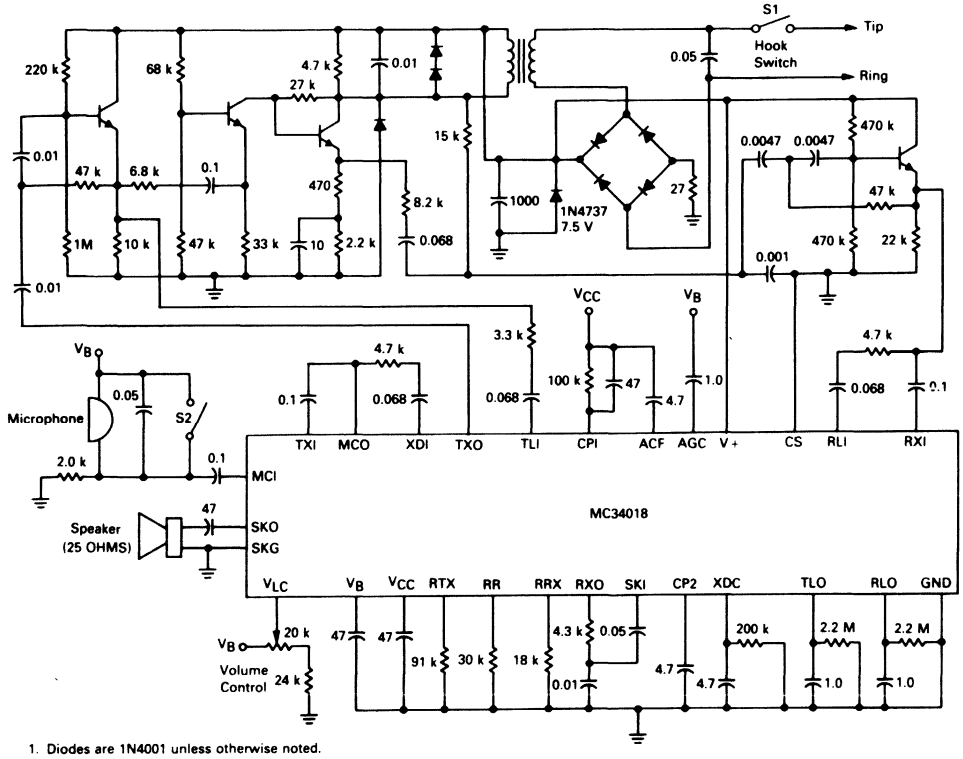


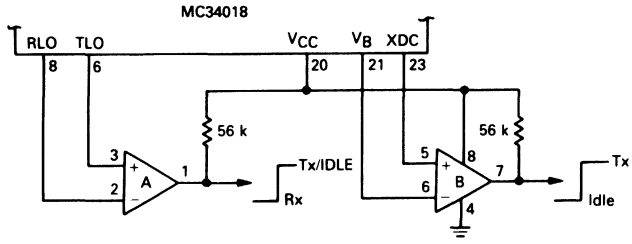
FIGURE 18 — SWITCHABLE HANDSET/HANDSFREE SYSTEM

FIGURE 19 — BASIC LINE POWERED SPEAKERPHONE



1. Diodes are 1N4001 unless otherwise noted.
2. 4 Transistors are 2N3904.
3. Recommended Transformer: Microtran T2106.

FIGURE 20 — DIGITAL TRANSMIT/IDLE/RECEIVE INDICATION



Comparators A & B = LM393 (Dual)

MOTOROLA

MC34114
MC34214

Product Preview

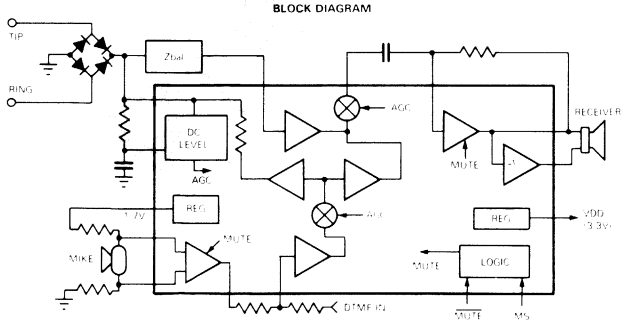
TELEPHONE SPEECH NETWORK WITH DIALER INTERFACE

The MC34114/214 is a monolithic integrated telephone speech network designed to replace the bulky magnetic hybrid circuit of a telephone set. The MC34114/214 incorporates the necessary functions of transmit amplification, receive amplification, and sidetone control, each with externally adjustable gain. Loop length equalization varies the gains based on loop current. The microphone amplifier has a balanced, differential input stage designed to reduce RFI problems. A $\overline{\text{MUTE}}$ input mutes the microphone and receive amplifiers during dialing. A regulated output voltage is provided for biasing the microphone, and a separate output voltage powers an external dialer. The MC34114/214 is designed for operation with a supply voltage as low as 1.2 volts, making party line operation possible. A MODE SELECT input sets the circuit for Pulse or tone use.

The MC34114 complies with Bell Telephone and British Telecom (BT) standards. The MC34214 complies with Nippon Telegraph and Telephone (NTT) standards. Both parts are available in a standard 18 pin DIP, and a 20 pin SOIC (surface mount) package.

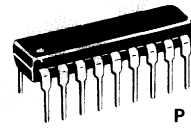
- Operation down to 1.2 volts.
- Externally adjustable transmit, receive, and sidetone gains.
- Differential Microphone amplifier input minimizes RFI.
- Transmit, receive, and sidetone equalization on both voice and DTMF signals.
- Regulated 1.7 volts output for biasing microphone.
- Regulated 3.3 volts output for powering external dialer.
- Microphone and receive amplifiers muted during dialing.
- Differential receive amplifier output eliminates coupling capacitor.
- Operates with receiver impedances of 150 ohms and higher.
- MC34114 complies with Bell Telephone and BT standards.
- MC34214 complies with NTT standards.

BLOCK DIAGRAM

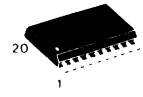


TELEPHONE SPEECH NETWORK WITH DIALER INTERFACE

SILICON MONOLOTHIC INTEGRATED CIRCUIT



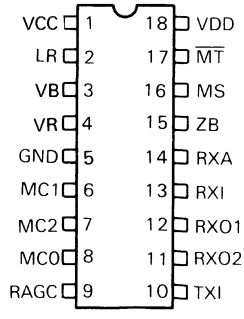
P SUFFIX
PLASTIC PACKAGE
CASE 707-02



DW SUFFIX
PLASTIC PACKAGE
CASE 751D-02

PIN ASSIGNMENT

(Top View)
(DIP Package)



ORDERING INFORMATION

STANDARDS	PKG.	PART NO.
Bell Tel. & BT	DIP	MC34114P
Bell Tel. & BT	SOIC	MC34114DW
NTT	DIP	MC34214P
NTT	SOIC	MC34214DW

MOTOROLA

MC34115

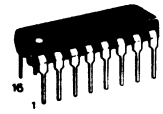
Specifications and Applications Information

CONTINUOUSLY VARIABLE SLOPE DELTA MODULATOR/DEMODULATOR

CONTINUOUSLY VARIABLE SLOPE DELTA MODULATOR/DEMODULATOR

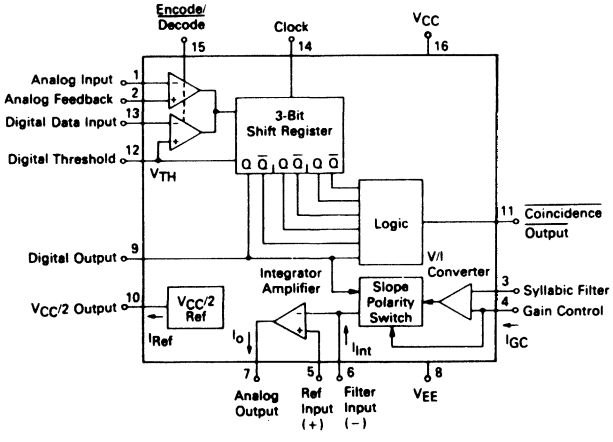
Providing a simplified approach to digital speech encoding/decoding, the MC34115 CVSD is designed for speech synthesis and commercial telephone applications. A single IC provides both encoding and decoding functions.

- Encode and Decode Functions Selectable with a Digital Input
- Utilization of Compatible I^2L — Linear Bipolar Technology
- CMOS Compatible Digital Output
- Digital Input Threshold Selectable ($V_{CC}/2$ reference provided on chip)
- 3-Bit Algorithm

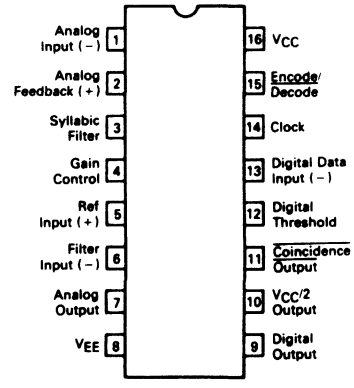


P SUFFIX
PLASTIC PACKAGE
CASE 648-05

CVSD BLOCK DIAGRAM



PIN CONNECTIONS



DS9667

MAXIMUM RATINGS

(All voltages referenced to V_{EE}, T_A = 25°C unless otherwise noted.) (See Note 2.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.4 to +18	Vdc
Differential Analog Input Voltage	V_{ID}	±5.0	Vdc
Digital Threshold Voltage	V_{TH}	−0.4 to V_{CC}	Vdc
Logic Input Voltage (Clock, Digital Data, Encode/$\overline{\text{Decode}}$)	V_{Logic}	−0.4 to +18	Vdc
Coincidence Output Voltage	$V_{O(Con)}$	−0.4 to +18	Vdc
Syllabic Filter Input Voltage	$V_{I(Syl)}$	−0.4 to V_{CC}	Vdc
Gain Control Input Voltage	$V_{I(GC)}$	−0.4 to V_{CC}	Vdc
Reference Input Voltage	$V_{I(Ref)}$	$V_{CC}/2$ − 1.0 to V_{CC}	Vdc
$V_{CC}/2$ Output Current	I_{Ref}	−25	mA
Operating Ambient Temperature Range	T_A	0 to +70	°C
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 12 V, V_{EE} = Gnd, T_A = 0°C to + 70°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage Range (Figure 1)	V_{CC}	4.75	12	16.5	Vdc
Power Supply Current (Figure 1) (Idle Channel)	I_{CC}				mA
V_{CC} = 5.0 V		—	4.6	7.5	
V_{CC} = 15 V		—	7.0	12	
Clock Rate	SR	—	16 k	—	Samples/s
Gain Control Current Range (Figure 2)	I_{GCR}	0.002	—	3.0	mA
Analog Comparator Input Range (Pins 1 and 2) 4.75 V ≤ V_{CC} ≤ 16.5 V	V_I	1.3	—	V_{CC} − 1.3	Vdc
Analog Output Range (Pin 7) 4.75 V ≤ V_{CC} ≤ 16.5 V, I_O = ±5.0 mA	V_O	1.3	—	V_{CC} − 1.3	Vdc
Input Bias Currents (Figure 3)	I_{IB}				μA
Comparator in Active Region					
Analog Input (I1)		—	0.5	2.5	
Analog Feedback (I2)		—	0.5	2.5	
Syllabic Filter Input (I3)		—	0.06	0.5	
Reference Input (I5)		—	−0.06	−0.5	
Input Offset Current	I_{IO}				μA
Comparator in Active Region					
Analog Input/Analog Feedback |I1−I2| — Figure 3		—	0.15	0.8	
Integrator Amplifier |I5−I6| — Figure 4		—	0.02	0.2	
Input Offset Voltage V/I Converter (Pins 3 and 4) — Figure 5	V_{IO}	—	2.0	10	mV
Transconductance	gm				mA/mV
V/I Converter, 0 to 3.0 mA		0.1	0.3	—	
Integrator Amplifier, 0 to +5.0 mA Load		1.0	10	—	
Propagation Delay Times (Note 1)					μs
Clock Trigger to Digital Output	t_{PLH}	—	1.0	3.0	
C_L = 25 pF to Gnd	t_{PHL}	—	0.8	3.0	
Clock Trigger to Coincidence Output	t_{PLH}	—	1.0	3.5	
C_L = 25 pF to Gnd	t_{PHL}	—	0.8	2.5	
R_L = 4.0 kΩ to V_{CC}					

NOTES 1. All propagation delay times measured 50% to 50% from the negative going (from V_{CC} to +0.4 V) edge of the clock.
2. Devices should not be operated at these values. The "Electrical Characteristics" provide conditions for actual device operation.

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Coincidence Output Voltage — Low Logic State $I_{OL(Con)}$ = 3.0 mA	$V_{OL(Con)}$	—	0.12	0.25	Vdc
Coincidence Output Leakage Current — High Logic State V_{OH} = 15 V	$I_{OH(Con)}$	—	0.01	0.5	μA
Applied Digital Threshold Voltage Range (Pin 12)	V_{TH}	+1.2	—	V_{CC} −2.0	Vdc
Digital Threshold Input Current 1.2 V ≤ V_{th} ≤ V_{CC} − 2.0 V	$I_{I(th)}$				μA
V_{IL} applied to Pins 13, 14 and 15		—	—	5.0	
V_{IH} applied to Pins 13, 14 and 15		—	−10	−50	
Maximum Integrator Amplifier Output Current	I_O	±5.0	—	—	mA
V_{CC}/2 Generator Maximum Output Current (Source only)	I_{Ref}	+10	—	—	mA
V_{CC}/2 Generator Output Impedance 0 to +10 mA	z_{Ref}	—	3.0	6.0	Ω
V_{CC}/2 Generator Tolerance 4.75 V ≤ V_{CC} ≤ 16.5 V	ϵ_r	—	—	±3.5	%
Logic Input Voltage (Pins 13, 14 and 15)					Vdc
Low Logic State	V_{IL}	Gnd	—	V_{th} −0.4	
High Logic State	V_{IH}	V_{th} +0.4	—	16.5	
Dynamic Total Loop Offset Voltage (Note 3) — Figures 3, 4 and 5	ΣV_{offset}				mV
I_{GC} = 33 μA, V_{CC} = 12 V					
T_A = 25°C		—	±2.5	±7.0	
0°C ≤ T_A ≤ +70°C		—	±3.0	±10	
I_{GC} = 33 μA, V_{CC} = 5.0 V					
T_A = 25°C		—	±4.0	±8.0	
0°C ≤ T_A ≤ +70°C		—	±4.5	±12	
Digital Output Voltage (Pin 9)					Vdc
I_{OL} = 3.6 mA	V_{OL}	—	0.1	0.4	
I_{OH} = −0.35 mA	V_{OH}	V_{CC} −1.0	V_{CC} −0.2	—	
Syllabic Filter Applied Voltage (Pin 3)	$V_{I(Syl)}$	+3.2	—	V_{CC}	Vdc
Integrating Current (Figure 2)	$\lvert I_{Int} \rvert$				
I_{GC} = 12 μA		8.0	10	12	μA
I_{GC} = 1.5 mA		1.4	1.5	1.6	mA
I_{GC} = 3.0 mA		2.75	3.0	3.25	mA
Dynamic Integrating Current Match (Figure 6) I_{GC} = 1.5 mA	$V_{O(Ave)}$	—	±100	±300	mV
Input Current — High Logic State	I_{IH}				μA
V_{IH} = 16.5 V					
Digital Data Input		—	—	+5.0	
Clock Input		—	—	+5.0	
Encode/$\overline{\text{Decode}}$ Input		—	—	+5.0	
Input Current — Low Logic State	I_{IL}				μA
V_{IL} = 0 V					
Digital Data Input		—	—	−10	
Clock Input		—	—	−360	
Encode/$\overline{\text{Decode}}$ Input		—	—	−36	
Clock Input, V_{IL} = 0.4 V		—	—	−72	

NOTE 3. Dynamic total loop offset (ΣV_{offset}) equals V_{IO} (comparator) (Figure 3) minus V_{IOX} (Figure 5). The input offset voltages of the analog comparator and of the integrator amplifier include the effects of input offset current through the input resistors. The slope polarity switch current mismatch appears as an average voltage across the 10 k integrator resistor. The clock frequency is 16 kHz. Idle channel performance is guaranteed if this dynamic total loop offset is less than one-half of the change in integrator output voltage during one clock cycle (ramp step size).

DEFINITIONS AND FUNCTION OF PINS

Pin 1 — Analog Input

This is the analog comparator inverting input where the voice signal is applied. It may be ac or dc coupled depending on the application. If the voice signal is to be level shifted to the internal reference voltage, then a bias resistor between Pins 1 and 10 is used. The resistor is used to establish the reference as the new dc average of the ac coupled signal. The analog comparator was designed for low hysteresis (typically less than 0.1 mV) and high gain (typically 70 dB).

Pin 2 — Analog Feedback

This is the non-inverting input to the analog signal comparator within the IC. In an encoder application it should be connected to the analog output of the encoder circuit. This may be Pin 7 or a low pass filter output connected to Pin 7. In a decode circuit Pin 2 is not used and may be tied to V_{CC} 2 on Pin 10, ground or left open.

The analog input comparator has bias currents of 2.5 μA max, thus the driving impedances of Pins 1 and 2 should be equal to avoid disturbing the idle channel characteristics of the encoder.

Pin 3 — Syllabic Filter

This is the point at which the syllabic filter voltage is returned to the IC in order to control the integrator step size. It is an NPN input to an op amp. The syllabic filter consists of an RC network between Pins 11 and 3. Typical time constant values of 6 ms to 50 ms are used in voice codecs.

Pin 4 — Gain Control Input

The syllabic filter voltage appears across C_S of the syllabic filter and is the voltage between V_{CC} and Pin 3. The active voltage to current (V–I) converter drives Pin 4 to the same voltage at a slew rate of typically 0.5 V/μs. Thus the current injected into Pin 4 (I_{GC}) is the syllabic filter voltage divided by the R_X resistance. Figure 7 shows the relationship between I_{GC} (x-axis) and the integrating current, I_{Int} (y-axis). The discrepancy, which is most significant at very low currents, is due to circuitry within the slope polarity switch which enables trimming to a low total loop offset. The R_X resistor is then varied to adjust the loop gain of the codec, but should be no larger than 5.0 kΩ to maintain stability.

Pin 5 — Reference Input

This pin is the non-inverting input of the integrator amplifier. It is used to reference the dc level of the output signal. In an encoder circuit it must reference the same voltage as Pin 1 and is tied to Pin 10.

Pin 6 — Filter Input

This inverting op amp input is used to connect the integrator external components. The integrating current (I_{Int}) flows into Pin 6 when the analog input (Pin 1) is high with respect to the analog feedback (Pin 2) in the encode mode or when the digital data input (Pin 13) is high in the decode mode. For the opposite states, I_{Int} flows out of Pin 6. Single integration systems require a capacitor and resistor between Pins 6 and 7. Multipole configurations will have different circuitry. The resistance between Pins 6 and 7 should typically be between 8 kΩ and 13 kΩ to maintain good idle channel characteristics.

Pin 7 — Analog Output

This is the integrator op amp output. It is capable of driving a 600-ohm load referenced to $V_{CC}/2$ to +6 dBm and can otherwise be treated as an op amp output. Pins 5, 6, and 7 provide full access to the integrator op amp for designing integration filter networks. The slew rate of the internally compensated integrator op amp is typically 0.5 V/μs. Pin 7 output is current limited for both polarities of current flow at typically 30 mA.

Pin 8 — V_{EE}

The circuit is designed to work in either single or dual power supply applications. Pin 8 is always connected to the most negative supply.

Pin 9 — Digital Output

The digital output provides the results of the delta modulator's conversion. It swings between V_{CC} and V_{EE} and is CMOS or TTL compatible. Pin 9 is inverting with respect to Pin 1 and non-inverting with respect to Pin 2. It is clocked on the falling edge of Pin 14. The typical 10% to 90% rise and fall times are 250 ns and 50 ns respectively for V_{CC} = 12 V and C_L = 25 pF to ground.

Pin 10 — $V_{CC}/2$ Output

An internal low impedance mid-supply reference is provided for use of the MC34115 in single supply applications. The internal regulator is a current source and must be loaded with a resistor to insure its sinking capability. If a +6 dBmo signal is expected across a 600 ohm input bias resistor, then Pin 10 must sink 2.2 V/600 Ω = 3.66 mA. This is only possible if Pin 10 sources 3.66 mA into a resistor normally and will source only the difference under peak load. The reference load resistor is chosen accordingly. A 0.1 μF bypass capacitor from Pin 10 to V_{EE} is also recommended. The $V_{CC}/2$ reference is capable of sourcing 10 mA and can be used as a reference elsewhere in the system circuitry.

Pin 11 — $\overline{\text{Coincidence Output}}$

The coincidence output will be low whenever the content of the internal 3 bit shift register is all 1s or all 0s. Pin 11 is an open collector of an NPN device and requires a pull-up resistor. If the syllabic filter is to have equal charge and discharge time constants, the value of R_P should be much less than R_S. In systems requiring different charge and discharge constants, the charging

DEFINITIONS AND FUNCTION OF PINS (continued)

constant is $R_S C_S$ while the decaying constant is $(R_S + R_P)C_S$. Thus longer decays are easily achievable. The NPN device should not be required to sink more than 3 mA. The typical 10% to 90% rise and fall times are 200 ns and 100 ns respectively for R_L = 4 kΩ to +12 V and C_L = 25 pF to ground.

Pin 12 — Digital Threshold

This input sets the switching threshold for Pins 13, 14, and 15. It is intended to aid in interfacing different logic families without external parts. Typically it is connected to the $V_{CC}/2$ reference for CMOS interface or can be biased two diode drops above V_{EE} for TTL interface.

Pin 13 — Digital Data Input

In a decode application, the digital data stream is applied to Pin 13. In an encoder it may be unused or may be used to transmit signaling message under the control of Pin 15. It is an inverting input with respect to Pin 9. When Pins 9 and 13 are connected, a toggle flip-flop is formed and a forced idle channel pattern can be transmitted. The digital data input level should be maintained for 0.5 μs before and after the clock trigger for proper clocking.

Pin 14 — Clock Input

The clock input determines the data rate of the codec circuit. A 16K bit rate requires a 16 kHz clock. The switching threshold of the clock input is set by Pin 12. The shift register circuit toggles on the falling edge of the clock input. The minimum width for a positive-going pulse on the clock input is 300 ns, whereas for a negative-going pulse, it is 900 ns.

Pin 15 — Encode/$\overline{\text{Decode}}$

This pin controls the connection of the analog input comparator and the digital input comparator to the internal shift register. If high, the result of the analog comparison will be clocked into the register on the falling edge at Pin 14. If low, the digital input state will be entered. This allows use of the IC as an encoder/decoder or simplex codec without external parts. Furthermore, it allows non-voice patterns to be forced onto the transmission line through Pin 13 in an encoder.

Pin 16 — V_{CC}

The power supply range is from 4.75 to 16.5 volts between pin V_{CC} and V_{EE}.

3

FIGURE 1 — POWER SUPPLY CURRENT

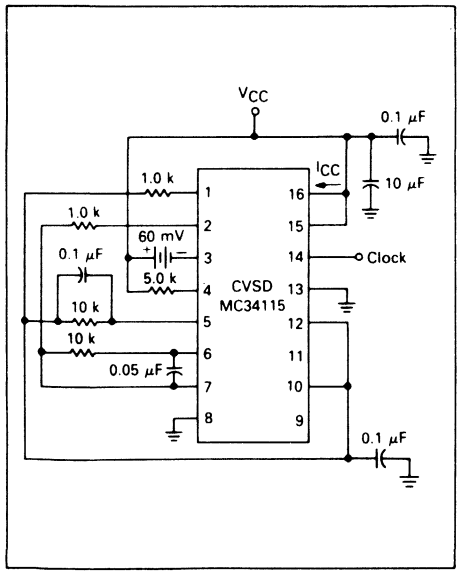
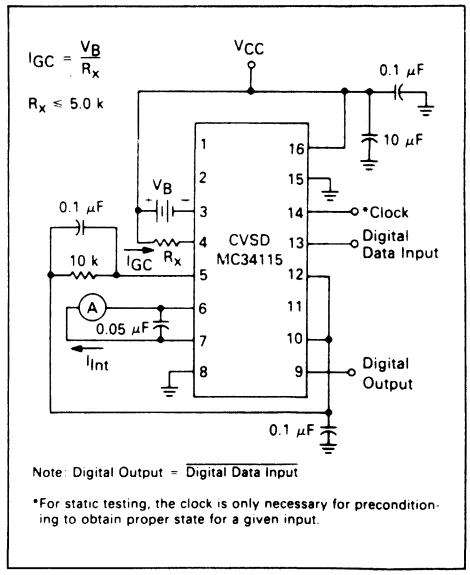


FIGURE 2 — I_{GCR}, GAIN CONTROL RANGE and I_{Int} — INTEGRATING CURRENT

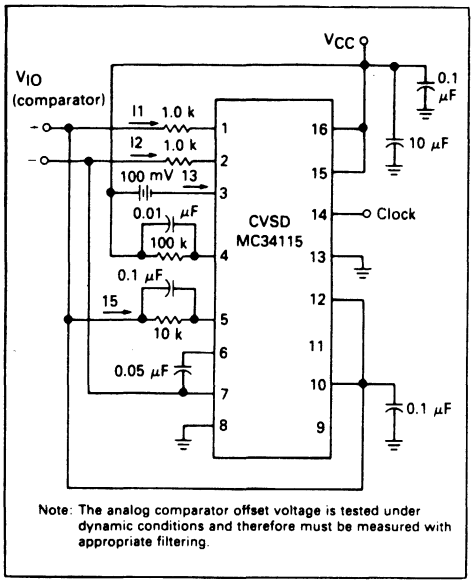


Note: Digital Output = $\overline{\text{Digital Data Input}}$

*For static testing, the clock is only necessary for preconditioning to obtain proper state for a given input.

3

FIGURE 3 — INPUT BIAS CURRENTS, ANALOG COMPARATOR OFFSET VOLTAGE AND CURRENT



Note: The analog comparator offset voltage is tested under dynamic conditions and therefore must be measured with appropriate filtering.

FIGURE 4 — INTEGRATOR AMPLIFIER OFFSET VOLTAGE AND CURRENT

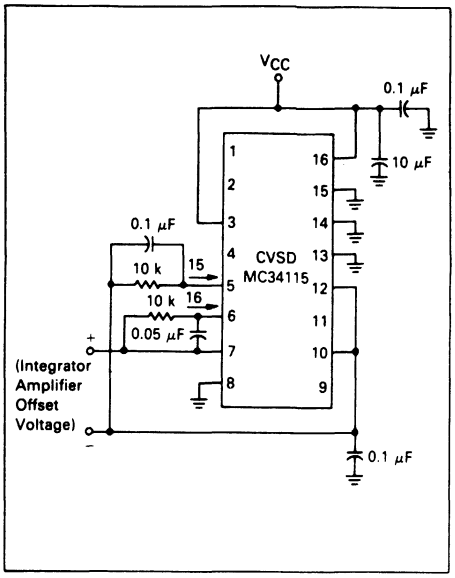
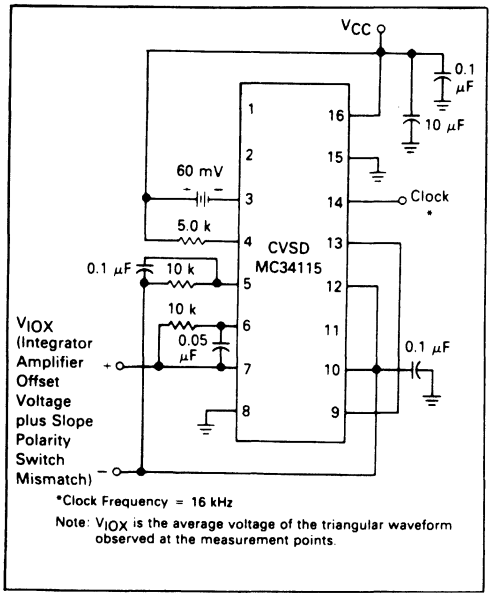


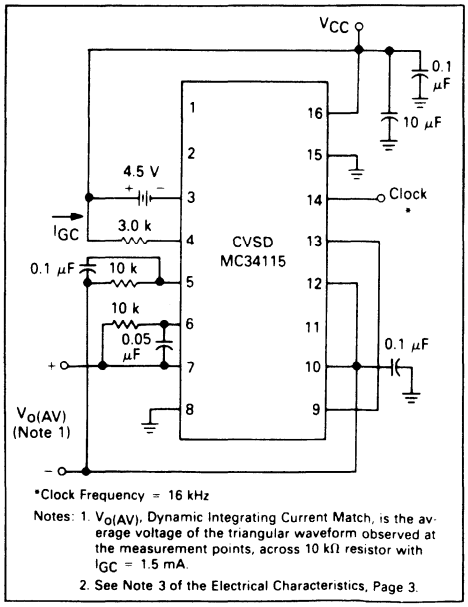
FIGURE 5 — V/I CONVERTER OFFSET VOLTAGE, V_{IO} and V_{IOX}



*Clock Frequency = 16 kHz

Note: V_{IOX} is the average voltage of the triangular waveform observed at the measurement points.

FIGURE 6 — DYNAMIC INTEGRATING CURRENT MATCH



*Clock Frequency = 16 kHz

Notes: 1. $V_{O(AV)}$, Dynamic Integrating Current Match, is the average voltage of the triangular waveform observed at the measurement points, across 10 kΩ resistor with I_{GC} = 1.5 mA.

2. See Note 3 of the Electrical Characteristics, Page 3.

TYPICAL PERFORMANCE CURVES

FIGURE 7 — TYPICAL I_{Int} versus I_{GC} (Mean ± 2σ)

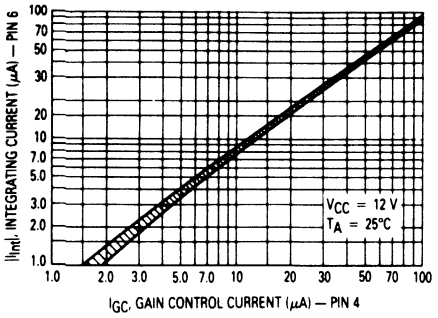
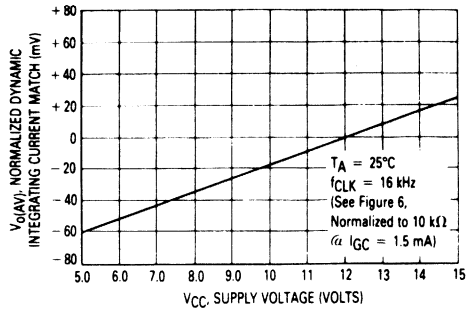


FIGURE 8 — NORMALIZED DYNAMIC INTEGRATING CURRENT MATCH versus V_{CC}



3

FIGURE 9 — NORMALIZED DYNAMIC INTEGRATING CURRENT MATCH versus CLOCK FREQUENCY

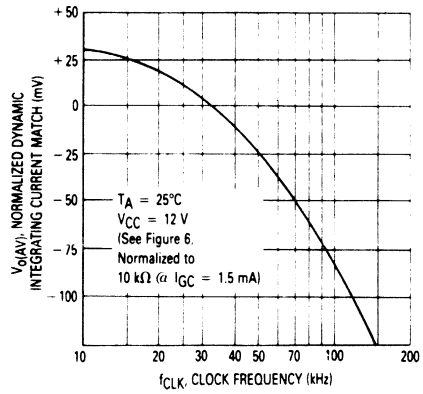


FIGURE 10 — DYNAMIC TOTAL LOOP OFFSET versus CLOCK FREQUENCY

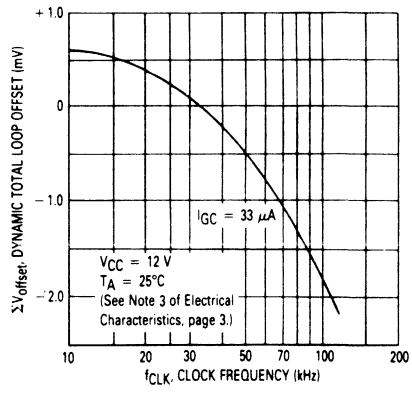


FIGURE 11 — BLOCK DIAGRAM OF THE CVSD ENCODER

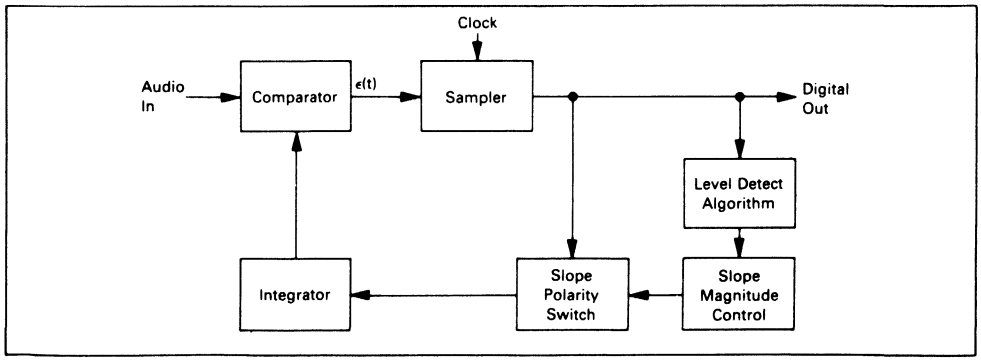


FIGURE 12 — CVSD WAVEFORMS

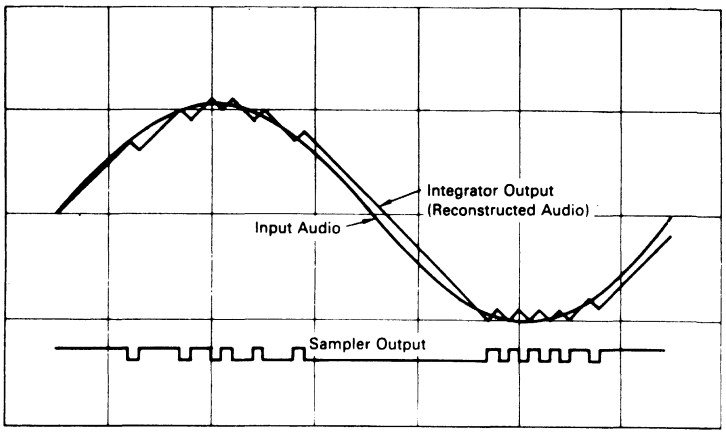
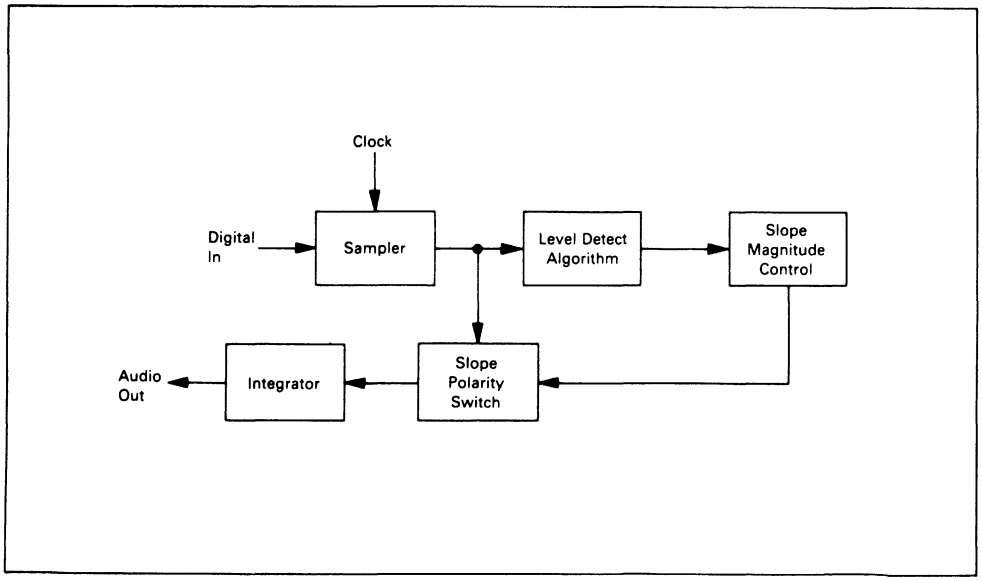
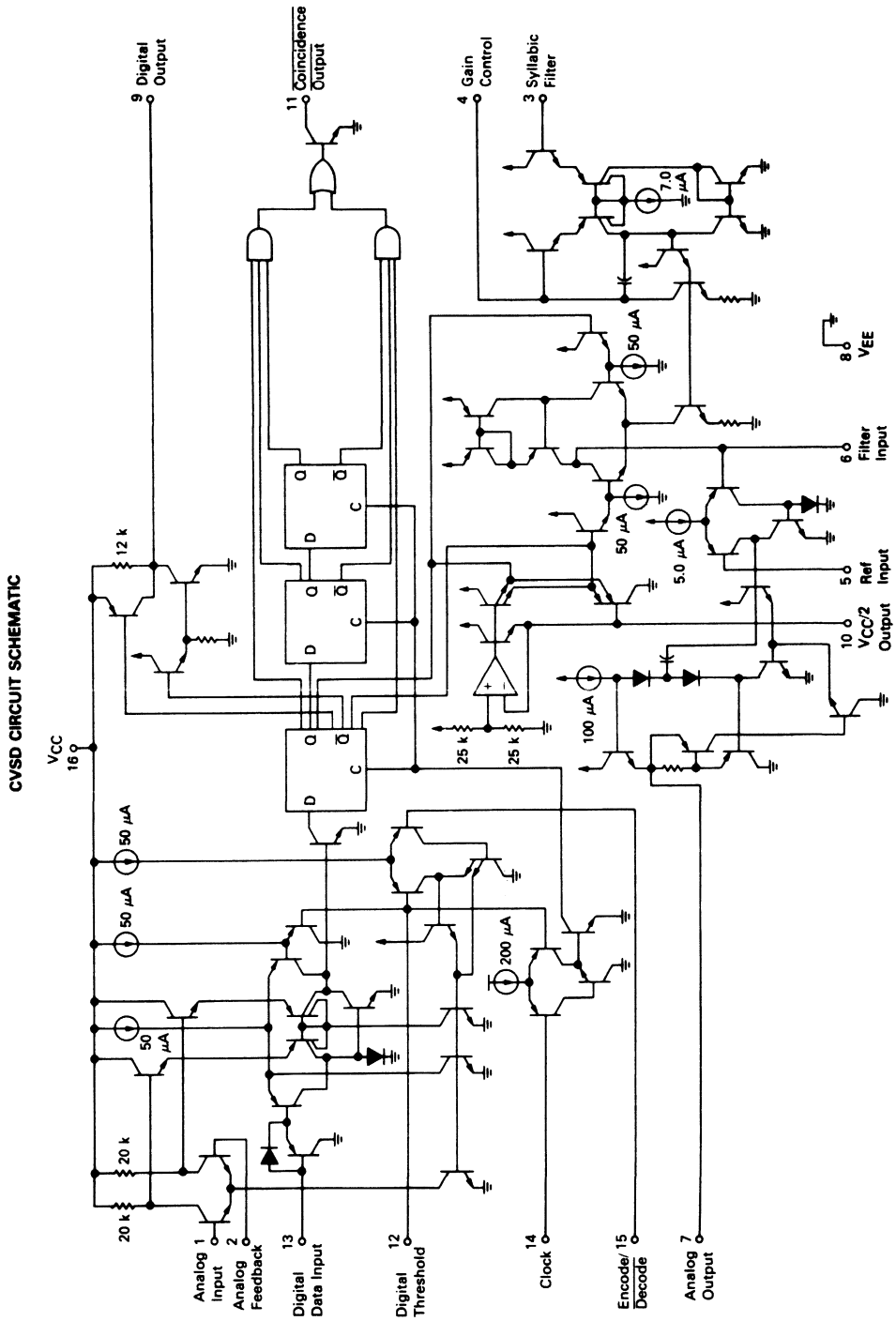


FIGURE 13 — BLOCK DIAGRAM OF THE CVSD DECODER




CVSD CIRCUIT SCHEMATIC
VCC
16
9 Digital Output
11 Coincidence Output
4 Gain Control
3 Syllabic Filter
8 VEE
6 Filter Input
5 Ref Input
10 VCC/2 Output
12 k
20 k
20 k
50 µA
50 µA
50 µA
200 µA
100 µA
25 k
25 k
5.0 µA
7.0 µA
Analog Input 1
Analog Feedback 2
Digital Data Input 13
Digital Threshold 12
Clock 14
Encode/Decode 15
Analog Output 7

CIRCUIT DESCRIPTION

The continuously variable slope delta modulator (CVSD) is a simple alternative to more complex conventional conversion techniques in systems requiring digital communication of analog signals. The human voice is analog, but digital transmission of any signal over great distance is attractive. Signal/noise ratios do not vary with distance in digital transmission and multiplexing, switching and repeating hardware is more economical and easier to design. However, instrumentation A to D converters do not meet the communications requirements. The CVSD A to D is well suited to the requirements of digital communications and is an economically efficient means of digitizing analog inputs for transmission.

The Delta Modulator

The innermost control loop of a CVSD converter is a simple delta modulator. A block diagram CVSD Encoder is shown in Figure 11. A delta modulator consists of a comparator in the forward path and an integrator in the feedback path of a simple control loop. The inputs to the comparator are the input analog signal and the intregrator output. The comparator output reflects the sign of the difference between the input voltage and the integrator output. That sign bit is the digital output and also controls the direction of ramp in the integrator. The comparator is normally clocked so as to produce a synchronous and band limited digital bit stream.

If the clocked serial bit stream is transmitted, received, and delivered to a similar integrator at a remote point, the remote integrator output is a copy of the transmitting control loop integrator output. To the extent that the integrator at the transmitting locations tracks the input signal, the remote receiver reproduces the input signal. Low pass filtering at the receiver output will eliminate most of the quantizing noise, if the clock rate of the bit stream is an octave or more above the bandwidth of the input signal. Voice bandwidth is 4 kHz and clock rates from 8 k and up are possible. Thus the delta modulator digitizes and transmits the analog input to a remote receiver. The serial, unframed nature of the data is ideal for communications networks. With no input at the transmitter, a continuous one zero alternation is transmitted. If the two integrators are made leaky, then during any loss of contact the receiver output decays to zero and receive restart begins without framing when the receiver reacquires. Similarly a delta modulator is tolerant of sporadic bit errors. Figure 12 shows the delta modulator waveforms while Figure 13 shows the corresponding CVSD decoder block diagram.

The Companding Algorithm

The fundamental advantages of the delta modulator are its simplicity and the serial format of its output. Its limitations are its ability to accurately convert the input within a limited digital bit rate. The analog input must be band limited and amplitude limited. The frequency limitations are governed by the nyquist rate while the amplitude capabilities are set by the gain of the integrator.

The frequency limits are bounded on the upper end; that is, for any input bandwidth there exists a clock frequency larger than that bandwidth which will transmit the signal with a specific noise level. However, the amplitude limits are bounded on both upper and lower ends. For a signal level, one specific gain will achieve an optimum noise level. Unfortunately, the basic delta modulator has a small dynamic range over which the noise level is constant.

The continuously variable slope circuitry provides increased dynamic range by adjusting the gain of the integrator. For a given clock frequency and input bandwidth the additional circuitry increases the delta modulator's dynamic range. External to the basic delta modulator is an algorithm which monitors the past few outputs of the delta modulator in a simple shift register. The register is 3 bits long. The accepted CVSD algorithm simply monitors the contents of the shift register and indicates if it contains all 1s or 0s. This condition is called coincidence. When it occurs, it indicates that the gain of the integrator is too small. The coincidence output charges a single pole low pass filter. The voltage output of this syllabic filter controls the integrator gain through a pulse amplitude modulator whose other input is the sign bit or up/down control.

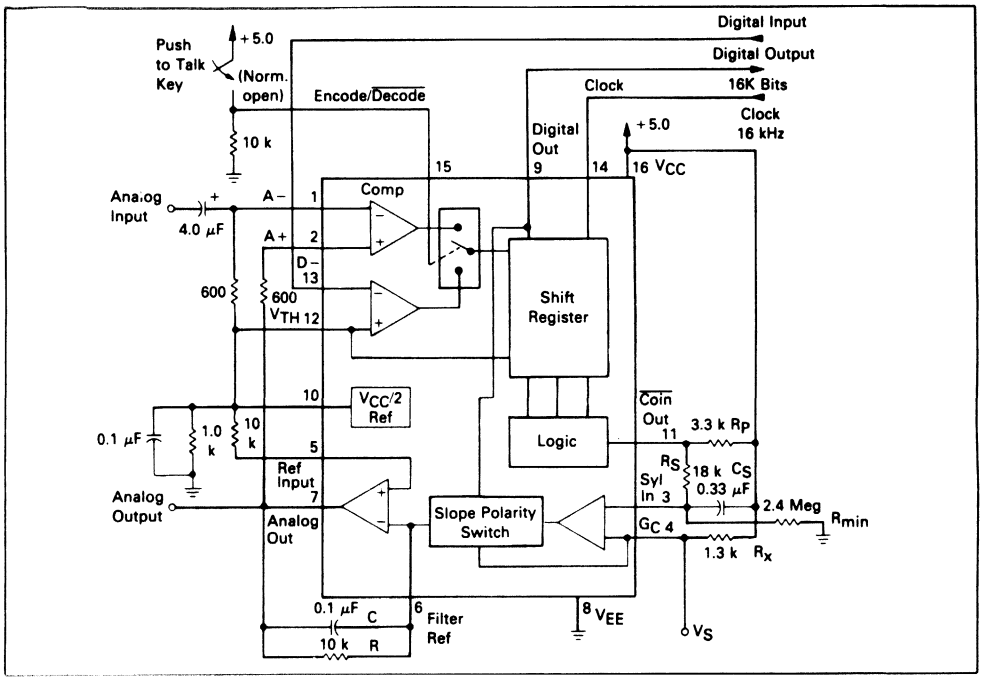
The simplicity of the all ones, all zeros algorithm should not be taken lightly. Many other control algorithms using the shift register have been tried. The key to the accepted algorithm is that it provides a measure of the average power or level of the input signal. Other techniques provide more instantaneous information about the shape of the input curve. The purpose of the algorithm is to control the gain of the integrator and to increase the dynamic range. Thus a measure of the average input level is what is needed.

The algorithm is repeated in the receiver and thus the level data is recovered in the receiver. Because the algorithm only operates on the past serial data, it changes the nature of the bit stream without changing the channel bit rate.

The effect of the algorithm is to compand the input signal. If a CVSD encoder is played into a basic delta modulator, the output of the delta modulator will reflect the shape of the input signal but all of the output will be at an equal level. Thus the algorithm at the output is needed to restore the level variations. The bit stream in the channel is as if it were from a standard delta modulator with a constant level input.

The delta modulator encoder with the CVSD algorithm provides an efficient method for digitizing a voice input in a manner which is especially convenient for digital communications requirements.

FIGURE 14 — 16 kHz SIMPLEX VOICE CODEC
(Using MC34115, Single Pole Companding and Single Integration)



APPLICATIONS INFORMATION

CVSD DESIGN CONSIDERATIONS

A simple CVSD encoder using the MC34115 is shown in Figure 14. This IC is a general purpose CVSD building block which allow the system designer to tailor the encoder's transmission characteristics to the application. Thus, the achievable transmission capabilities are constrained by the fundamental limitations of delta modulation and the design of encoder parameters. The performance is not dictated by the internal configuration of the MC34115. There are six design considerations involved in designing the basic CVSD building block into a specific codec application.

These are listed below:

1. Selection of clock rate
2. Selection of loop gain
3. Selection of minimum step size
4. Design of integration filter transfer function
5. Design of syllabic filter transfer function
6. Design of low pass filter at the receiver

The circuit in Figure 14 is the most basic CVSD circuit possible. For many applications in secure radio or other intelligible voice channel requirements, it is entirely sufficient. In this circuit, items 4 and 5 are reduced to their simplest form. They syllabic and integration filters are both single pole networks. The selection of items 1 through 3 govern the codec performance.

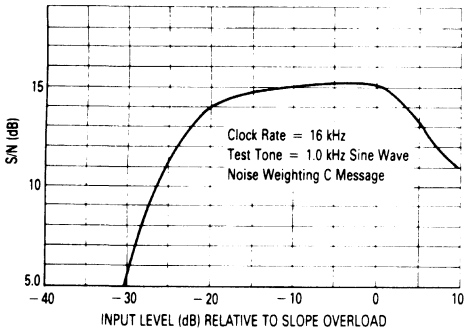
Layout Considerations

Care should be exercised to isolate all digital signal paths (Pins 9, 11, 13, and 14) from analog signal paths (Pins 1–7 and 10) in order to achieve proper idle channel performance.

Clock Rate

With minor modifications the circuit in Figure 14 may be operated anywhere from 9.6 kHz to 64 kHz clock rates. Obviously the higher the clock rate the higher the S/N performance. The circuit in Figure 14 typically produces the S/N performance shown in Figure 15. The selection of clock rate is usually dictated by the bandwidth of the transmission medium. Voice bandwidth systems will require no higher than 9600 Hz. Some radio systems will allow 12 kHz. Private 4-wire telephone systems are often operated at 16 kHz and commercial telephone performance can be achieved at 32K bits and above.

FIGURE 15 — SIGNAL-TO-NOISE PERFORMANCE OF MC34115 WITH SINGLE INTEGRATION, SINGLE-POLE AND COMPANDING AT 16K BITS — TYPICAL



Selection of Loop Gain

The gain of the circuit in Figure 14 is set by resistor R_X. R_X must be selected to provide the proper integrator step size for high level signals such that the companding ratio does not exceed about 25%. The companding ratio is the active low duty cycle of the coincidence output on Pin 11 of the codec circuit. Thus the system gain is dependent on:

1. The maximum level and frequency of the input signal.
2. The transfer function of the integration filter.

For voice codecs the typical input signal is taken to be a sine wave at 1 kHz of 0 dBmo level. In practice, the useful dynamic range extends about 6 dB above the design level. In any system the companding ratio should not exceed 30%.

To calculate the required step size current, we must describe the transfer characteristics of the integration filter. In the basic circuit of Figure 14, a single pole of 160 Hz is used.

$$R = 10\ k\Omega,\ C = 0.1\ \mu F$$

$$\frac{V_O}{I_i} = \frac{1}{C(S + 1/RC)} \equiv \frac{K}{S + \omega_O}$$

$$\omega_O = 2\pi f$$

$$10^3 = \omega_O = 2\pi f$$

$$f = 159.2\ Hz$$

Note that the integration filter produces a single-pole response from 300 to 3 kHz. The current required to move the integrator output a specific voltage from zero is simply:

$$I_i = \frac{V_O}{R} + C\frac{dV_O}{dt}$$

Now a 0 dBmo sine wave has a peak value of 1.0954 volts. In 1/8 of a cycle of a sine wave centered around the zero crossing, the sine wave changes by approximately its peak value. The CVSD step should trace that change. The required current for a 0 dBm 1 kHz sine wave is:

$$I_i = \frac{1.1\ V}{*2(10\ k\Omega)} + \frac{0.1\ \mu F(1.1)}{0.125\ ms} = 0.935\ mA$$

*The maximum voltage across R when maximum slew is required is:

$$\frac{1.1\ V}{2}$$

Now the voltage range of the syllabic filter is the power supply voltage, thus:

$$R_X = 0.25(V_{CC})\frac{1}{0.935\ mA}$$

A similar procedure can be followed to establish the proper gain for any input level and integration filter type.

Minimum Step Size

The final parameter to be selected for the simple codec in Figure 14 is idle channel step size. With no input signal, the digital output becomes a one-zero alternating pattern and the analog output becomes a small triangle wave. Mismatches of internal currents and offsets limit the minimum step size which will produce a perfect idle channel pattern. The MC34115 is tested to ensure that a 20 mVp-p mimimum step size at 16 kHz will attain a proper idle channel. The idle channel step size must be twice the specified total loop offset if a one-zero idle pattern is desired. In some applications a much smaller minimum step size (e.g., 0.1 mV) can produce quiet performance without providing a 1-0 pattern.

CVSD DESIGN CONSIDERATIONS (continued)

To set the idle channel step size, the value of R_{min} must be selected. With no input signal, the slope control algorithm is inactive. A long series of ones or zeros never occurs. Thus, the voltage across the syllabic filter capacitor (C_S) would decay to zero. However, the voltage divider of R_S and R_{min} (see Figure 14) sets the minimum allowed voltage across the syllabic filter capacitor. That voltage must produce the desired ramps at the analog output. Again we write the filter input current equation:

$$I_i = \frac{V_o}{R} + C\frac{dV_o}{dt}$$

For values of V_o near $V_{CC}/2$ the V_o/R term is negligible; thus

$$I_i = C_S\frac{\Delta V_o}{\Delta T}$$

where ΔT is the clock period and ΔV_o is the desired peak-to-peak value of the idle output. For a 16K-bit system using the circuit in Figure 14

$$I_i = \frac{0.1\ \mu F\ 20\ mV}{62.5\ \mu s} = 32\ \mu A$$

The voltage on C_S which produces a 32 μA current is determined by the value of R_x.

$I_iR_x = V_Smin$; for 32 μA, V_Smin = 41.6 mV

In Figure 14 R_S is 18 kΩ. That selection is discussed with the syllabic filter considerations. The voltage divider of R_S and R_{min} must produce an output of 41.6 mV.

$$V_{CC}\frac{R_S}{R_S + R_{min}} = V_{Smin} \quad R_{min} \simeq 2.4\ M\Omega$$

Having established these three parameters — clock rate, loop gain and minimum step size — the encoder circuit in Figure 14 will function at near optimum performance for input levels around 0 dBm.

3

INCREASING CVSD PERFORMANCE

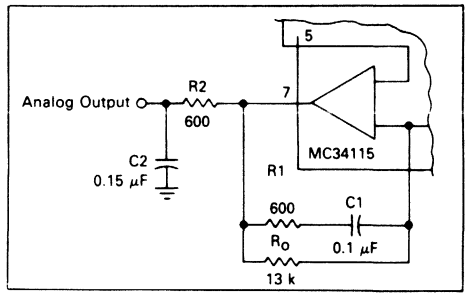
Integration Filter Design

The circuit in Figure 14 uses a single-pole integration network formed with a 0.1 μF capacitor and a 10 kΩ resistor. It is possible to improve the performance of the circuit in Figure 14 by 1 or 2 dB by using a two-pole integration network. The improved circuit is shown.

The first pole is still placed below 300 Hz to provide the 1/S voice content curve and a second pole is placed somewhere above the 1 kHz frequency. For telephony circuits, the second pole can be placed above 1.8 kHz to exceed the 1633 touchtone frequency. In other communication systems, values as low as 1 kHz may be selected. In general, the lower in frequency the second pole is placed, the greater the noise improvement. Then, to ensure the encoder loop stability, a zero is added to keep the phase shift less than 180°. This zero should be placed slightly above the low-pass output filter break frequency so as not to reduce the effectiveness of the second pole. A network of 235 Hz, 2 kHz and 5.2 kHz is typical for telephone applications while 160 Hz, 1.2 kHz and 2.8 kHz might be used in voice only channels. (Voice only channels can use an output low-pass filter which breaks at about 2.5 kHz.) The two-pole network in Figure 16 has a transfer function of:

$$\frac{V_o}{I_i} = \frac{R_0R_1\left(S + \frac{1}{R_1C_1}\right)}{R_2C_2(R_0 + R_1)\left(S + \frac{1}{(R_0 + R_1)C_1}\right)S + \left(\frac{1}{R_2C_2}\right)}$$

FIGURE 16 — IMPROVED FILTER CONFIGURATION



These component values are for the telephone channel circuit poles described in the text. The R2, C2 product can be provided with different values of R and C. R2 should be chosen to be equal to the termination resistor on Pin 1.

Thus the two poles and the zero can be selected arbitrarily as long as the zero is at a higher frequency than the first pole. The values in Figure 16 represent one implementation of the telephony filter requirement.

The selection of the two-pole filter network affects the selection of the loop gain value and the minimum step size resistor. The required integrator current for a given change in voltage now becomes:

$$I_i = \frac{V_o}{R_0} + \left(\frac{R_2C_2}{R_0} + \frac{R_1C_1}{R_0} + C_1\right)\frac{\Delta V_o}{\Delta T} + \left(R_2C_2C_1 + \frac{R_1C_1R_2C_2}{R_0}\right)\frac{\Delta V_o^2}{\Delta T^2}$$

The calculation of desired gain resistor R_X then proceeds exactly as previously described.

Syllabic Filter Design

The syllabic filter in Figure 14 is a simple single-pole network of 18 kΩ and 0.33 μF. This produces a 6.0 ms time constant for the averaging of the coincidence output signal. The voltage across the capacitor determines the integrator current which in turn establishes the step size. The integrator current and the resulting step size determine the companding ratio and the S/N performance. The companding ratio is defined as the voltage across C_S/V_{CC}.

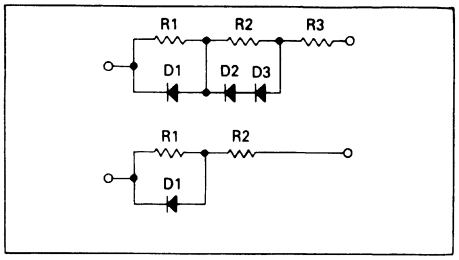
The S/N performance may be improved by modifying the voltage to current transformation produced by R_X. If different portions of the total R_X are shunted by diodes, the integrator current can be other than $(V_{CC} - V_S)/R_X$. These breakpoint curves must be designed experimentally for the particular system application. In general, one would wish that the current would double with input level. To design the desired curve, supply current to Pin 4 of the codec from an external source. Input a signal level and adjust the current until the S/N performance is optimum. Then record the syllabic filter voltage and the current. Repeat this for all desired signal levels. Then derive the resistor diode network which produces that curve on a curve tracer.

Once the network is designed with the curve tracer, it is then inserted in place of R_X in the circuit and the forced optimum noise performance will be achieved from the active syllabic algorithm.

Diode breakpoint networks may be very simple or moderately complex and can improve the usable dynamic range of any codec. In the past they have been used in high performance telephone codecs.

Typical resistor-diode networks are shown in Figure 17.

FIGURE 17 — RESISTOR-DIODE NETWORKS



Output Low Pass Filter

A low pass filter is required at the receiving circuit output to eliminate quantizing noise. In general, the lower the bit rate, the better the filter must be. The filter in Figure 18 provides excellent performance for 12 kHz to 40 kHz systems.

FIGURE 18 — HIGH PERFORMANCE ELLIPTIC FILTER FOR CVSD OUTPUT

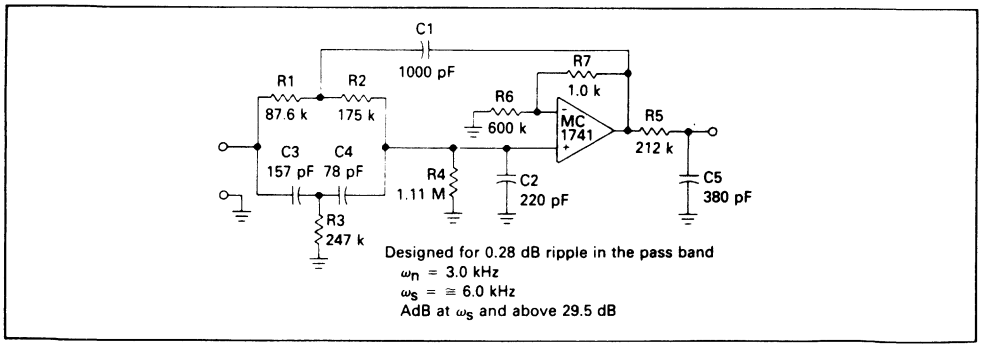
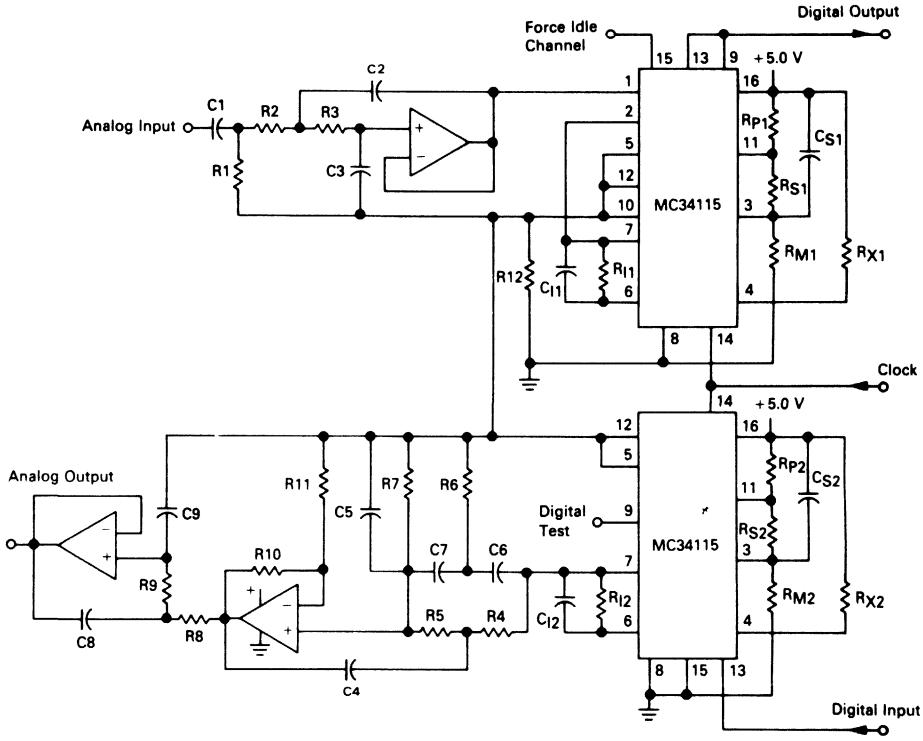


FIGURE 19 — FULL DUPLEX/16K BIT CVSD VOICE CODEC USING MC34115 AND MC3503/6 OP AMP



Codec Components

R_{X1}, R_{X2} — 3.3 kΩ
R_{P1}, R_{P2} — 3.3 kΩ
R_{S1}, R_{S2} — 100 kΩ
R_{I1}, R_{I2} — 20 kΩ
R_{12} — 1 kΩ
R_{M1}, R_{M2} — 10 MΩ
Minimum step size = 20 mV
C_{S1}, C_{S2} — 0.05 μF
C_{I1}, C_{I2} — 0.05 μF
2 MC34115
1 MC3403 (or MC3406)

Note: All Res. 5%
All Cap. 5%

Input Filter Specifications

12 dB/Octave Rolloff above 3.3 kHz
6 dB/Octave Rolloff below 50 Hz

Output Filter Specifications

Break Frequency — 3.3 kHz
Stop Band — 9 kHz
Stop Band Atten. — 50 dB
Rolloff — >40 dB/Octave

Filter Components

R1 — 965 Ω
R2 — 72 kΩ
R3 — 72 kΩ
R4 — 63.46 kΩ
R5 — 127 kΩ
R6 — 365.5 kΩ
R7 — 1.645 MΩ
R8 — 72 kΩ
R9 — 72 kΩ
R10 — 29.5 kΩ
R11 — 72 kΩ

C1 — 3.3 μF
C2 — 837 pF
C3 — 536 pF
C4 — 1000 pF
C5 — 222 pF
C6 — 77 pF
C7 — 38 pF
C8 — 837 pF
C9 — 536 pF

Note: All Res. 0.1% to 1%.
All Cap. 1.0%

MOTOROLA

MC34118

Specifications and Applications Information

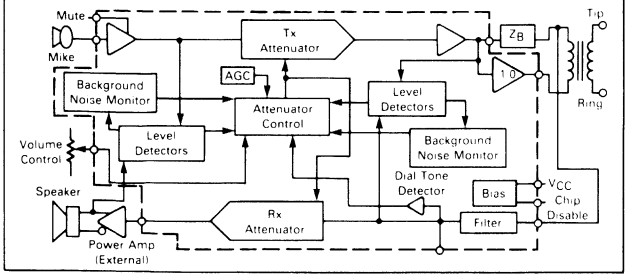
VOICE SWITCHED SPEAKERPHONE CIRCUIT

The MC34118 Voice Switched Speakerphone Circuit incorporates the necessary amplifiers, attenuators, level detectors, and control algorithm to form the heart of a high quality hands-free speakerphone system. Included are a microphone amplifier with adjustable gain and MUTE control, Transmit and Receive attenuators which operate in a complementary manner, level detectors at both input and output of both attenuators, and background noise monitors for both the transmit and receive channels. A Dial Tone Detector prevents the dial tone from being attenuated by the Receive background noise monitor circuit. Also included are two line driver amplifiers which can be used to form a hybrid network in conjunction with an external coupling transformer. A high-pass filter can be used to filter out 60 Hz noise in the receive channel, or for other filtering functions. A Chip Disable pin permits powering down the entire circuit to conserve power on long loops where loop current is at a minimum.

The MC34118 may be operated from a power supply, or it can be powered from the telephone line, requiring typically 5.0 mA. The MC34118 can be interfaced directly to Tip and Ring (through a coupling transformer) for stand-alone operation, or it can be used in conjunction with a handset speech network and or other features of a featurephone.

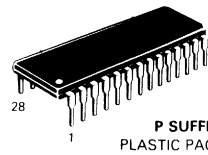
- Improved Attenuator Gain Range: 52 dB Between Transmit and Receive
- Low Voltage Operation for Line-Powered Applications (3.0–6.5 V)
- 4-Point Signal Sensing for Improved Sensitivity
- Background Noise Monitors for Both Transmit and Receive Paths
- Microphone Amplifier Gain Set by External Resistors — Mute Function Included
- Chip Disable for Active Standby Operation
- On Board Filter Pinned-Out for User Defined Function
- Dial Tone Detector to Inhibit Receive Idle Mode During Dial Tone Presence
- Standard 28-Pin Plastic DIP Package and SOIC Package Available
- Compatible with MC34119 Speaker Amplifier

SIMPLIFIED BLOCK DIAGRAM

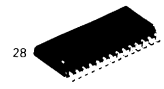


VOICE SWITCHED SPEAKERPHONE CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 710-02



DW SUFFIX
PLASTIC PACKAGE
CASE 751F-01

PIN CONNECTIONS

(Top View)

FO	1	28	GND
FI	2	27	CPR
CD	3	26	RLI1
V_{CC}	4	25	RLO1
HTO	5	24	TLO1
HTO	6	23	TLI1
HTI	7	22	RXO
TXO	8	21	RXI
TXI	9	20	RLI2
MCO	10	19	RLO2
MCI	11	18	TLO2
MUT	12	17	TLI2
VLC	13	16	CPT
CT	14	15	V_B

(Pin assignments same for both packages)

DS9696

ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Units
Supply Voltage (Pin 4)	−1.0, +7.0	Vdc
Voltage at CD (Pin 3), MUT (Pin 12)	−1.0, V_{CC} + 1.0	Vdc
Voltage at VLC (Pin 13)	−1.0, V_{CC} + 0.5	Vdc
Voltage at TXI (Pin 9), RXI (Pin 21), FI (Pin 2)	−0.5, V_{CC} + 0.5	Vdc
Storage Temperature Range	−65 to +150	°C

Devices should not be operated at or outside these values. The "Recommended Operating Limits" provide for actual device operation.

RECOMMENDED OPERATING LIMITS

Parameter	Min	Typ	Max	Units
Supply Voltage (Pin 4) (See Text)	3.5	—	6.5	Vdc
CD Input (Pin 3), MUT Input (Pin 12)	0	—	V_{CC}	Vdc
I_{VB} Current (Pin 15)	—	—	500	μA
VLC (Pin 13)	0.3 x V_B	—	V_B	Vdc
Attenuator Input Signal Voltage (Pins 9, 21)	0	—	350	mVrms
Microphone Amplifier, Hybrid Amplifier Gain	0	—	40	dB
Load Current @ RXO, TXO (Pins 8, 22) @ MCO (Pin 10) @ HTO−, HTO+ (Pins 6, 5)	0 0 0	— — —	±2.0 ±1.0 ±5.0	mA
Ambient Operating Temperature Range	−20	—	+60	°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0 V, CD ≤ 0.8 V, unless noted)

Parameter	Symbol	Min	Typ	Max	Units
POWER SUPPLY					
V_{CC} Supply Current (V_{CC} = 6.5 V, CD = 0.8 V) (V_{CC} = 6.5 V, CD = 2.0 V)	I_{CC}	— —	5.5 600	8.0 800	mA μA
CD Input Resistance (V_{CC} = V_{CD} = 6.5 V) CD Input Voltage — High — Low	R_{CD} V_{CDH} V_{CDL}	50 2.0 0	90 — —	— V_{CC} 0.8	kΩ Vdc Vdc
V_B Output Voltage (V_{CC} = 3.5 V) (V_{CC} = 5.0 V)	V_B	— 1.8	1.3 2.1	— 2.4	Vdc
V_B Output Resistance (I_{VB} = 1.0 mA)	R_{OVB}	—	400	—	Ω
V_B Power Supply Rejection Ratio (C_{VB} = 220 μF, f = 1.0 kHz)	PSRR	—	54	—	dB
ATTENUATORS (T_A = +25°C)					
Receive Attenuator Gain (f = 1.0 kHz, V_{LC} = V_B) Rx Mode, RXI = 150 mVrms (V_{CC} = 5.0 V) Rx Mode, RXI = 150 mVrms (V_{CC} = 3.5 V) Gain Change − V_{CC} = 3.5 V versus V_{CC} = 5.0 V AGC Gain Change − V_{CC} = 2.8 V versus V_{CC} = 5.0 V* Idle Mode, RXI = 150 mVrms Range (Rx to Tx Mode)	 G_{RX} G_{RX} ΔG_{RX1} ΔG_{RX2} G_{RXI} ΔG_{RX3}	 +4.0 +4.0 −0.5 — −22 49	 +6.0 +6.0 0 −25 −20 52	 +8.0 +8.0 +0.5 −15 −17 54	dB
Volume Control Range (Rx Mode, 0.3 V_B < V_{LC} < V_B)	V_{CR}	27	35	—	dB
RXO DC Voltage (Rx Mode)	V_{RXO}	—	V_B	—	Vdc
ΔRXO DC Voltage (Rx to Tx Mode)	ΔV_{RXO}	—	±10	±150	mV
RXO High Voltage (I_{out} = −1.0 mA RXI = V_B + 1.5 V)	V_{RXOH}	3.7	—	—	Vdc
RXO Low Voltage (I_{out} = +1.0 mA, RXI = V_B − 1.0, Output measured with respect to V_B)*	V_{RXOL}	—	−1.5	−1.0	Vdc
RXI Input Resistance (RXI < 350 mVrms)	R_{RXI}	7.0	10	14	kΩ

(continued)

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0 V, CD ≤ 0.8 V, unless noted)

Parameter	Symbol	Min	Typ	Max	Units
ATTENUATORS — continued (T_A = +25°C)					
Transmit Attenuator Gain (f = 1.0 kHz) Tx Mode, TXI = 150 mVrms Idle Mode, TXI = 150 mVrms Range (Tx to Rx Mode)	 G_{TX} G_{TXI} ΔG_{TXI}	 +4.0 −22 49	 +6.0 −20 52	 +8.0 −17 54	dB
TXO DC Voltage (Tx Mode)	V_{TXO}	—	V_B	—	Vdc
ΔTXO DC Voltage (Tx to Rx Mode)	ΔV_{TXO}	—	±30	±150	mV
TXO High Voltage (I_{out} = −1.0 mA TXI = V_B + 1.5 V)	V_{TXOH}	3.7	—	—	Vdc
TXO Low Voltage (I_{out} = +1.0 mA, TXI = V_B − 1.0 V, Output measured with respect to V_B)*	V_{TXOL}	—	−1.5	−1.0	Vdc
TXI Input Resistance (TXI < 350 mVrms)	R_{TXI}	7.0	10	14	kΩ
Gain Tracking (G_{RX} + G_{TX}, @ Tx, Idle, Rx)*	G_{TR}	—	±0.1	—	dB

*See text for explanation.

ATTENUATOR CONTROL (T_A = +25°C)

C_T Voltage (Pin 14 − V_B) Rx Mode (V_{LC} = V_B) Idle Mode Tx Mode	V_{CT}	 — — —	 +240 0 −240	 — — —	mV
C_T Source Current (switching to Rx mode)	I_{CTR}	−85	−60	−40	μA
C_T Sink Current (switching to Tx mode)	I_{CTT}	+40	+60	+85	μA
C_T Slow Idle Current	I_{CTS}	—	0	—	μA
C_T Fast Idle Internal Resistance	R_{FI}	1.5	2.0	3.6	kΩ
V_{LC} Input Current	I_{VLC}	—	−60	—	nA
Dial Tone Detector Threshold	V_{DT}	10	15	20	mV

MICROPHONE AMPLIFIER (T_A = +25°C, V_{MUT} ≤ 0.8 V, A_{VCL} = 31 dB unless otherwise noted)

Ouptut Offset (V_{MCO} − V_B, Feedback R = 180 kΩ)	MCO_{VOS}	−50	0	+50	mVdc
Open Loop Gain (f < 100 Hz)	A_{VOLM}	70	80	—	dB
Gain Bandwidth	GBW_M	—	1.0	—	MHz
Output High Voltage (I_{out} = −1.0 mA, V_{CC} = 5.0 V)	V_{MCOH}	3.7	—	—	Vdc
Output Low Voltage (I_{out} = +1.0 mA)	V_{MCOL}	—	—	200	mVdc
Input Bias Current (@ MCI)	I_{BM}	—	−40	—	nA
Muting (ΔGain) (f = 1.0 kHz, V_{MUT} = 2.0 V) (300 Hz < f < 10 kHz)	GMT	−55 —	— −68	— —	dB
MUT Input Resistance (V_{CC} = V_{MUT} = 6.5 V)	R_{MUT}	50	90	—	kΩ
MUT Input — High	V_{MUTH}	2.0	—	V_{CC}	Vdc
MUT Input — Low	V_{MUTL}	0	—	0.8	Vdc
Distortion (300 Hz < f < 10 kHz)	THD_M	—	0.15	—	%

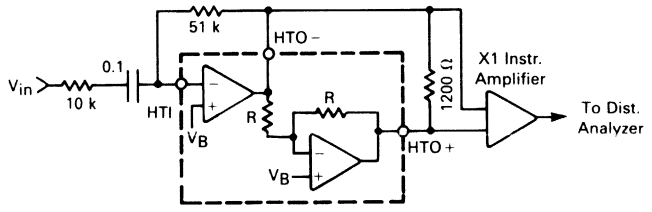
HYBRID AMPLIFIERS (T_A = +25°C)

HTO− Offset (V_{HTO-} − V_B, Feedback R = 51 kΩ)	H_{VOS}	−20	0	+20	mVdc
HTO− to HTO+ Offset (Feedback R = 51 kΩ)	HB_{VOS}	−30	0	+30	mVdc
Open Loop Gain (HTI to HTO−, f < 100 Hz)	A_{VOLH}	60	80	—	dB
Gain Bandwidth	GBW_H	—	1.0	—	MHz
Closed Loop Gain (HTO− to HTO+)	A_{VCLH}	−0.35	0	+0.35	dB
Input Bias Current (@ HTI)	I_{BH}	—	−30	—	nA
HTO− High Voltage (I_{out} = −5.0 mA)	V_{HT-H}	3.7	—	—	Vdc
HTO− Low Voltage (I_{out} = +5.0 mA)	V_{HT-L}	—	—	250	mVdc
HTO+ High Voltage (I_{out} = −5.0 mA)	V_{HT+H}	3.7	—	—	Vdc
HTO+ Low Voltage (I_{out} = +5.0 mA)	V_{HT+L}	—	—	450	mVdc
Distortion (300 Hz < f < 10 kHz, See Figure 1)	THD_H	—	0.3	—	%

Parameter	Symbol	Min	Typ	Max	Units
LEVEL DETECTORS AND BACKGROUND NOISE MONITORS (T_A = +25°C)					
Transmit-Receive Switching Threshold (Ratio of Current at RLI1 + RLI2 to 20 μA at TLI1 + TLI2 to switch from Tx to Rx)	I_{TH}	0.8	1.0	1.2	
Source Current at RLO1, RLO2, TLO1, TLO2	I_{LSO}	—	−2.0	—	mA
Sink Current at RLO1, RLO2, TLO1, TLO2	I_{LSK}	—	4.0	—	μA
CPR, CPT Output Resistance (I_{out} = 1.5 mA)	R_{CP}	—	35	—	Ω
CPR, CPT Leakage Current	I_{CPLK}	—	−0.2	—	μA
FILTER (T_A = +25°C)					
Voltage Offset at FO (V_{FO} − V_B, 220 kΩ from V_B to FI)	FO_{VOS}	−200	−90	0	mV
FO Sink Current	I_{FO}	150	260	400	μA
FI Bias Current	I_{FI}	—	−50	—	nA
SYSTEM DISTORTION (T_A = +25°C, f = 1.0 kHz)					
Rx Mode (From FI to RXO, FO connected to RXI)	THD_R	—	0.5	3.0	%
Tx Mode (From MCI to HTO−/HTO+, includes Tx attenuator)	THD_T	—	0.8	3.0	%

1. All currents into a device pin are positive, those out of a pin are negative. Algebraic convention rather than magnitude is used to define limits.

FIGURE 1 — HYBRID AMPLIFIER DISTORTION TEST



TEMPERATURE CHARACTERISTICS

Parameter	Typical Value @ 25°C	Typical Change −20 to +60°C
V_{CC} Supply Current (CD = 0.8 V)	5.0 mA	−0.3 %/°C
V_{CC} Supply Current (CD = 2.0 V)	400 μA	−0.4 %/°C
V_B Output Voltage (V_{CC} = 5.0 V)	2.1 V	+0.8 %/°C
Attenuator Gain (Max Gain)	+6.0 dB	0.0008 dB/°C
Attenuator Gain (Max Attenuation)	−46 dB	0.004 dB/°C
Attenuator Input Resistance (@ TXI, RXI)	10 kΩ	+0.6 %/°C
Dial Tone Detector Threshold	15 mV	+20 μV/°C
CT Source, Sink Current	±60 μA	−0.15 %/°C
Microphone, Hybrid Amplifier Offset	0 mV	±4.0 μV/°C
Transmit-Receive Switching Threshold	1.0	±0.02 %/°C
Sink Current at RLO1, RLO2, TLO1, TLO2	4.0 μA	−10 nA/°C
Closed Loop Gain (HTO− to HTO+)	0 dB	0.001 %/°C

PIN DESCRIPTION

Pin	Name	Description
1	FO	Filter output. Output impedance is less than 50 ohms.
2	FI	Filter input. Input impedance is greater than 1.0 Mohm.
3	CD	Chip Disable. A logic low (<0.8 V) sets normal operation. A logic high (>2.0 V) disables the IC to conserve power. Input impedance is nominally 90 kΩ.
4	V_{CC}	A supply voltage of +2.8 to +6.5 volts is required, at ≈ 5.0 mA. As V_{CC} falls from 3.5 to 2.8 volts, an AGC circuit reduces the receive attenuator gain by ≈ 25 dB (when in the receive mode).
5	HTO+	Output of the second hybrid amplifier. The gain is internally set at −1.0 to provide a differential output, in conjunction with HTO−, to the hybrid transformer.
6	HTO−	Output of the first hybrid amplifier. The gain of the amp is set by external resistors.
7	HTI	Input and summing node for the first hybrid amplifier. DC level is ≈V_B.
8	TXO	Output of the transmit attenuator. DC level is approximately V_B.
9	TXI	Input to the transmit attenuator. Max. signal level is 350 mVrms. Input impedance is ≈10 kΩ.
10	MCO	Output of the microphone amplifier. The gain of the amplifier is set by external resistors.
11	MCI	Input and summing node of the microphone amplifier. DC level is ≈ V_B.
12	MUT	Mute input. A logic low (<0.8 V) sets normal operation. A logic high (>2.0 V) mutes the microphone amplifier without affecting the rest of the circuit. Input impedance is nominally 90 kΩ.

Pin	Name	Description
13	VLC	Volume control input. When VLC = V_B, the receive attenuator is at maximum gain when in the receive mode. When VLC = 0.3 V_B, the receive gain is down 35 dB. Does not affect the transmit mode.
14	C_T	An RC at this pin sets the response time for the circuit to switch modes.
15	V_B	An output voltage ≈V_{CC}/2. This voltage is a system ac ground, and biases the volume control. A filter cap is required.
16	CPT	An RC at this pin sets the time constant for the transmit background monitor.
17	TLI2	Input to the transmit level detector on the mike/speaker side.
18	TLO2	Output of the transmit level detector on the mike/speaker side, and input to the transmit background monitor.
19	RLO2	Output of the receive level detector on the mike/speaker side.
20	RLI2	Input to the receive level detector on the mike/speaker side.
21	RXI	Input to the receive attenuator and dial tone detector. Max input level is 350 mV RMS. Input impedance is ≈10 kΩ.
22	RXO	Output of the receive attenuator. DC level is approximately V_B.
23	TLI1	Input to the transmit level detector on the line side.
24	TLO1	Output of the transmit level detector on the line side.
25	RLO1	Output of the receive level detector on the line side, and input to the receive background monitor.
26	RLI1	Input to the receive level detector on the line side.
27	CPR	An RC at this pin sets the time constant for the receive background monitor.
28	GND	Ground pin for the entire IC.

Note: Pin numbers are identical for the DIP package and the SOIC package.

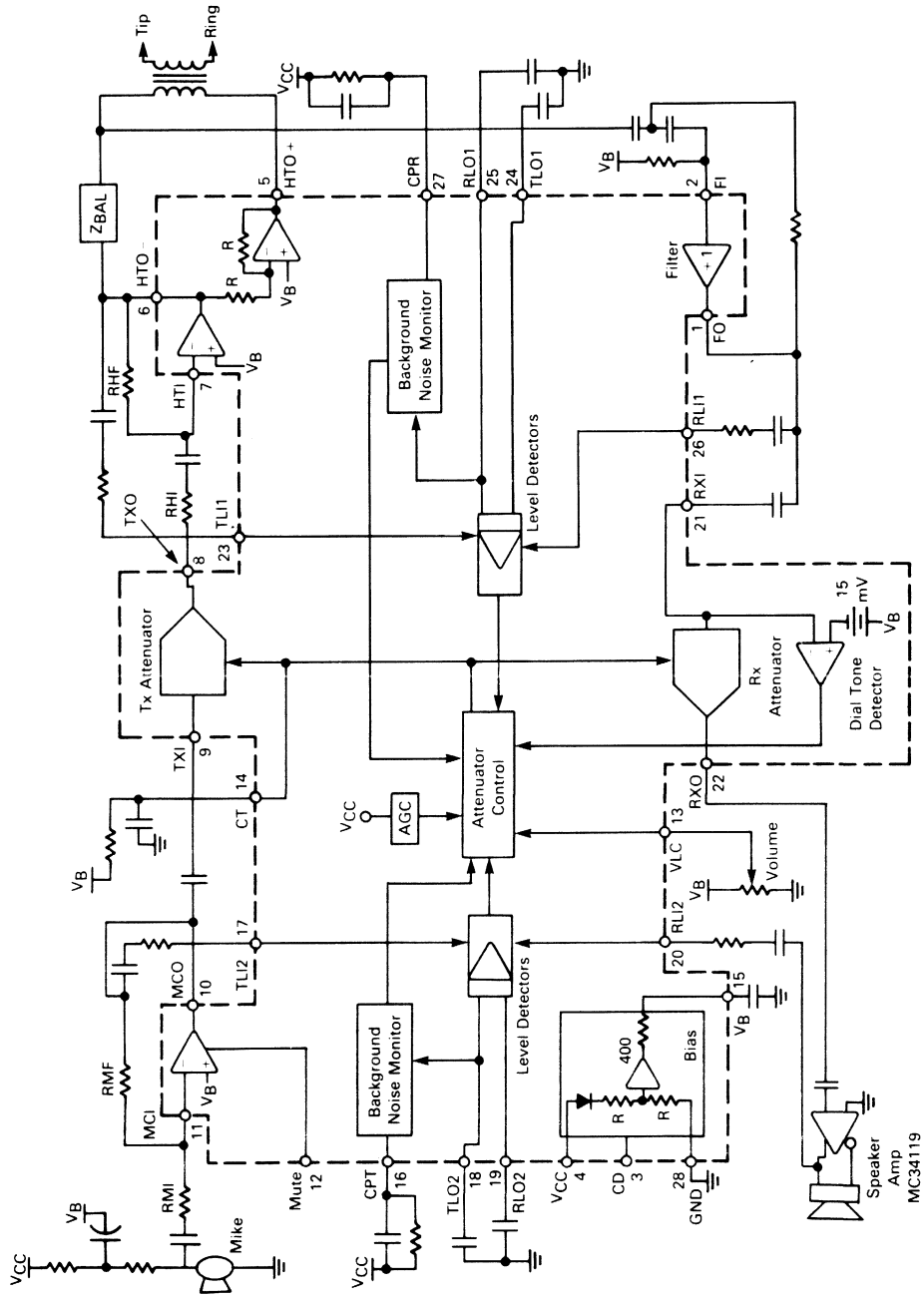


FIGURE 2 — MC34118 BLOCK DIAGRAM

3

FUNCTIONAL DESCRIPTION

INTRODUCTION

The fundamental difference between the operation of a speakerphone and a handset is that of half-duplex versus full-duplex. The handset is full duplex since conversation can occur in both directions (transmit and receive) simultaneously. A speakerphone has higher gain levels in both paths, and attempting to converse full duplex results in oscillatory problems due to the loop that exists within the system. The loop is formed by the receive and transmit paths, the hybrid, and the acoustic coupling (speaker to microphone). The only practical and economical solution used to date is to design the speakerphone to function in a half duplex mode — i.e., only one person speaks at a time, while the other listens. To achieve this requires a circuit which can detect who is talking, switch on the appropriate path (transmit or receive), and switch off (attenuate) the other path. In this way, the loop gain is maintained less than unity. When the talkers exchange function, the circuit must quickly detect this, and switch the circuit appropriately. By providing speech level detectors, the circuit operates in a "hands-free" mode, eliminating the need for a "push-to-talk" switch.

The handset, by the way, has the same loop as the speakerphone. But since the gains are considerably lower, and since the acoustic coupling from the earpiece to the mouthpiece is almost non-existent (the receiver is normally held against a person's ear), oscillations don't occur.

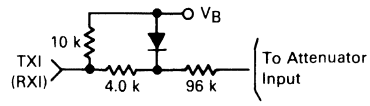
The MC34118 provides the necessary level detectors, attenuators, and switching control for a properly operating speakerphone. The detection sensitivity and timing are externally controllable. Additionally, the MC34118 provides background noise monitors which make the circuit insensitive to room and line noise, hybrid amplifiers for interfacing to Tip and Ring, the microphone amplifier, and other associated functions. Please refer to the Block Diagram (Figure 2) when reading the following sections.

ATTENUATORS

The transmit and receive attenuators are complementary in function, i.e., when one is at maximum gain (+6.0 dB), the other is at maximum attenuation (−46 dB), and vice versa. They are never both fully on or both fully off. The sum of their gains remains constant (within a nominal error band of ±0.1 dB) at a typical value of −40 dB (see Figure 10). Their purpose is to control the transmit and receive paths to provide the half-duplex operation required in a speakerphone.

The attenuators are non-inverting, and have a −3.0 dB (from max gain) frequency of ≈100 kHz. The input impedance of each attenuator (TXI and RXI) is nominally 10 kΩ (see Figure 3), and the input signal should be limited to 350 mVrms (990 mVp-p) to prevent distortion. That maximum recommended input signal is independent of the volume control setting. The diode clamp on the inputs limits the input swing, and therefore the maximum negative output swing. This is the reason for V_{RXOL} and V_{TXOL} specification being defined as they are in the Electrical Characteristics. The output impedance is <10 Ω until the output current limit (typically 2.5 mA) is reached.

FIGURE 3 — ATTENUATOR INPUT STAGE



The attenuators are controlled by the single output of the Control Block, which is measurable at the C_T pin (Pin 14). When the C_T pin is at +240 millivolts with respect to V_B, the circuit is in the receive mode (receive attenuator is at +6.0 dB). When the C_T pin is at −240 millivolts with respect to V_B, the circuit is in the transmit mode (transmit attenuator is at +6.0 dB). The circuit is in an idle mode when the C_T voltage is equal to V_B, causing the attenuators' gains to be halfway between their fully on and fully off positions (−20 dB each). Monitoring the C_T voltage (with respect to V_B) is the most direct method of monitoring the circuit's mode.

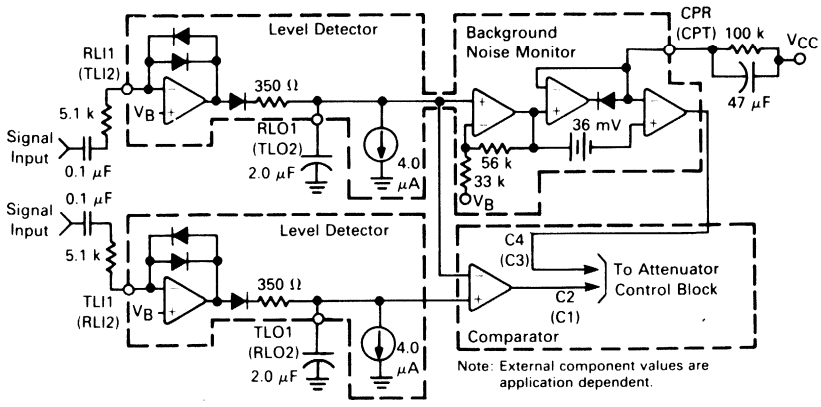
The inputs to the Control Block are seven: 2 from the comparators operated by the level detectors, 2 from the background noise monitors, the volume control, the dial-tone detector, and the AGC circuit. These seven inputs are described below.

LEVEL DETECTORS

There are four level detectors — two on the receive side and two on the transmit side. Refer to Figure 4 — the terms in parentheses form one system, and the other terms form the second system. Each level detector is a high gain amplifier with back-to-back diodes in the feedback path, resulting in non-linear gain, which permits operation over a wide dynamic range of speech levels. Refer to the graphs of Figures 11, 12 and 13 for their dc and ac transfer characteristics. The sensitivity of each level detector is determined by the external resistor and capacitor at each input (TLI1, TLI2, RLI1, and RLI2). Each output charges an external capacitor through a diode and limiting resistor, thus providing a dc representation of the input ac signal level. The outputs have a quick rise time (determined by the capacitor and an internal 350 Ω resistor), and a slow decay time set by an internal current source and the capacitor. The capacitors on the four outputs should have the same value (±10%) to prevent timing problems.

Referring to Figure 2, on the receive side, one level detector (RLI1) is at the receive input receiving the same

FIGURE 4 — LEVEL DETECTORS



signal as at Tip and Ring, and the other (RLI2) is at the output of the speaker amplifier. On the transmit side, one level detector (TLI2) is at the output of the microphone amplifier, while the other (TLI1) is at the hybrid output. Outputs RLO1 and TLO1 feed a comparator, the output of which goes to the Attenuator Control Block. Likewise, outputs RLO2 and TLO2 feed a second comparator which also goes to the Attenuator Control Block. The truth table for the effects of the level detectors on the Control Block is given in the section describing the Control Block.

BACKGROUND NOISE MONITORS

The purpose of the background noise monitors is to distinguish speech (which consists of bursts) from background noise (a relatively constant signal level). There are two background noise monitors — one for the receive path and one for the transmit path. Referring to Figure 4, the receive background noise monitor is operated on by the RLI1-RLO1 level detector, while the transmit background noise monitor is operated on by the TLI2-TLO2 level detector. They monitor the background noise by storing a dc voltage representative of the respective noise levels in capacitors at CPR and CPT. The voltages at these pins have slow rise times (determined by the external RC), but fast decay times. If the signal at RLI1 (or TLI2) changes slowly, the voltage at CPR (or CPT) will remain more positive than the voltage at the non-inverting input of the monitor's output comparator. When speech is present, the voltage on the non-inverting input of the comparator will rise quicker than the voltage at the inverting input (due to the burst characteristic of speech), causing its output to change. This output is sensed by the Attenuator Control Block.

The 36 mV offset at the comparator's input keeps the comparator from changing state unless the speech level exceeds the background noise by ≈4.0 dB. The time constant of the external RC (≈4.7 seconds) determines the response time to background noise variations.

VOLUME CONTROL

The volume control input at VLC (Pin 13) is sensed as a voltage with respect to V_B. The volume control affects the attenuators *only* in the receive mode. It has no effect in the idle or transmit modes.

When in the receive mode, the gain of the receive attenuator will be + 6.0 dB, and the gain of the transmit attenuator will be −46 dB only when VLC is equal to V_B. As VLC is reduced below V_B, the gain of the receive attenuator is reduced (see Figure 14), and the gain of the transmit attenuator is increased such that their sum remains constant. Changing the voltage at VLC changes the voltage at C_T (see the Attenuator Control Block section), which in turn controls the attenuators.

The volume control setting does not affect the maximum attenuator input signal at which noticeable distortion occurs.

The bias current at VLC is typically 60 nA out of the pin, and does not vary significantly with the VLC voltage or with V_{CC}.

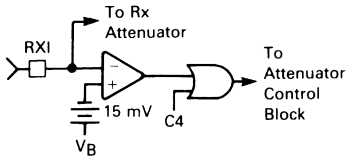
DIAL TONE DETECTOR

The dial tone detector is a comparator with one side connected to the receive input (RXI) and the other input connected to V_B with a 15 mV offset (see Figure 5). If the circuit is in the receive mode, and the incoming signal is greater than 15 mV (10 mVrms), the comparator's output will change, disabling the receive idle mode. The receive attenuator will then be at a setting determined solely by the volume control.

The purpose of this circuit is to prevent the dial tone

(which would be considered as continuous noise) from fading away as the circuit would have the tendency to switch to the idle mode. By disabling the receive idle mode, the dial tone remains at the normally expected full level.

FIGURE 5 — DIAL TONE DETECTOR



AGC

The AGC circuit affects the circuit only in the receive mode, and only when the supply voltage (V_{CC}) is less than 3.5 volts. As V_{CC} falls below 3.5 volts, the gain of the receive attenuator is reduced according to the graph of Figure 15. The transmit path attenuation changes such that the sum of the transmit and receive gains remains constant.

The purpose of this feature is to reduce the power (and current) used by the speaker when a line-powered speakerphone is connected to a long line, where the available power is limited. By reducing the speaker power, the voltage sag at V_{CC} is controlled, preventing possible erratic operation.

ATTENUATOR CONTROL BLOCK

The Attenuator Control Block has the seven inputs described above:

— The output of the comparator operated by RLO2 and TLO2 (microphone/speaker side) — designated C1.
— The output of the comparator operated by RLO1 and TLO1 (Tip/Ring side) — designated C2.
— The output of the transmit background noise monitor — designated C3.
— The output of the receive background noise monitor — designated C4.
— The volume control.
— The dial tone detector.
— The AGC circuit.

The single output of the Control Block controls the two attenuators. The effect of C1–C4 is as follows:

Inputs				Output
C1	C2	C3	C4	Mode
Tx	Tx	1	X	Transmit
Tx	Rx	y	y	Fast Idle
Rx	Tx	y	y	Fast Idle
Rx	Rx	X	1	Receive
Tx	Tx	0	X	Slow Idle
Tx	Rx	0	0	Slow Idle
Rx	Tx	0	0	Slow Idle
Rx	Rx	X	0	Slow Idle

X = Don't Care; y = C3 and C4 are not both 0.

A definition of the above terms:

1) "Transmit" means the transmit attenuator is fully on (+6.0 dB), and the receive attenuator is at max. attenuation (−46 dB).
2) "Receive" means both attenuators are controlled by the volume control. At max. volume, the receive attenuator is fully on (+6.0 dB), and the transmit attenuator is at max. attenuation (−46 dB).
3) "Fast Idle" means both transmit and receive speech are present in approximately equal levels. The attenuators are quickly switched (30 ms) to idle until one speech level dominates the other.
4) "Slow Idle" means speech has ceased in both transmit and receive paths. The attenuators are then slowly switched (1 second) to the idle mode.
5) Switching to the full transmit or receive modes from any other mode is at the fast rate (−30 ms).

A summary of the truth table is as follows:

1) The circuit will switch to transmit if: a) *both* transmit level detectors sense higher signal levels relative to the respective receive level detectors (TLI1 versus RLI1, TLI2 versus RLI2), *and* b) the transmit background noise monitor indicates the presence of speech.

2) The circuit will switch to receive if: a) *both* receive level detectors sense higher signal levels relative to the respective transmit level detectors, *and* b) the receive background noise monitor indicates the presence of speech.

3) The circuit will switch to the fast idle mode if the level detectors *disagree* on the relative strengths of the signal levels, *and* at least one of the background noise monitors indicates speech. For example, referring to the Block Diagram (Figure 2), if there is sufficient signal at the microphone amp output (TLI2) to override the speaker signal (RLI2), *and* there is sufficient signal at the receive input (RLI1) to override the signal at the hybrid output (TLI1), *and* either or both background monitors indicate speech, then the circuit will be in the fast idle mode. Two conditions which can cause the fast idle mode to occur are a) when both talkers are attempting to gain control of the system by talking at the same time, and b) when one talker is in a very noisy environment, forcing the other talker to continually override that noise level. In general, the fast idle mode will occur infrequently.

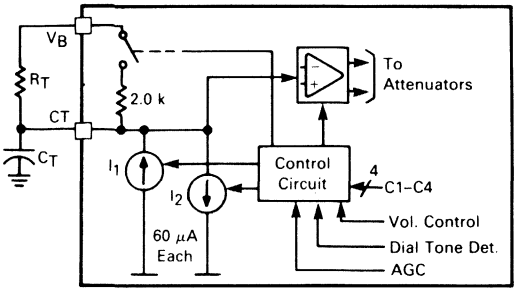
4) The circuit will switch to the slow idle mode when a) both talkers are quiet (no speech present), or b) when one talker's speech level is continuously overriden by noise at the other speaker's location.

The time required to switch the circuit between transmit, receive, fast idle and slow idle is determined in part by the components at the C_T pin (Pin 14). (See the section on Switching Times for a more complete explanation of the switching time components.) A schematic of the C_T circuitry is shown in Figure 6, and operates as follows:

— R_T is typically 120 kΩ, and C_T is typically 5.0 μF.
— To switch to the receive mode, I_1 is turned on (I_2 is off), charging the external capacitor to +240 mV above V_B. (An internal clamp prevents further charging of the capacitor.)
— To switch to the transmit mode, I_2 is turned on (I_1 is off) bringing down the voltage on the capacitor to −240 mV with respect to V_B.

— To switch to idle quickly (fast idle), the current sources are turned off, and the internal 2.0 kΩ resistor is switched in, discharging the capacitor to V_B with a time constant = 2.0 k x C_T.
— To switch to idle slowly (slow idle), the current sources are turned off, the switch at the 2.0 kΩ resistor is open, and the capacitor discharges to V_B through the external resistor R_T with a time constant = R_T x C_T.

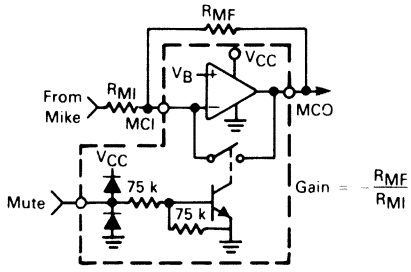
FIGURE 6 — CT ATTENUATOR CONTROL BLOCK CIRCUIT



MICROPHONE AMPLIFIER

The microphone amplifier (Pins 10, 11) has the non-inverting input internally connected to V_B, while the inverting input and the output are pinned out. Unlike most op-amps, the amplifier has an all-NPN output stage, which maximizes phase margin and gain-bandwidth. This feature ensures stability at gains less than unity, as well as with a wide range of reactive loads. The open loop gain is typically 80 dB (f <100 Hz), and the gain-bandwidth is typically 1.0 MHz (See Figure 16). The maximum p-p output swing is typically 1.0 volt less than V_{CC} with an output impedance of <10 Ω until current limiting is reached (typically 1.5 mA). Input bias current at MCI is typically 40 nA out of the pin.

FIGURE 7 — MICROPHONE AMPLIFIER AND MUTE



The muting function (Pin 12), when activated, will reduce the gain of the amplifier to ≈ −39 dB (with RMI = 5.1 kΩ) by shorting the output to the inverting input (see Figure 7). The mute input has a threshold of ≈1.5 volts, and the voltage at this pin must be kept within the range of ground and V_{CC} (see Figure 17). If the mute function is not used, the pin should be grounded.

HYBRID AMPLIFIERS

The two hybrid amplifiers (at HTO +, HTO −, and HTI), in conjunction with an external transformer, provide the two-to-four wire converter for interfacing to the telephone line. The gain of the first amplifier (HTI to HTO −) is set by external resistors (gain = $-R_{HF}/R_{HI}$ in Figure 2), and its output drives the second amplifier, the gain of which is internally set at −1.0. Unlike most op-amps, the amplifiers have an all-NPN output stage, which maximizes phase margin and gain-bandwidth. This feature ensures stability at gains less than unity, as well as with a wide range of reactive loads. The open loop gain of the first amplifier is typically 80 dB, and the gain bandwidth of each amplifier is ≈1.0 MHz (see Figure 16). The maximum p-p output swing of each amplifier is typically 1.2 volts less than V_{CC} with an output impedance of <10 Ω until current limiting is reached (typically 8.0 mA). The output current capability is guaranteed to be a minimum of 5.0 mA. The bias current at HTI is typically 30 nA out of the pin.

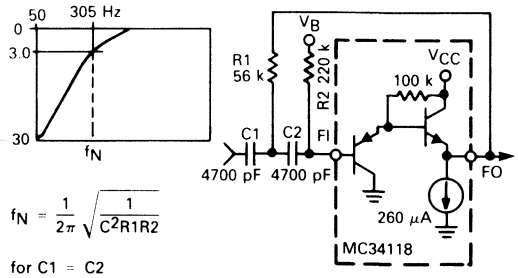
The connections to the coupling transformer are shown in the Block Diagram (Figure 2). The block labeled ZBal is the balancing network necessary to match the line impedance.

FILTER

The operation of the filter circuit is determined by the external components. The circuit within the MC34118, from pins FI to FO is a buffer with a high input impedance (>1.0 MΩ), and a low output impedance (<50 Ω). The configuration of the external components determines whether the circuit is a high-pass filter (as shown in Figure 2), a low-pass filter, or a band-pass filter.

As a high pass filter, with the components shown in Figure 8, the filter will keep out 60 Hz (and 120 Hz) hum which can be picked up by the external telephone lines.

FIGURE 8 — HIGH PASS FILTER



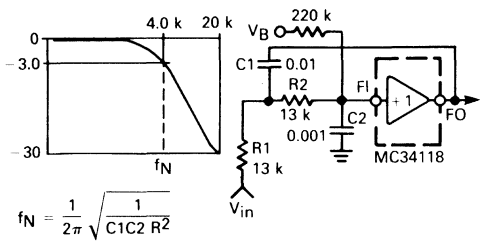
$f_N = \frac{1}{2\pi}\sqrt{\frac{1}{C^2R1R2}}$

for C1 = C2

As a low pass filter (Figure 9), it can be used to roll off the high end frequencies in the receive circuit, which aids in protecting against acoustic feedback problems.

With an appropriate choice of an input coupling capacitor to the low pass filter, a band pass filter is formed.

FIGURE 9 — LOW PASS FILTER



$$f_N = \frac{1}{2\pi}\sqrt{\frac{1}{C1C2\,R^2}}$$

for R1 = R2

POWER SUPPLY, V_B, AND CHIP DISABLE

The power supply voltage at V_{CC} (Pin 4) is to be between 3.5 and 6.5 volts for normal operation, with reduced operation possible down to 2.8 volts (see Figure 15 and the AGC section). The power supply current is shown in Figure 18 for both the power-up and power-down mode.

The output voltage at V_B (Pin 15) is $\approx(V_{CC} - 0.7)/2$, and provides the ac ground for the system. The output impedance at V_B is $\approx 400\ \Omega$ (see Figure 19), and in conjunction with the external capacitor at V_B, forms a low pass filter for power supply rejection. Figure 20 indicates the amount of rejection with different capacitors. The choice of capacitor is application dependent based on whether the circuit is powered by the telephone line or a power supply.

Since V_B biases the microphone and hybrid amplifiers, the amount of supply rejection at their outputs is directly related to the rejection at V_B, as well as their respective gains. Figure 21 depicts this graphically.

The Chip Disable (Pin 3) permits powering down the IC to conserve power and/or for muting purposes. With CD $\leq$0.8 volts, normal operation is in effect. With CD $\geq$2.0 volts and $\leq V_{CC}$, the IC is powered down. In the powered down mode, the microphone and the hybrid amplifiers are disabled, and their outputs go to a high impedance state. Additionally, the bias is removed from the level detectors. The bias is not removed from the filter (Pins 1, 2), the attenuators (Pins 8, 9, 21, 22), or from Pins 13, 14, and 15 (the attenuators are disabled, however, and will not pass a signal). The input impedance at CD is typically 90 kΩ, has a threshold of $\approx$1.5 volts, and the voltage at this pin must be kept within the range of ground and V_{CC} (see Figure 17). If CD is not used, the pin should be grounded.

FIGURE 10 — ATTENUATOR GAIN versus V_{CT} (PIN 14)

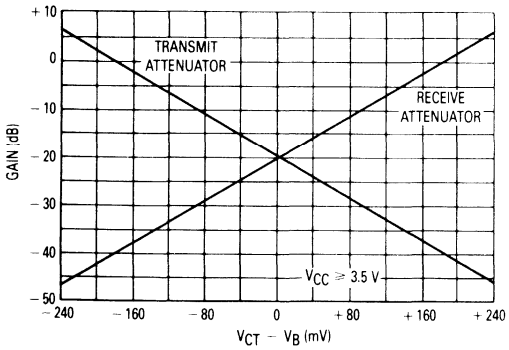


FIGURE 11 — LEVEL DETECTOR DC TRANSFER CHARACTERISTICS

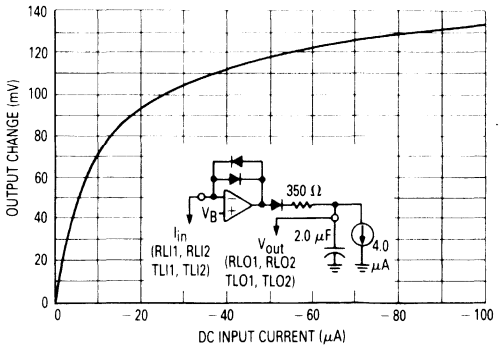


FIGURE 12 — LEVEL DETECTOR AC TRANSFER CHARACTERISTICS

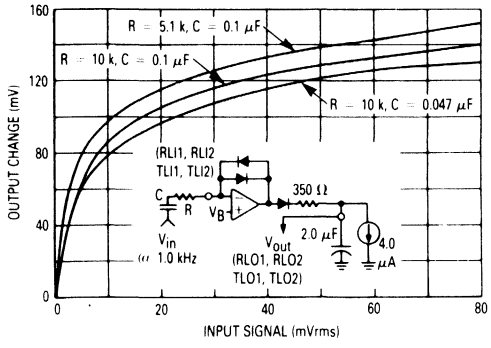


FIGURE 13 — LEVEL DETECTOR AC TRANSFER CHARACTERISTICS versus FREQUENCY

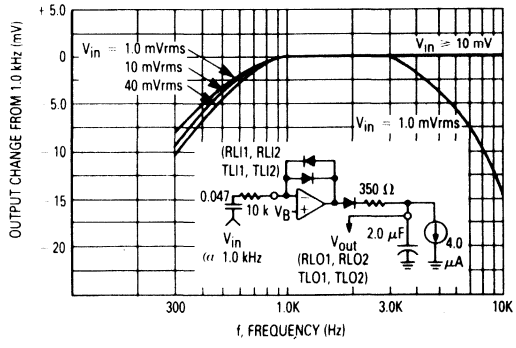


FIGURE 14 — RECEIVE ATTENUATOR versus VOLUME CONTROL

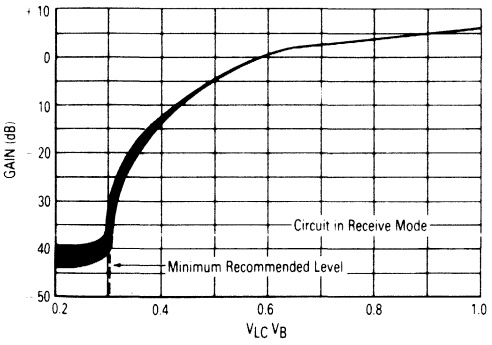


FIGURE 15 — RECEIVE ATTENUATION GAIN versus V_{CC}

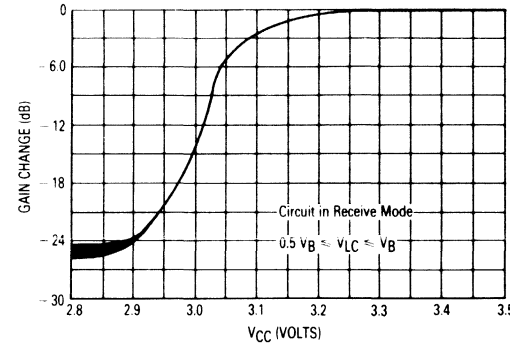


FIGURE 16 — MICROPHONE AMPLIFIER AND 1ST HYBRID AMPLIFIER OPEN LOOP GAIN AND PHASE

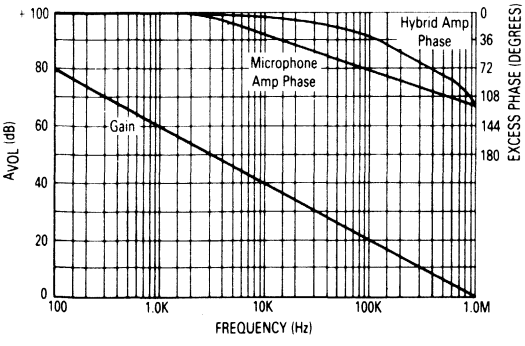
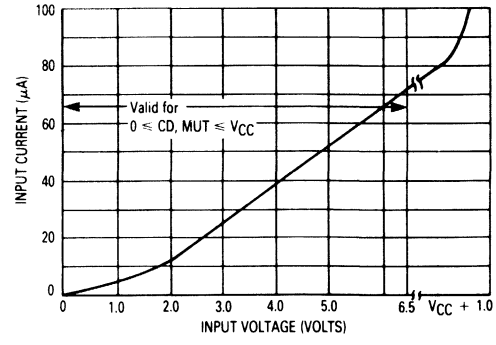


FIGURE 17 — INPUT CHARACTERISTICS @ CD, MUT



3

FIGURE 18 — SUPPLY CURRENT versus SUPPLY VOLTAGE

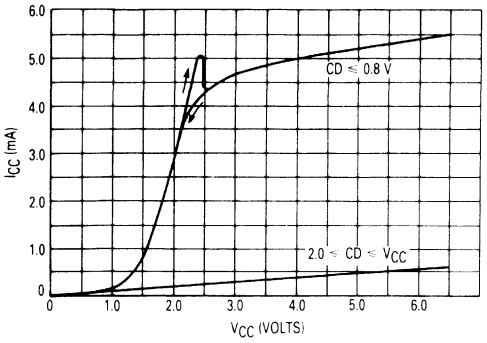


FIGURE 19 — V_B OUTPUT CHARACTERISTICS

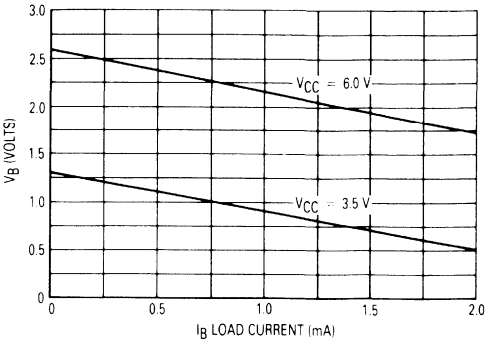


FIGURE 20 — V_B POWER SUPPLY REJECTION versus FREQUENCY AND V_B CAPACITOR

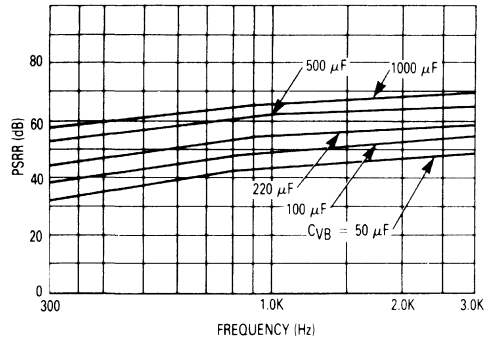


FIGURE 21 — POWER SUPPLY REJECTION OF THE MICROPHONE AND HYBRID AMPLIFIERS

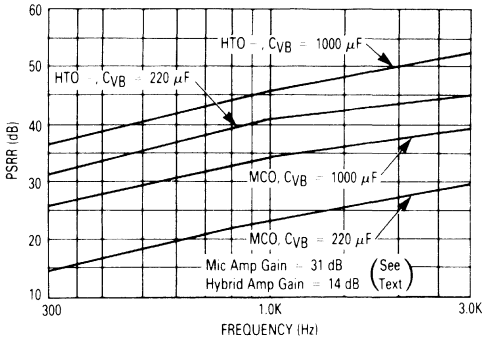
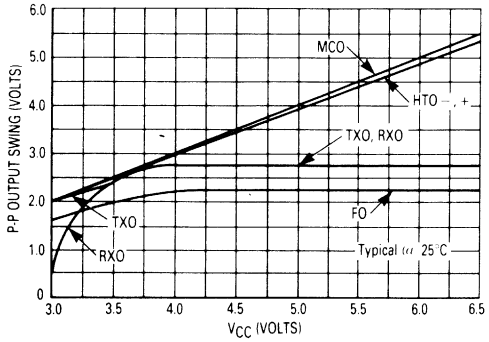


FIGURE 22 — TYPICAL OUTPUT SWING versus V_{CC}



DESIGN GUIDELINES

SWITCHING TIME

The switching time of the MC34118 circuit is dominated by the components at C_T (Pin 14, refer to Figure 6), and secondarily by the capacitors at the level detector outputs (RLO1, RLO2, TLO1, TLO2).

The time to switch to receive or to transmit from idle is determined by the capacitor at C_T, together with the internal current sources (refer to Figure 6). The switching time is:

$$\Delta T = \frac{\Delta V \times C_T}{I}$$

For the typical case where ΔV = 240 mV, I = 60 μA, and C_T is 5.0 μF, ΔT = 20 ms. If the circuit switches directly from receive to transmit (or vice-versa), the total switching time would be 40 ms.

The switching time from either receive or transmit to idle depends on which type of idle mode is in effect. If the circuit is going to "fast idle," the time constant is determined by the C_T capacitor, and the internal 2.0 kΩ resistor (Figure 6). With C_T = 5.0 μF, the time constant is ≈10 ms, giving a switching time to idle of ≈30 ms (for 95% change). Fast idle is an infrequent occurrence, however, occurring when both speakers are talking and competing for control of the circuit. The switching time from idle back to either transmit or receive is described above.

If the circuit is switching to "slow idle," the time constant is determined by the C_T capacitor and R_T, the external resistor (see Figure 6). With C_T = 5.0 μF, and R_T = 120 kΩ, the time constant is ≈600 ms, giving a switching time of ≈1.8 seconds (for 95% change). The switching period to slow idle begins when both speakers have stopped talking. The switching time back to the original mode will depend on how soon that speaker begins speaking again. The sooner the speaking starts during the 1.8 second period, the quicker the switching time since a smaller voltage excursion is required. That switching time is determined by the internal current sources as described above.

The above switching times occur, however, after the level detectors have detected the appropriate signal levels, since their outputs operate the Attenuator Control Block. Referring to Figure 4, the rise time of the level detectors' outputs to new speech is quick by comparison (≈1.0 ms), determined by the internal 350 Ω resistor and the external capacitor (typically 2.0 μF). The output's decay time is determined by the external capacitor, and an internal 4.0 μA current source giving a decay rate of ≈60 ms for a 120 mV excursion at RLO or TLO. However, the overall response time of the circuit is not a constant since it depends on the relative strength of the signals at the different level detectors, as well as the timing of the signals with respect to each other. The capacitors at the four outputs (RLO1, RLO2, TLO1, TLO2) must be equal value (±10%) to prevent problems in timing and level response.

The rise time of the level detector's outputs is not significant since it is so short. The decay time, however, provides a significant part of the "hold time" necessary to hold the circuit during the normal pauses in speech.

The components at the inputs of the level detectors (RLI1, RLI2, TLI1, TLI2) do not affect the switching time, but rather affect the relative signal levels required to switch the circuit, as well as the frequency response of the detectors.

DESIGN EQUATIONS

Referring to Figure 24 (the coupling capacitors have been omitted for simplicity), and the circuit of Figure 23, the following definitions will be used (all measurements are at 1.0 kHz):

- G_{MA} is the gain of the microphone amplifier measured from the microphone output to TXI (typically 35 V/V, or 31 dB);
- G_{TX} is the gain of the transmit attenuator, measured from TXI to TXO;
- G_{HA} is the gain of hybrid amplifiers, measured from TXO to the HTO − /HTO + differential output (typically 10.2 V/V, or 20.1 dB);
- G_{HT} is the gain from HTO − /HTO + to Tip/Ring for transmit signals, and includes the balance network (measured at 0.4 V/V, or − 8.0 dB);
- G_{ST} is the sidetone gain, measured from HTO − / HTO + to the filter input (measured at 0.18 V/V, or − 15 dB);
- G_{HR} is the gain from Tip/Ring to the filter input for receive signals (measured at 0.833 V/V or − 1.6 dB);
- G_{FO} is the gain of the filter stage, measured from the input of the filter to RXI, typically 0 dB at 1.0 kHz;
- G_{RX} is the gain of the receive attenuator measured from RXI to RXO;
- G_{SA} is the gain of the speaker amplifier, measured from RXO to the differential output of the MC34119 (typically 22 V/V or 26.8 dB);
- G_{AC} is the acoustic coupling, measured from the speaker differential voltage to the microphone output voltage.

I) Transmit Gain

The transmit gain, from the microphone output (V_M) to Tip and Ring, is determined by the output characteristics of the microphone, and the desired transmit level. For example, a typical electret microphone will produce ≈0.35 mVrms under normal speech conditions. To achieve 100 mVrms at Tip/Ring, an overall gain of 285 V/V is necessary. The gain of the transmit attenuator is fixed at 2.0 (+ 6.0 dB), and the gain through the hybrid of Figure 23 (G_{HT}) is nominally 0.4 (− 8.0 dB). Therefore a gain of 357 V/V is required of the microphone and hybrid amplifiers. It is desirable to have the majority of that gain in the microphone amplifier for three reasons: 1) the low level signals from the microphone should be amplified as soon as possible to minimize signal/noise

3

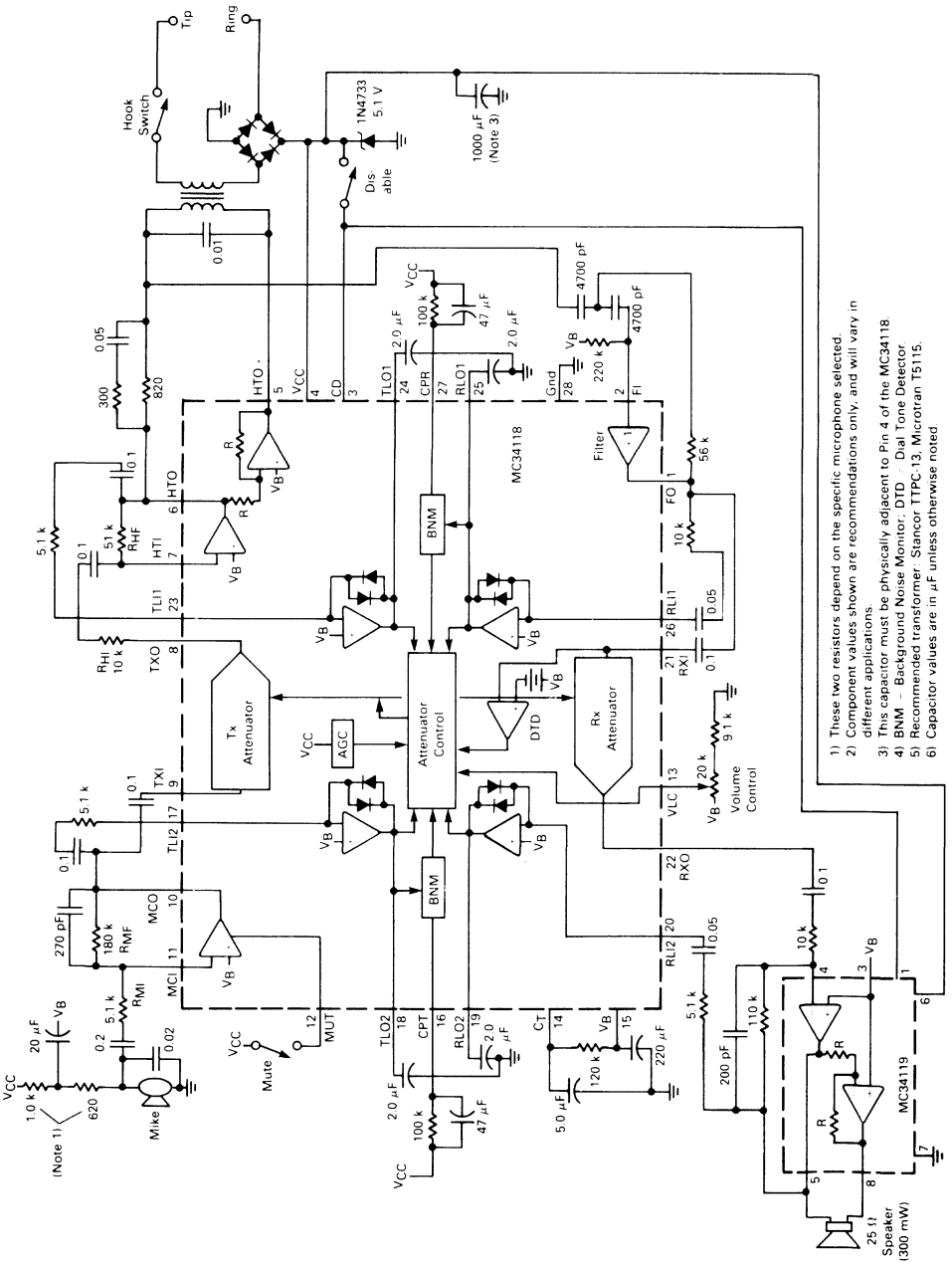
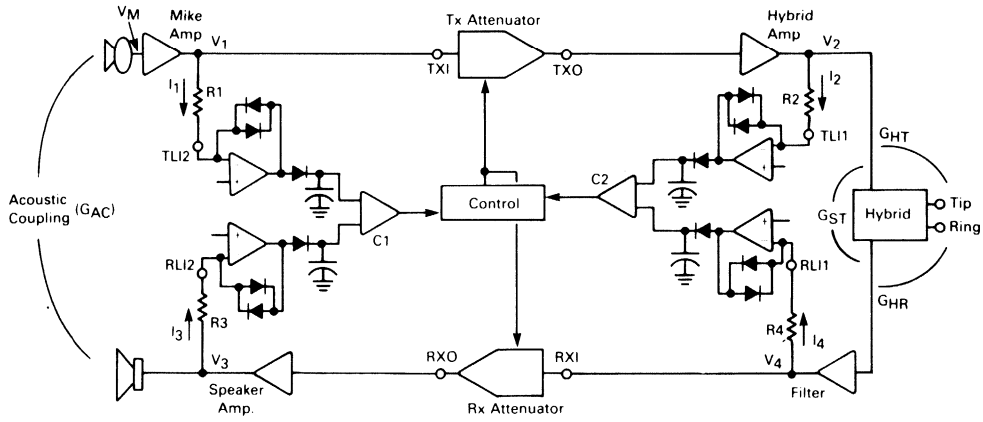


FIGURE 23 — MC34118 APPLICATION CIRCUIT (BASIC LINE POWERED SPEAKERPHONE)

FIGURE 24 — BASIC BLOCK DIAGRAM FOR DESIGN PURPOSES



problems; 2) to provide a reasonable signal level to the TLI2 level detector; and 3) to minimize any gain applied to broadband noise generated within the attenuator. However, to cover the normal voiceband, the microphone amplifier's gain should not exceed 48 dB (see Figure 16). For the circuit of Figure 23, the gain of the microphone amplifier was set at 35 V/V (31 dB), and the differential gain of the hybrid amplifiers was set at 10.2 V/V (20.1 dB).

II) Receive Gain

The overall receive gain depends on the incoming signal level, and the desired output power at the speaker. Nominal receive levels (independent of the peaks) at Tip/Ring can be 35 mVrms (−27 dBm), although on long lines that level can be down to 8.0 mVrms (−40 dBm). The speaker power is:

$$P_{SPK} = \frac{10^{dBm/10} \times 0.6}{R_S} \qquad \text{(Equation 1)}$$

where R_S is the speaker impedance, and the dBm term is the incoming signal level increased by the gain of the receive path. Experience has shown that ≈30 dB gain is a satisfactory amount for the majority of applications. Using the above numbers and Equation 1, it would appear that the resulting power to the speaker is extremely low. However, Equation 1 does not consider the peaks in normal speech, which can be 10 to 15 times the rms value. Considering the peaks, the overall average power approaches 20–30 mW on long lines, and much more on short lines.

Referring to Figure 23, the gain from Tip/Ring to the filter input was measured at 0.833 V/V (−1.6 dB), the filter's gain is unity, and the receive attenuator's gain is 2.0 V/V (+6.0 dB) at maximum volume. The speaker amplifier's gain is set at 22 V/V (26.8 dB), which puts the overall gain at ≈31.2 dB.

III) Loop Gain

The total loop gain (of Figure 24) must add up to less than zero dB to obtain a stable circuit. This can be expressed as:

$$G_{MA} + G_{TX} + G_{HA} + G_{ST} + G_{FO} + G_{RX} + G_{SA} + G_{AC} < 0 \qquad \text{(Equation 2)}$$

Using the typical numbers mentioned above, and knowing that $G_{TX} + G_{RX} = -40$ dB, the required acoustic coupling can be determined:

$$G_{AC} < -[31 + 20.1 + (-15) + 0 + (-40) + 26.8] = -22.9 \text{ dB.} \qquad \text{(Equation 3)}$$

An acoustic loss of at least 23 dB is necessary to prevent instability and oscillations, commonly referred to as "singing." However, the following equations show that greater acoustic loss is necessary to obtain proper level detection and switching.

IV) Switching Thresholds

To switch comparator C1, currents I_1 and I_3 need to be determined. Referring to Figure 24, with a receive signal V_L applied to Tip/Ring, a current I_3 will flow through R3 into RLI2 according to the following equation:

$$I_3 = \frac{V_L}{R3}\left[G_{HR} \times G_{FO} \times G_{RX} \times \frac{G_{SA}}{2}\right] \qquad \text{(Equation 4)}$$

where the terms in the brackets are the V/V gain terms. The speaker amplifier gain is divided by two since G_{SA} is the differential gain of the amplifier, and V_3 is obtained from one side of that output. The current I_1, coming from the microphone circuit, is defined by:

$$I_1 = \frac{V_M \times G_{MA}}{R1} \quad \text{(Equation 5)}$$

where V_M is the microphone voltage. Since the switching threshold occurs when $I_1 = I_3$, combining the above two equations yields:

$$V_M = V_L \times \frac{R1}{R3} \frac{[G_{HR} \times G_{FO} \times G_{RX} \times G_{SA}]}{G_{MA} \times 2} \quad \text{(Equation 6)}$$

This is the general equation defining the microphone voltage necessary to switch comparator C1 when a receive signal V_L is present. The highest V_M occurs when the receive attenuator is at maximum gain (+6.0 dB). Using the typical numbers for Equation 6 yields:

$$V_M = 0.52\ V_L \quad \text{(Equation 7)}$$

To switch comparator C2, currents I_2 and I_4 need to be determined. With sound applied to the microphone, a voltage V_M is created by the microphone, resulting in a current I_2 into TLI1:

$$I_2 = \frac{V_M}{R2}\left[G_{MA} \times G_{TX} \times \frac{G_{HA}}{2}\right] \quad \text{(Equation 8)}$$

Since G_{HA} is the differential gain of the hybrid amplifiers, it is divided by two to obtain the voltage V_2 applied to R2. Comparator C2 switches when $I_4 = I_2$. I_4 is defined by:

$$I_4 = \frac{V_L}{R4}[G_{HR} \times G_{FO}] \quad \text{(Equation 9)}$$

Setting $I_4 = I_2$, and combining the above equations results in:

$$V_L = V_M \times \frac{R4}{R2} \times \frac{[G_{MA} \times G_{TX} \times G_{HA}]}{[G_{HR} \times G_{FO} \times 2]} \quad \text{(Equation 10)}$$

This equation defines the line voltage at Tip/Ring necessary to switch comparator C2 in the presence of a microphone voltage. The highest V_L occurs when the circuit is in the transmit mode (G_{TX} = +6.0 dB). Using the typical numbers for Equation 10 yields:

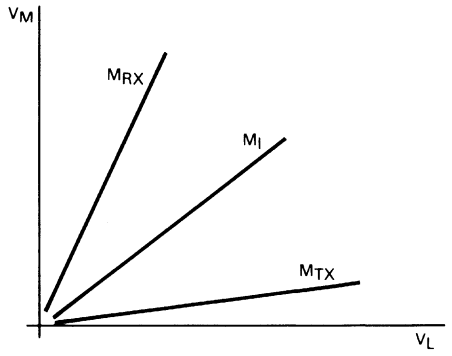
$$V_L = 840\ V_M \quad (\text{or } V_M = 0.0019\ V_L) \quad \text{(Equation 11)}$$

At idle, where the gain of the two attenuators is −20 dB (0.1 V/V), Equations 6 and 10 yield the same result:

$$V_M = 0.024\ V_L \quad \text{(Equation 12)}$$

Equations 7, 11, and 12 define the thresholds for switching, and are represented in the following graph:

FIGURE 25 — SWITCHING THRESHOLDS



The "M" terms are the slopes of the lines (0.52, 0.024, and 0.0019) which are the coefficients of the three equations. The M_{RX} line represents the receive to transmit threshold in that it defines the microphone signal level necessary to switch to transmit in the presence of a given receive signal level. The M_{TX} line represents the transmit to receive threshold. The M_I line represents the idle condition, and defines the threshold level on one side (transmit or receive) necessary to overcome noise on the other.

Some comments on the above graph:

— Acoustic coupling and sidetone coupling were not included in Equations 7 and 12. Those couplings will affect the actual performance of the final speakerphone due to their interaction with speech at the microphone, and the receive signal coming in at Tip/Ring. The effects of those couplings are difficult to predict due to their associated phase shifts and frequency response. In some cases the coupling signal will add, and other times subtract from the incoming signal. The physical design of the speakerphone enclosure, as well as the specific phone line to which it is connected, will affect the acoustic and sidetone couplings, respectively.

— The M_{RX} line helps define the maximum acoustic coupling allowed in a system, which can be found from the following equation:

$$G_{AC\text{-}MAX} = \frac{R1}{2 \times R3 \times G_{MA}} \quad \text{(Equation 13)}$$

Equation 13 is independent of the volume control setting. Conversely, the acoustic coupling of a designed system helps determine the minimum slope of that line. Using the component values of Figure 23 in Equation

13 yields a $G_{AC\text{-}MAX}$ of −37 dB. Experience has shown, however, that an acoustic coupling loss of >40 dB is desirable.

— The M_{TX} line helps define the maximum sidetone coupling (G_{ST}) allowed in the system, which can be found from the following equation:

$$G_{ST} = \frac{R4}{2 \times R2 \times G_{FO}} \qquad \text{(Equation 14)}$$

Using the component values of Figure 23 in Equation 14 yields a maximum sidetone of 0 dB. Experience has shown, however, that a minimum of 6.0 dB loss is preferable.

The above equations can be used to determine the resistor values for the level detector inputs. Equation 6 can be used to determine the R1 R3 ratio, and Equation 10 can be used to determine the R4 R2 ratio. In Figure 24, R1–R4 each represent the combined impedance of the resistor and coupling capacitor at each level detector input. The magnitude of each RC's impedance should be kept within the range of 2.0 k–15 kΩ in the voiceband (due to the typical signal levels present) to obtain the best performance from the level detectors. The specific R and C at each location will determine the frequency response of that level detector.

APPLICATION INFORMATION

DIAL TONE DETECTOR

The threshold for the dial tone detector is internally set at 15 mV (10 mVrms) below V_B (see Figure 5). That threshold can be reduced by connecting a resistor from RXI to ground. The resistor value is calculated from:

$$R = 10\text{ k}\left[\frac{V_B}{\Delta V} - 1\right]$$

where V_B is the voltage at Pin 15, and ΔV is the amount of threshold reduction. By connecting a resistor from V_{CC} to RXI, the threshold can be increased. The resistor value is calculated from:

$$R = 10\text{ k}\left[\frac{V_{CC} - V_B}{\Delta V} - 1\right]$$

where ΔV is the amount of the threshold increase.

BACKGROUND NOISE MONITORS

For testing or circuit analysis purposes, the transmit or receive attenuators can be set to the "on" position, by disabling the background noise monitors, and applying a signal so as to activate the level detectors. Grounding the CPR pin will disable the receive background noise monitor, thereby indicating the "presence of speech" to the attenuator control block. Grounding CPT does the same for the transmit path.

Additionally, the receive background noise monitor is automatically disabled by the dial tone detector whenever the receive signal exceeds the detector's threshold.

TRANSMIT/RECEIVE DETECTION PRIORITY

Although the MC34118 was designed to have an idle mode such that the attenuators are halfway between their full on and full off positions, the idle mode can be biased towards the transmit or the receive side. With this done, gaining control of the circuit from idle will be easier for that side towards which it is biased since that path will have less attenuation at idle.

By connecting a resistor from C_T (Pin 14) to ground, the circuit will be biased towards the transmit side. The resistor value is calculated from:

$$R = R_T\left[\frac{V_B}{\Delta V} - 1\right]$$

where R is the added resistor, R_T is the resistor normally between Pins 14 and 15 (typically 120 kΩ), and ΔV is the difference between V_B and the voltage at C_T at idle (refer to Figure 10).

By connecting a resistor from C_T (Pin 14) to V_{CC}, the circuit will be biased towards the receive side. The resistor value is calculated from:

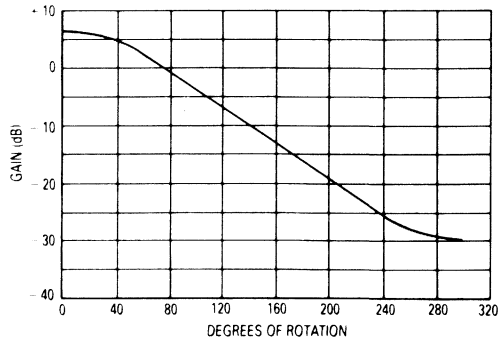
$$R = R_T\left[\frac{V_{CC} - V_B}{\Delta V} - 1\right]$$

R, R_T, and ΔV are the same as above. Switching time will be somewhat affected in each case due to the different voltage excursions required to get to transmit and receive from idle. For practical considerations, the ΔV shift should not exceed 100 mV.

VOLUME CONTROL

If a potentiometer with a standard linear taper is used for the volume control, the graph of Figure 14 indicates that the receive gain will not vary in a linear manner with respect to the pot's position. In situations where this may be objectionable, a potentiometer with an audio taper (commonly used in radio volume controls) will provide a more linear relationship as indicated in Figure 26. The slight non-linearity at each end of the graph is due to the physical construction of the potentiometer, and will vary among different manufacturers.

FIGURE 26 — RECEIVE ATTENUATOR GAIN versus POTENTIOMETER POSITION USING AUDIO TAPER



APPLICATION CIRCUIT

The circuit of Figure 23 is a basic speakerphone, to be used in parallel with any other telephone which con-

tains the ringer, dialer, and handset functions. The circuit is powered entirely by the telephone line's loop current, and its characteristics are shown in Figures 27–30.

FIGURE 27 — DC V-I CHARACTERISTICS

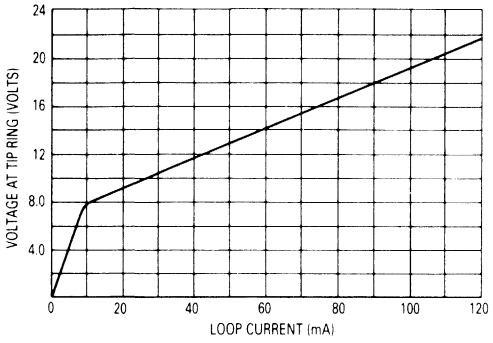


FIGURE 28 — AC TERMINATION IMPEDANCE

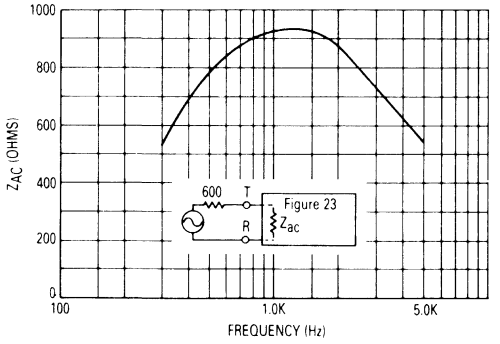


FIGURE 29 — TRANSMIT GAIN — MICROPHONE TO TIP/RING

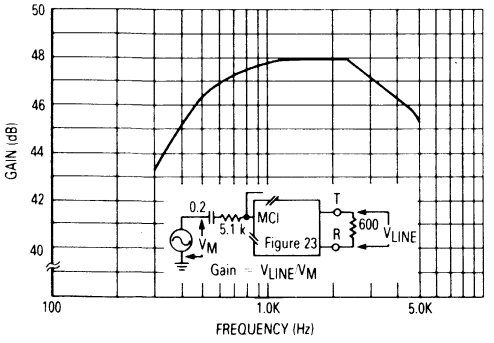


FIGURE 30 — RECEIVE GAIN

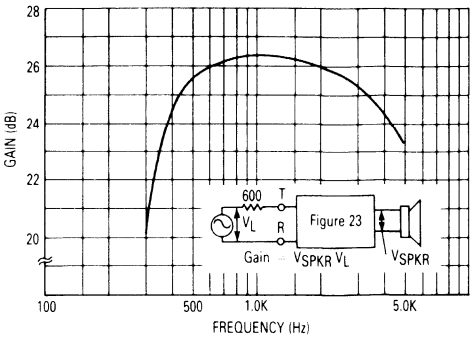
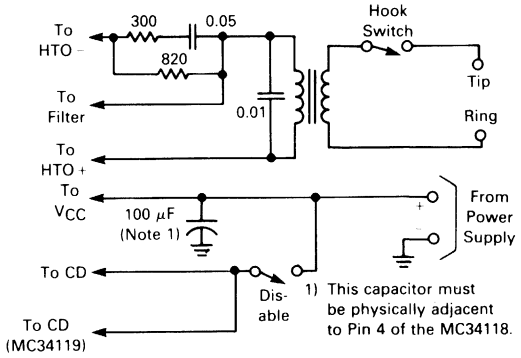


Figure 31 shows how the same circuit can be configured to be powered from a 3.5–6.0 volt power supply rather than the phone line.

FIGURE 31 — OPERATING FROM A POWER SUPPLY



ADDING A DIALER

Figure 32 shows the addition of a dialer to the circuit of Figure 23, with the additional components shown in bold. The MC145412 pulse/tone dialer is shown configured for DTMF operation. The DTMF output (Pin 18) is fed to the hybrid amplifiers at HTI, and the DTMF levels at Tip/Ring are adjusted by varying the 39 kΩ resistor. The Mute Output (active low at Pin 11) mutes the microphone amplifier, and attenuates the DTMF signals in the receive path (by means of the 10 k/3.0 k divider). The MC34118 is forced into the fast idle mode during dialing. The 3.0 volt battery provides for memory retention of the dialer's 10 number storage when the circuit is unpowered.

RFI INTERFERENCE

Potential radio frequency interference problems should be addressed early in the electrical and mechanical design of the speakerphone. RFI may enter the cir-

cuit through Tip and Ring, through the microphone wiring to the microphone amplifier, or through any of the PC board traces. The most sensitive pins on the MC34118 are the inputs to the level detectors (RLI1, RLI2, TLI1, TLI2) since, when there is no speech present, the inputs are high impedance and these op amps are in a near open loop condition. The board traces to these pins should be kept short, and the resistor and capacitor for each of these pins should be physically close to the pins. Any other high impedance input pin (MCI, HTI, FI, VLC) should be considered sensitive to RFI signals.

IN THE FINAL ANALYSIS . . .

Proper operation of a speakerphone is a combination of proper mechanical (acoustic) design as well as proper electronic design. The acoustics of the enclosure must be considered early in the design of a speakerphone. In general, electronics cannot compensate for poor acoustics, low speaker quality, or any combination of the two. Proper acoustic separation of the speaker and microphone, as described in the Design Equations, is essential. The physical location of the microphone, along with the characteristics of the selected microphone, will play a large role in the quality of the transmitted sound. The microphone and speaker vendors can usually provide additional information on the use of their products.

In the final analysis, the circuits shown in this data sheet will have to be "fine tuned" to match the acoustics of the enclosure, the specific hybrid, and the specific microphone and speaker selected. The component values shown in this data sheet should be considered as starting points only. The gains of the transmit and receive paths are easily adjusted at the microphone and speaker amplifiers, respectively. The switching response can then be fine tuned by varying (in small steps) the components at the level detector inputs until satisfactory operation is obtained for both long and short lines.

SUGGESTED VENDORS

Microphones

Primo Microphones Inc.
Bensenville, IL 60106
312-595-1022
Model EM-60

MURA Corp.
Westbury, N.Y. 11590
516-935-3640
Model EC-983-7

Hosiden America Corp.
Elk Grove Village, IL 60007
312-981-1144
Model KUC2123

25 Ω Speakers

Panasonic Industrial Co.
Seacaucus, N.J. 07094
201-348-5233
Model EAS-45P19S

Telecom Transformers

Microtran Co., Inc.
Valley Stream, N.Y. 11528
516-561-6050
Various models — ask for catalog and Application Bulletin F232

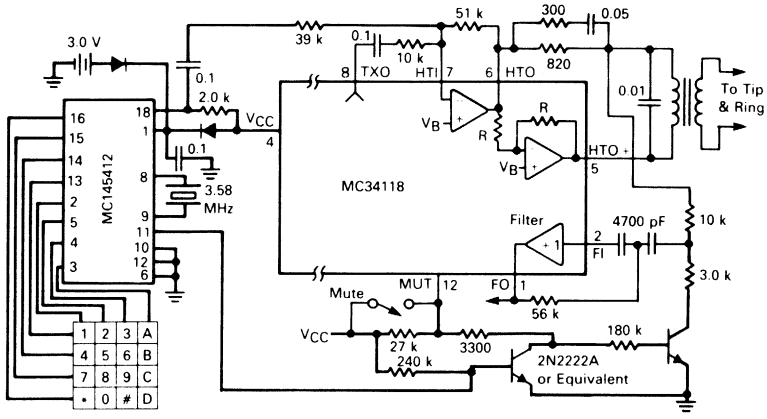
Stancor Products
Logansport, IN 46947
219-722-2244
Various models — ask for catalog

PREM Magnetics, Inc.
McHenry, IL 60050
815-385-2700
Various models — ask for catalog

Onan Power/Electronics
Minneapolis, MN 55437
612-921-5600
Model TC 38-6

Motorola Inc. does not endorse or warrant the suppliers referenced.

FIGURE 32 — ADDING A DIALER TO THE SPEAKERPHONE



MOTOROLA

MC34119

Advance Information

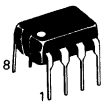
LOW POWER AUDIO AMPLIFIER

The MC34119 is a low power audio amplifier integrated circuit intended (primarily) for telephone applications, such as in speakerphones. It provides differential speaker outputs to maximize output swing at low supply voltages (2.0 volts minimum). Coupling capacitors to the speaker are not required. Open loop gain is 80 dB, and the closed loop gain is set with two external resistors. A Chip Disable pin permits powering down and/or muting the input signal. The MC34119 is available in a standard 8-pin DIP or a surface mount package.

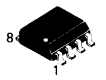
- Wide Operating Supply Voltage Range (2–16 volts) — Allows Telephone Line Powered Applications
- Low Quiescent Supply Current (2.7 mA Typical) for Battery Powered Applications
- Chip Disable Input to Power Down the IC
- Low Power-Down Quiescent Current (65 μA Typical)
- Drives a Wide Range of Speaker Loads (8–100 Ohms)
- Output Power Exceeds 250 mW with 32 Ohm Speaker
- Low Total Harmonic Distortion (0.5% Typical)
- Gain Adjustable from <0 dB to >46 dB for Voice Band
- Requires Few External Components

LOW POWER AUDIO AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

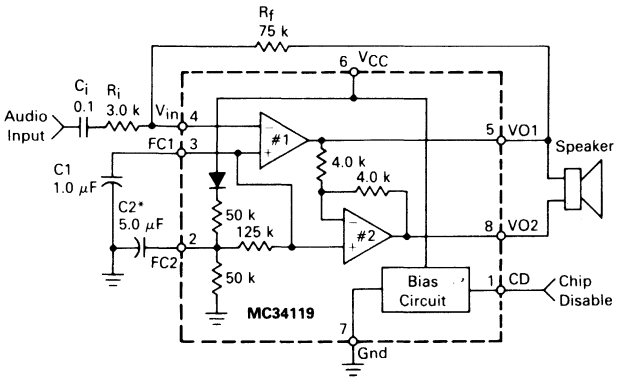


P SUFFIX
PLASTIC PACKAGE
CASE 626-04



D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8

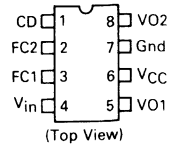
BLOCK DIAGRAM AND TYPICAL APPLICATION CIRCUIT



* = Optional

Differential Gain = $2 \times \frac{R_f}{R_i}$

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION	
MC34119P	Plastic DIP
MC34119D	SO8 Plastic DIP

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ADI1367

ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Units
Supply Voltage	− 1.0 to + 18	Vdc
Maximum Output Current at VO1, VO2	± 250	mA
Maximum Voltage @ V_{in}, FC1, FC2, CD	− 1.0, V_{CC} + 1.0	Vdc
Applied Output Voltage to VO1, VO2 when disabled	− 1.0, V_{CC} + 1.0	Vdc
Junction Temperature	− 55, + 140	°C

Devices should not be operated at these values. The "Recommended Operating Limits" provide for actual device operation.

RECOMMENDED OPERATING LIMITS

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	V_{CC}	+ 2.0	—	+ 16	Vdc
Load Impedance	R_L	8.0	—	100	Ω
Peak Load Current	I_L	—	—	± 200	mA
Differential Gain (5.0 kHz bandwidth)	AVD	0	—	46	dB
Voltage @ CD (Pin 1)	VCD	0	—	V_{CC}	Vdc
Ambient Temperature	T_A	0	—	+ 70	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristics	Symbol	Min	Typ	Max	Units
AMPLIFIERS (AC CHARACTERISTICS)					
AC Input Resistance (@ V_{in})	r_i	—	>30	—	MΩ
Open Loop Gain (Amplifier #1, f < 100 Hz)	A_{VOL1}	80	—	—	dB
Closed Loop Gain (Amplifier #2) (V_{CC} = 6.0 V, f = 1.0 kHz, R_L = 32 Ω)	A_{V2}	− 0.35	0	+ 0.35	dB
Gain Bandwidth Product	GBW	—	1.5	—	MHz
Output Power, V_{CC} = 3.0 V, R_L = 16 Ω, THD ≤ 10% V_{CC} = 6.0 V, R_L = 32 Ω, THD ≤ 10% V_{CC} = 12 V, R_L = 100 Ω, THD ≤ 10%	P_{out3} P_{out6} P_{out12}	55 250 400	— — —	— — —	mW
Total Harmonic Distortion (f = 1.0 kHz) (V_{CC} = 6.0 V, R_L = 32 Ω, P_{out} = 125 mW) (V_{CC} ≥ 3.0 V, R_L = 8.0 Ω, P_{out} = 20 mW) (V_{CC} ≥ 12 V, R_L = 32 Ω, P_{out} = 200 mW)	THD	— — —	0.5 0.5 0.6	1.0 — —	%
Power Supply Rejection (V_{CC} = 6.0 V, ΔVCC = 3.0 V) (C1 = ∞, C2 = 0.01 μF) (C1 = 0.1 μF, C2 = 0, f = 1.0 kHz) (C1 = 1.0 μF, C2 = 5.0 μF, f = 1.0 kHz)	PSRR	50 — —	— 12 52	— — —	dB
Muting (V_{CC} = 6.0 V, 1.0 kHz ≤ f ≤ 20 kHz, CD = 2.0 V)	GMT	—	>70	—	dB
AMPLIFIERS (DC CHARACTERISTICS)					
Output DC Level @ VO1, VO2, V_{CC} = 3.0 V, R_L = 16 Ω (R_f = 75 k) V_{CC} = 6.0 V V_{CC} = 12 V	VO(3) VO(6) VO(12)	1.0 — —	1.15 2.65 5.65	1.25 — —	Vdc
Output High Level (I_{out} = − 75 mA, 2.0 V ≤ V_{CC} ≤ 16 V)	V_{OH}	—	V_{CC} − 1.0	—	Vdc
Output Low Level (I_{out} = 75 mA, 2.0 V ≤ V_{CC} ≤ 16 V)	V_{OL}	—	0.16	—	Vdc
Output DC Offset Voltage (VO1–VO2) (V_{CC} = 6.0 V, R_f = 75 kΩ, R_L = 32 Ω)	ΔV_O	− 30	0	+ 30	mV
Input Bias Current @ V_{in} (V_{CC} = 6.0 V)	I_{IB}	—	− 100	− 200	nA
Equivalent Resistance @ FC1 (V_{CC} = 6.0 V)	R_{FC1}	100	150	220	kΩ
Equivalent Resistance @ FC2 (V_{CC} = 6.0 V)	R_{FC2}	18	25	40	kΩ
CHIP DISABLE (Pin 1)					
Input Voltage — Low	V_{IL}	—	—	0.8	Vdc
Input Voltage — High	V_{IH}	2.0	—	—	Vdc
Input Resistance (V_{CC} = V_{CD} = 16 V)	R_{CD}	50	90	175	kΩ
POWER SUPPLY					
Power Supply Current (V_{CC} = 3.0 V, R_L = ∞, CD = 0.8 V) (V_{CC} = 16 V, R_L = ∞, CD = 0.8 V) (V_{CC} = 3.0 V, R_L = ∞, CD = 2.0 V)	I_{CC3} I_{CC16} I_{CCD}	— — —	2.7 3.3 65	4.0 5.0 100	mA μA

Note: Currents into a pin are positive, currents out of a pin are negative.

PIN DESCRIPTION

Symbol	Pin	Description
CD	1	Chip Disable — Digital input. A Logic "0" (<0.8 V) sets normal operation. A Logic "1" (≥2.0 V) sets the power down mode. Input impedance is nominally 90 kΩ.
FC2	2	A capacitor at this pin increases power supply rejection, and affects turn-on time. This pin can be left open if the capacitor at FC1 is sufficient.
FC1	3	Analog Ground for the amplifiers. A 1.0 μF capacitor at this pin (with a 5.0 μF capacitor at Pin 2) provides (typically) 52 dB of power supply rejection. Turn-on time of the circuit is affected by the capacitor on this pin. This pin can be used as an alternate input.
V_{in}	4	Amplifier input. The input capacitor and resistor set low frequency rolloff and input impedance. The feedback resistor is connected to this pin and VO1.
VO1	5	Amplifier Output #1. The dc level is ≈ (V_{CC} − 0.7 V)/2.
V_{CC}	6	DC supply voltage (+2.0 to +16 volts) is applied to this pin.
GND	7	Ground pin for the entire circuit.
VO2	8	Amplifier Output #2. This signal is equal in amplitude, but 180° out of phase with that at VO1. The dc level is ≈ (V_{CC} − 0.7 V)/2.

3

TYPICAL TEMPERATURE PERFORMANCE (0° < T_A < +70°C)

Function	Typical Change	Units
Input Bias Current ($@$ V_{in})	±40	pA/°C
Total Harmonic Distortion (V_{CC} = 6.0 V, R_L = 32 Ω, P_{out} = 125 mW, f = 1.0 kHz)	+0.003	%/°C
Power Supply Current (V_{CC} = 3.0 V, R_L = ∞, CD = 0 V) (V_{CC} = 3.0 V, R_L = ∞, CD = 2.0 V)	 −2.5 −0.03	μA/°C

DESIGN GUIDELINES

GENERAL

The MC34119 is a low power audio amplifier capable of low voltage operation (V_{CC} = 2.0 V minimum) such as that encountered in line-powered speakerphones. The circuit provides a differential output (VO1–VO2) to the speaker to maximize the available voltage swing at low voltages. The differential gain is set by two external resistors. Pins FC1 and FC2 allow controlling the amount of power supply and noise rejection, as well as providing alternate inputs to the amplifiers. The CD pin permits powering down the IC for muting purposes and to conserve power.

AMPLIFIERS

Referring to the block diagram, the internal configuration consists of two identical operational amplifiers. Amplifier #1 has an open-loop gain of ≥80 dB (at f ≤ 100 Hz), and the closed loop gain is set by external resistors R_f and R_i. The amplifier is unity gain stable, and has a unity gain frequency of approximately 1.5 MHz. In order to adequately cover the telephone voice band (300–3400 Hz), a maximum closed loop gain of 46 dB is recommended. Amplifier #2 is internally set to a gain of −1.0 (0 dB).

The outputs of both amplifiers are capable of sourcing and sinking a peak current of 200 mA. The outputs can typically swing to within ≈0.4 volts above ground, and to within ≈1.3 volts below V_{CC}, at the maximum current. See Figures 18 and 19 for V_{OH} and V_{OL} curves.

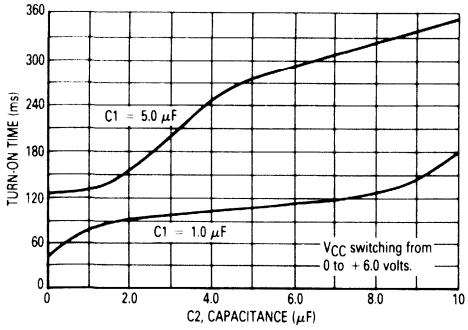
The output dc offset voltage (VO1–VO2) is primarily a function of the feedback resistor (R_f), and secondarily due to the amplifiers' input offset voltages. The input offset voltage of the two amplifiers will generally be similar for a particular IC, and therefore nearly cancel each other at the outputs. Amplifier #1's bias current, however, flows out of V_{in} (Pin 4) and through R_f, forcing VO1 to shift negative by an amount equal to [R_f x I_{IB}]. VO2 is shifted positive an equal amount. The output offset voltage specified in the Electrical Characteristics is measured with the feedback resistor shown in the Typical Application Circuit, and therefore takes into account the bias current as well as internal offset voltages of the amplifiers. The bias current is constant with respect to V_{CC}.

FC1 and FC2

Power supply rejection is provided by the capacitors (C1 and C2 in the Typical Application Circuit) at FC1 and FC2. C2 is somewhat dominant at low frequencies, while C1 is dominant at high frequencies, as shown in the graphs of Figures 4–7. The required values of C1 and C2 depend on the conditions of each application. A line powered speakerphone, for example, will require more filtering than a circuit powered by a well regulated power supply. The amount of rejection is a function of the capacitors, and the equivalent impedance looking into FC1 and FC2 (listed in the Electrical Characteristics as R_{FC1} and R_{FC2}).

In addition to providing filtering, C1 and C2 also affect the turn-on time of the circuit at power-up, since the two capacitors must charge up through the internal 50 k and 125 kΩ resistors. The graph of Figure 1 indicates the turn-on time upon application of V_{CC} of +6.0 volts. The turn-on time is ≈60% longer for V_{CC} = 3.0 volts, and ≈20% less for V_{CC} = 9.0 volts. Turn-off time is <10 μs upon removal of V_{CC}.

FIGURE 1 — TURN-ON TIME versus C1, C2 AT POWER-ON



CHIP DISABLE

The Chip Disable (Pin 1) can be used to power down the IC to conserve power, or for muting, or both. When at a Logic "0" (0 to 0.8 volts), the MC34119 is enabled for normal operation. When Pin 1 is at a Logic "1" (2.0 to V_{CC} volts), the IC is disabled. If Pin 1 is open, that is equivalent to a Logic "0," although good design practice dictates that an input should never be left open. Input impedance at Pin 1 is a nominal 90 kΩ. The power supply current (when disabled) is shown in Figure 15.

Muting, defined as the change in differential gain from normal operation to muted operation, is in excess of 70 dB. The turn-off time of the audio output, from the application of the CD signal, is <2.0 μs, and turn on-time is 12–15 ms. Both times are independent of C1, C2, and V_{CC}.

When the MC34119 is disabled, the voltages at FC1 and FC2 do not change as they are powered from V_{CC}. The outputs, VO1 and VO2, change to a high impedance condition, removing the signal from the speaker. If signals from other sources are to be applied to the outputs (while disabled), they must be within the range of V_{CC} and Ground.

POWER DISSIPATION

Figures 8–10 indicate the device dissipation (within the IC) for various combinations of V_{CC}, R_L, and load power. The maximum power which can safely be dissipated within the MC34119 is found from the following equation:

$$P_D = (140°C - T_A)/\theta_{JA}$$

where T_A is the ambient temperature;
and θ_{JA} is the package thermal resistance (100°C/W for the standard DIP package, and 180°C/W for the surface mount package.)

The power dissipated within the MC34119, in a given application, is found from the following equation:

$$P_D = (V_{CC} \times I_{CC}) + (I_{RMS} \times V_{CC}) - (R_L \times I_{RMS}^2)$$

where I_{CC} is obtained from Figure 15;
and I_{RMS} is the RMS current at the load;
and R_L is the load resistance.

Figures 8–10, along with Figures 11–13 (distortion curves), and a peak working load current of ±200 mA, define the operating range for the MC34119. The operating range is further defined in terms of allowable load power in Figure 14 for loads of 8.0 Ω, 16 Ω, and 32 Ω. The left (ascending) portion of each of the three curves is defined by the power level at which 10% distortion occurs. The center flat portion of each curve is defined by the maximum output current capability of the MC34119. The right (descending) portion of each curve is defined by the maximum internal power dissipation of the IC at 25°C. At higher ambient temperatures, the maximum load power must be reduced according to the above equations. Operating the device beyond the current and junction temperature limits will degrade long term reliability.

LAYOUT CONSIDERATIONS

Normally a snubber is not needed at the output of the MC34119, unlike many other audio amplifiers. However, the PC board layout, stray capacitances, and the manner in which the speaker wires are configured, may dictate otherwise. Generally the speaker wires should be twisted tightly, and be not more than a few inches in length.

TYPICAL CHARACTERISTICS

FIGURE 2 — AMPLIFIER #1 OPEN LOOP GAIN AND PHASE

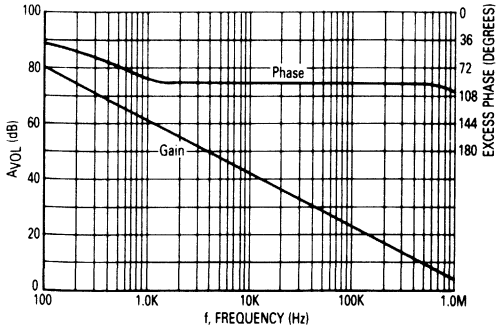
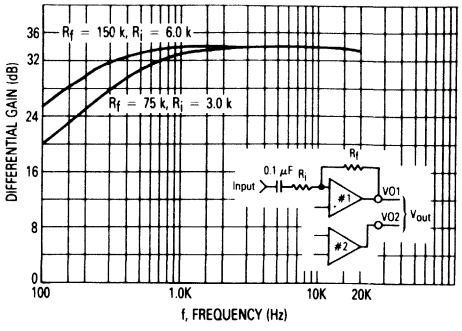


FIGURE 3 — DIFFERENTIAL GAIN versus FREQUENCY



POWER SUPPLY REJECTION versus FREQUENCY

FIGURE 4 — C2 = 10 μF

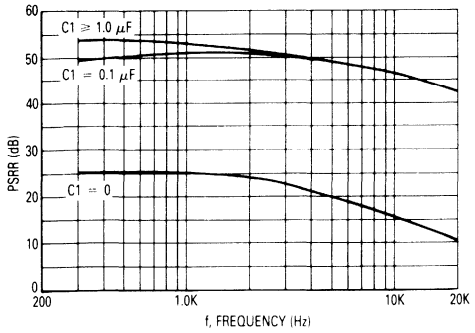


FIGURE 5 — C2 = 5.0 μF

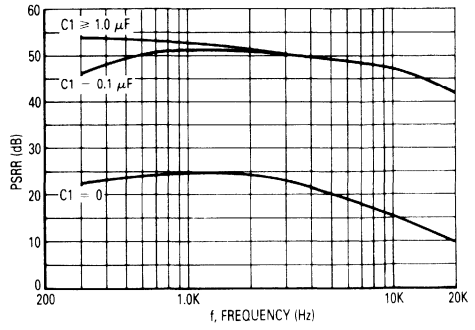


FIGURE 6 — C2 = 1.0 μF

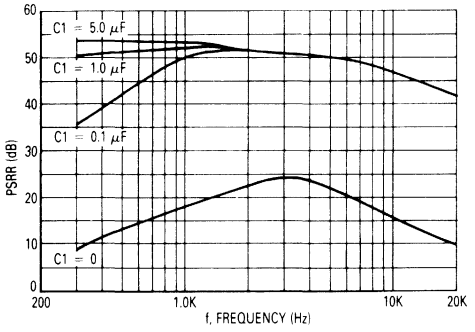


FIGURE 7 — C2 = 0

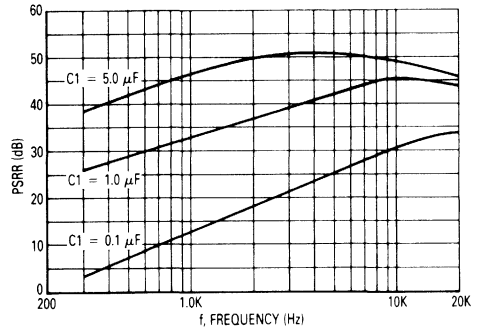


FIGURE 8 — DEVICE DISSIPATION 8.0 Ω LOAD

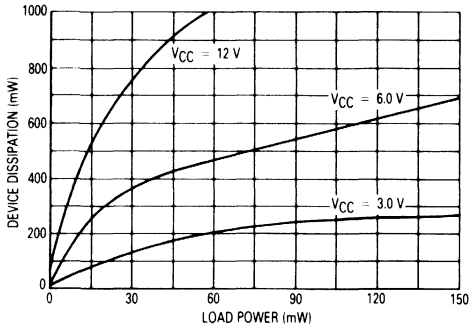


FIGURE 9 — DEVICE DISSIPATION 16 Ω LOAD

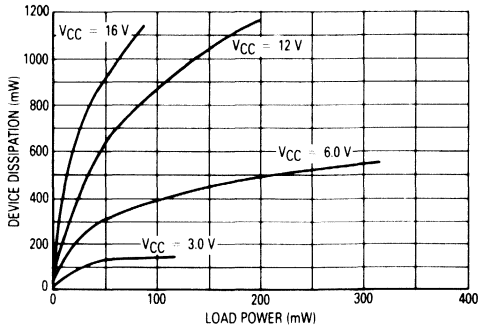


FIGURE 10 — DEVICE DISSIPATION 32 Ω LOAD

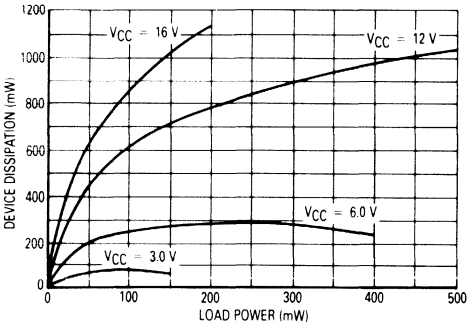


FIGURE 11 — DISTORTION versus POWER f = 1.0 kHz, AVD = 34 dB

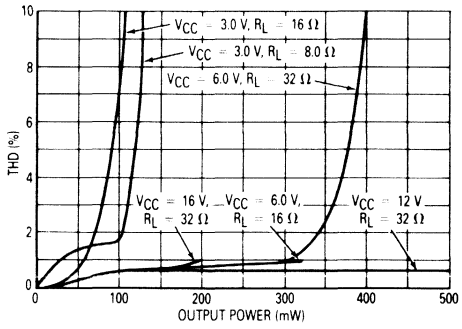


FIGURE 12 — DISTORTION versus POWER f = 3.0 kHz, AVD = 34 dB

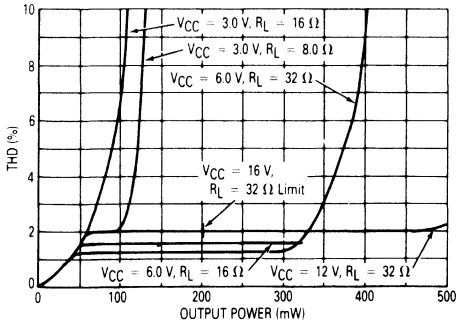
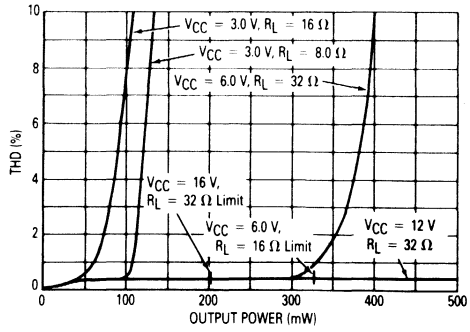


FIGURE 13 — DISTORTION versus POWER f = 1, 3.0 kHz, AVD = 12 dB



3

FIGURE 14 — MAXIMUM ALLOWABLE LOAD POWER

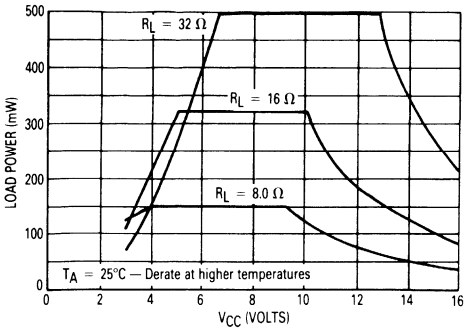
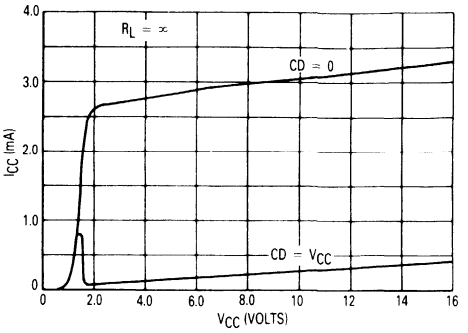


FIGURE 15 — POWER SUPPLY CURRENT



3

FIGURE 16 — SMALL SIGNAL RESPONSE

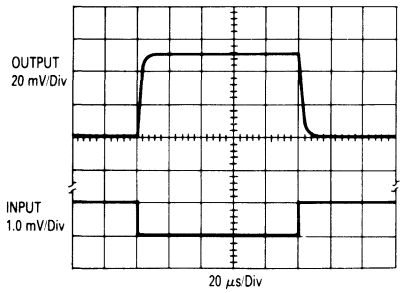


FIGURE 17 — LARGE SIGNAL RESPONSE

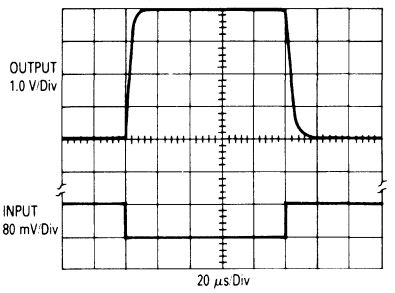


FIGURE 18 — V_{CC}–V_{OH} @ VO1, VO2 versus LOAD CURRENT

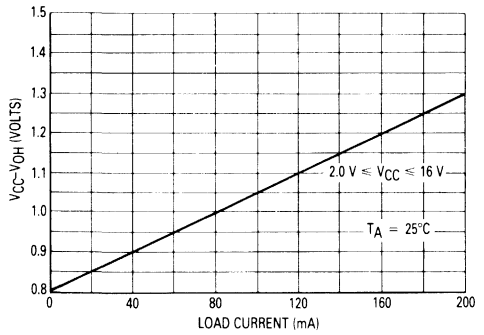


FIGURE 19 — V_{OL} @ VO1, VO2 versus LOAD CURRENT

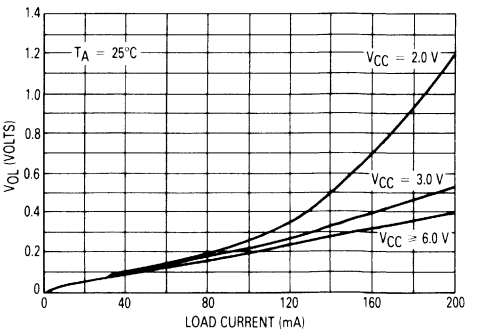


FIGURE 20 — INPUT CHARACTERISTICS @ CD (PIN 1)

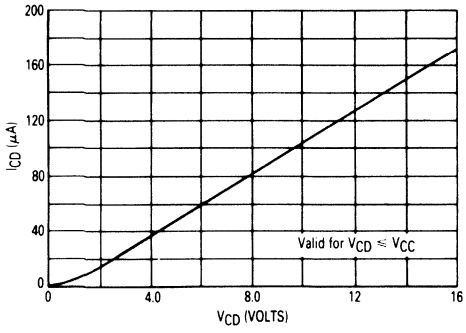
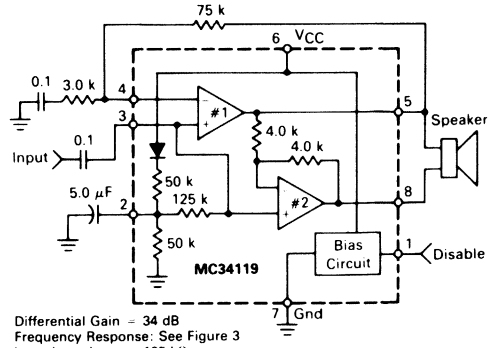


FIGURE 21 — AUDIO AMPLIFIER WITH HIGH INPUT IMPEDANCE



Differential Gain ≈ 34 dB
Frequency Response: See Figure 3
Input Impedance ≈ 125 kΩ
PSRR ≈ 50 dB

FIGURE 22 — AUDIO AMPLIFIER WITH BASS SUPPRESSION

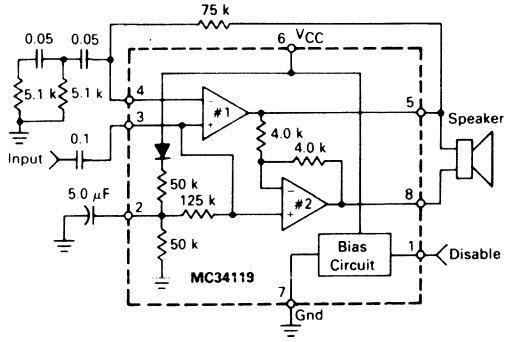


FIGURE 23 — FREQUENCY RESPONSE OF FIGURE 22

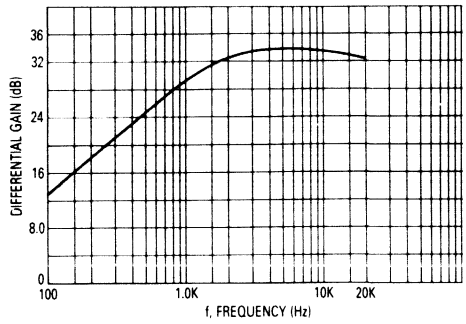


FIGURE 24 — AUDIO AMPLIFIER WITH BANDPASS

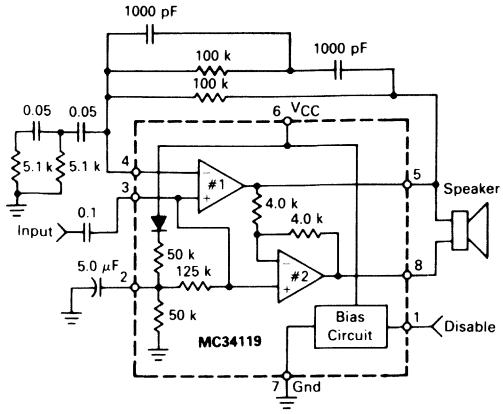


FIGURE 25 — FREQUENCY RESPONSE OF FIGURE 24

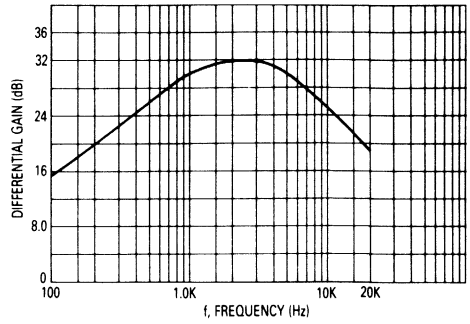
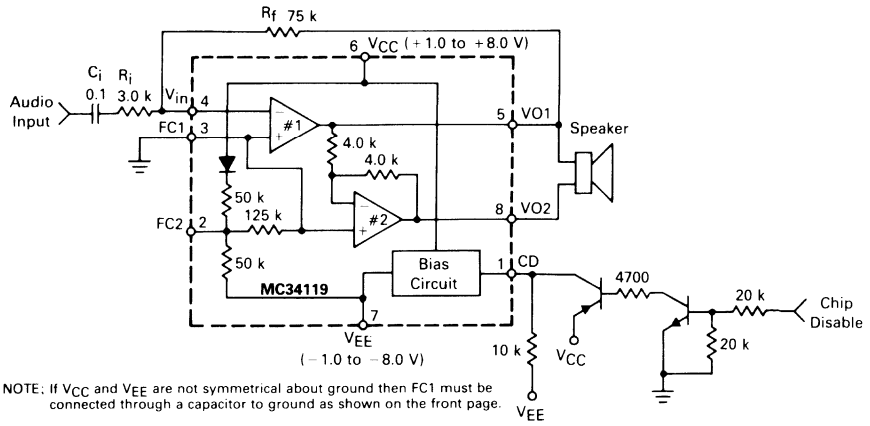


FIGURE 26 — SPLIT SUPPLY OPERATION



NOTE: If V_{CC} and V_{EE} are not symmetrical about ground then FC1 must be connected through a capacitor to ground as shown on the front page.

3

MOTOROLA

MC34120

Product Preview

SUBSCRIBER LOOP INTERFACE CIRCUIT

The MC34120 is designed to provide the interface from the 4-wire side of a central office, or PBX, to the two wire subscriber line. Interface functions include battery feed, loop termination AC impedance, hook switch detection, adjustable transmit, receiver and transhybrid gains, and adjustable loop current limit. Additionally, the MC34120 provides a minimum of 58 dB of longitudinal balance.

The transmit and receive signals are referenced to analog ground, easing the interface to codecs, filters, etc. The Hook Status output can be connected directly to TTL or CMOS circuitry. A Power Down input (TTL and CMOS compatible) permits local control of the circuit.

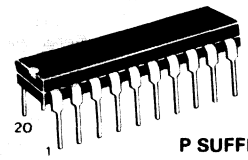
Internal drivers allow the external loop current pass transistors to be standard bipolar transistors (non-Darlington).

The MC34120 will be available in both a 20 pin DIP and a 20 pin surface mount (SOIC) package.

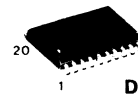
- 58 dB longitudinal balance (minimum).
- Transmit, receive, and transhybrid gains externally adjustable.
- Proper hook switch detection with 30k Ω leakage to ground.
- Adjustable current limit.
- Critical sense resistors included internally.
- Standard power supplies: 48 volts, and +5 volts, ±10%.
- Internal drivers for external pass transistors.
- Power down input.
- Available in 20 pin DIP and 20 pin SOIC plastic packages.
- Operating ambient temperature: 0 to +70°C.

SUBSCRIBER LOOP INTERFACE CIRCUIT (SLIC)

THIN FILM SILICON MONOLITHIC INTEGRATED CIRCUIT

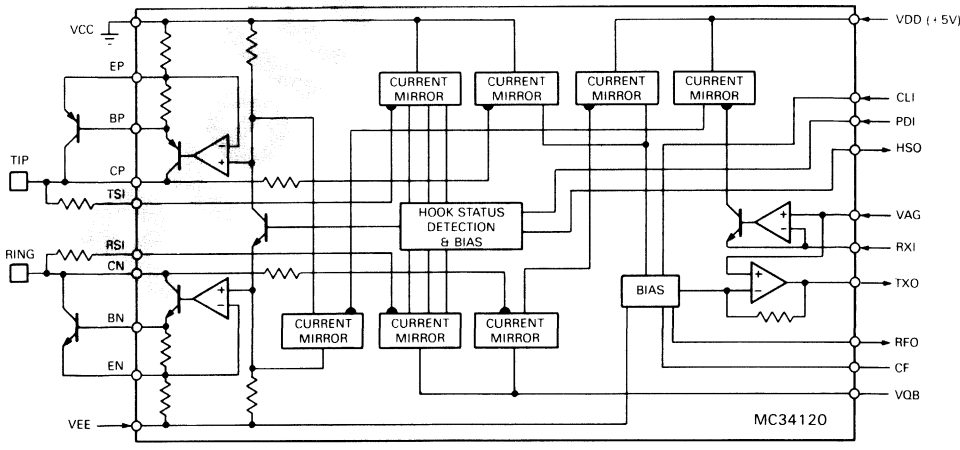


P SUFFIX
PLASTIC PACKAGE
CASE 738-02



DW SUFFIX
PLASTIC PACKAGE
CASE 751D-02

This data sheet contains preliminary information and design objectives. All specifications are subject to change without notice.



MOTOROLA

MC34129
MC33129

Advance Information

HIGH PERFORMANCE CURRENT MODE CONTROLLER

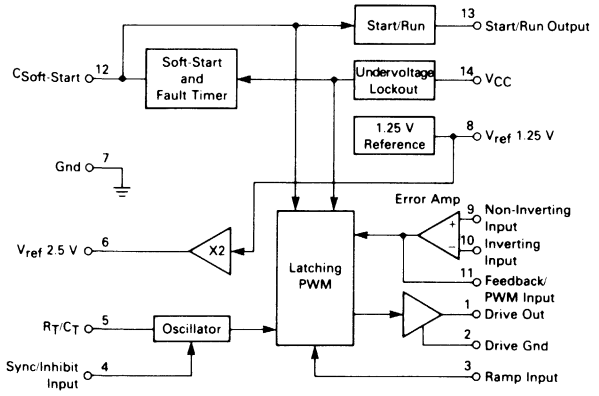
The MC34129 series are high performance current mode switching regulators specifically designed for use in low power digital telephone applications. These integrated circuits feature a unique internal fault timer that provides automatic restart for overload recovery. For enhanced system efficiency, a start/run comparator is included to implement bootstrapped operation of V_{CC}. Other functions contained are a temperature compensated reference, reference amplifier, fully accessible error amplifier, sawtooth oscillator with sync input, pulse width modulator comparator, and a high current totem pole driver ideally suited for driving a power MOSFET.

Also included are protective features consisting of soft-start, undervoltage lockout, cycle-by-cycle current limiting, adjustable dead time, and a latch for single pulse metering.

Although these devices are primarily intended for use in digital telephone systems, they can be used cost effectively in many other applications.

- Current Mode Operation to 300 kHz
- Automatic Feed Forward Compensation
- Latching PWM for Cycle-By-Cycle Current Limiting
- Continuous Retry after Fault Timeout
- Soft-Start with Maximum Peak Switch Current Clamp
- Internally Trimmed 2% Bandgap Reference
- High Current Totem Pole Driver
- Input Undervoltage Lockout
- Low Start-Up and Operating Current
- Direct Interface with Motorola SENSEFET Products

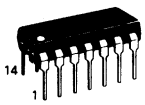
SIMPLIFIED BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice. SENSEFET is a trademark of Motorola Inc.

HIGH PERFORMANCE CURRENT MODE CONTROLLER

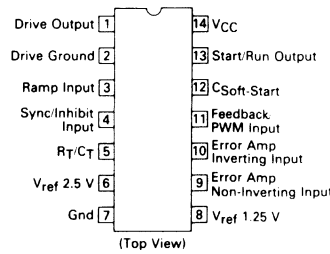
SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 646-06

D SUFFIX
PLASTIC PACKAGE
CASE 751A-01
SO-14

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC34129D	0 to +70°C	SO-14 Plastic DIP
MC34129P	0 to +70°C	Plastic DIP
MC33129D	−40 to +85°C	SO-14 Plastic DIP
MC33129P	−40 to +85°C	Plastic DIP

ADI1349

MAXIMUM RATING

Rating	Symbol	Value	Unit
V_{CC} Zener Current	$I_{Z(V_{CC})}$	50	mA
Start/Run Output Zener Current	$I_{Z(Start/Run)}$	50	mA
Analog Inputs (Pins 3, 5, 9, 10, 11, 12)	—	0.3 to 5.5	V
Sync Input Voltage	V_{sync}	-0.3 to V_{CC}	V
Drive Output Current, Source or Sink	I_{DRV}	1.0	A
Current, Reference Outputs (Pins 6, 8)	I_{ref}	20	mA
Power Dissipation and Thermal Characteristics			
D Suffix Package SO-14 Case 751A-01			
Maximum Power Dissipation @ T_A = 70°C	P_D	552	mW
Thermal Resistance Junction to Air	$R_{\theta JA}$	145	°C/W
P Suffix Package Case 646-06			
Maximum Power Dissipation @ T_A = 70°C	P_D	800	mW
Thermal Resistance Junction to Air	$R_{\theta JA}$	100	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A		°C
MC34129		0 to +70	
MC33129		-40 to +85	
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 10 V, T_A = 25°C [Note 1] unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
REFERENCE SECTIONS					
Reference Output Voltage, T_A = 25°C	V_{ref}				V
1.25 V Ref., I_L = 0 mA		1.225	1.250	1.275	
2.50 V Ref., I_L = 1.0 mA		2.375	2.500	2.625	
Reference Output Voltage, T_A = T_{low} to T_{high}	V_{ref}				V
1.25 V Ref., I_L = 0 mA		1.200	—	1.300	
2.50 V Ref., I_L = 1.0 mA		2.250	—	2.750	
Line Regulation (V_{CC} = 4.0 V to 12 V)	Reg_{line}				mV
1.25 V Ref., I_L = 0 mA		—	2.0	12	
2.50 V Ref., I_L = 1.0 mA		—	10	50	
Load Regulation	Reg_{load}				mV
1.25 V Ref., I_L = -10 to +500 μA		—	1.0	12	
2.50 V Ref., I_L = -0.1 to +1.0 mA		—	3.0	25	
ERROR AMPLIFIER					
Input Offset Voltage (V_{in} = 1.25 V)	V_{IO}				mV
T_A = 25°C		—	1.5	—	
T_A = T_{low} to T_{high}		—	—	10	
Input Offset Current (V_{in} = 1.25 V)	I_{IO}	—	10	—	nA
Input Bias Current (V_{in} = 1.25 V)	I_{IB}				nA
T_A = 25°C		—	25	—	
T_A = T_{low} to T_{high}		—	—	200	
Input Common-Mode Voltage Range	V_{ICR}	—	0.5 to 5.5	—	V
Open-Loop Voltage Gain (V_O = 1.25 V)	A_{VOL}	65	87	—	dB
Gain Bandwidth Product (V_O = 1.25 V, f = 100 kHz)	GBW	500	750	—	kHz
Power Supply Rejection Ratio (V_{CC} = 5.0 to 10 V)	PSRR	65	85	—	dB
Output Source Current (V_O = 1.5 V)	I_{Source}	40	80	—	μA
Output Voltage Swing					V
High State (I_{Source} = 0 μA)	V_{OH}	1.75	1.96	2.25	
Low State (I_{Sink} = 500 μA)	V_{OL}	—	0.1	0.15	

Note 1. T_{low} = 0°C for MC34129
-40°C for MC33129
T_{high} = +70°C for MC34129
= +85°C for MC33129

ELECTRICAL CHARACTERISTICS (V_{CC} = 10 V, T_A = 25°C [Note 1] unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
PWM COMPARATOR					
Input Offset Voltage (V_{in} = 1.25 V)	V_{IO}	150	275	400	mV
Input Bias Current	I_{IB}	—	−120	−250	μA
Propagation Delay, Ramp Input to Drive Output	$t_{PLH(IN/DRV)}$	—	250	—	ns
SOFT-START					
Capacitor Charge Current (Pin 12 = 0 V)	I_{chg}	0.75	1.2	1.50	μA
Buffer Input Offset Voltage (V_{in} = 1.25 V)	V_{IO}	—	15	40	mV
Buffer Output Voltage (I_{Sink} = 100 μA)	V_{OL}	—	0.15	0.225	V
FAULT TIMER					
Restart Delay Time	t_{DLY}	200	400	600	μs
START/RUN COMPARATOR					
Threshold Voltage (Pin 12)	V_{th}	—	2.0	—	V
Threshold Hysteresis Voltage (Pin 12)	V_H	—	350	—	mV
Output Voltage (I_{Sink} = 500 μA)	V_{OL}	9.0	10	10.3	V
Output Off-State Leakage Current (V_{OH} = 15 V)	$I_{S/R(leak)}$	—	0.4	2.0	μA
Output Zener Voltage (I_Z = 10 mA)	V_Z	—	(V_{CC} + 7.6)	—	V
OSCILLATOR					
Frequency (R_T = 25.5 kΩ, C_T = 390 pF)	f_{OSC}	80	100	120	kHz
Capacitor C_T Discharge Current (Pin 5 = 1.2 V)	I_{dischg}	240	350	460	μA
Sync Input Current					μA
High State (V_{in} = 2.0 V)	I_{IH}	—	40	125	
Low State (V_{in} = 0.8 V)	I_{IL}	—	15	35	
Sync Input Resistance	R_{in}	12.5	32	50	kΩ
DRIVE OUTPUT					
Output Voltage					V
High State (I_{Source} = 200 mA)	V_{OH}	8.3	8.9	—	
Low State (I_{Sink} = 200 mA)	V_{OL}	—	1.4	1.8	
Low State Holding Current	I_H	—	225	—	μA
Output Voltage Rise Time (C_L = 500 pF)	t_r	—	100	—	ns
Output Voltage Fall Time (C_L = 500 pF)	t_f	—	30	—	ns
Output Pull-Down Resistance	R_{PD}	100	225	350	kΩ
UNDERVOLTAGE LOCKOUT					
Start-Up Threshold	V_{th}	3.0	3.6	4.2	V
Hysteresis	V_H	5.0	10	15	%
TOTAL DEVICE					
Power Supply Current R_T = 25.5 kΩ, C_T = 390 pF, C_L = 500 pF	I_{CC}	1.0	2.5	4.0	mA
Power Supply Zener Voltage (I_Z = 10 mA)	V_Z	12	14.3	—	V

Note 1. T_{low} = 0°C for MC34129 = −40°C for MC33129 T_{high} = +70°C for MC34129 = +85°C for MC33129

FIGURE 1 — TIMING RESISTOR versus OSCILLATOR FREQUENCY

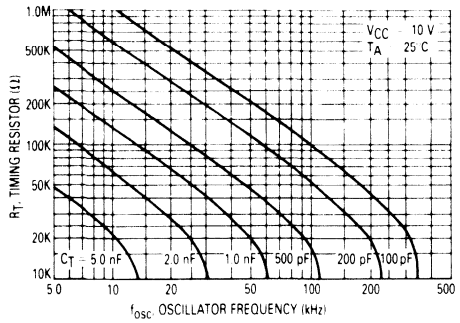


FIGURE 2 — OUTPUT DEAD-TIME versus OSCILLATOR FREQUENCY

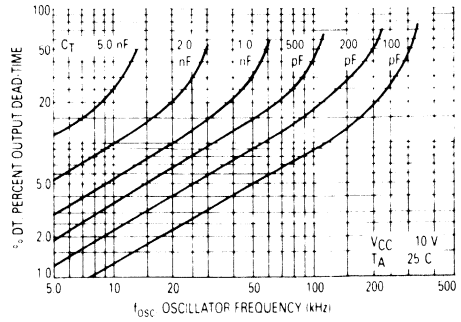


FIGURE 3 — OSCILLATOR FREQUENCY CHANGE versus TEMPERATURE

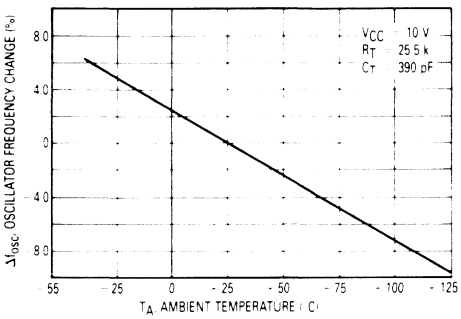


FIGURE 4 — ERROR AMP OPEN-LOOP GAIN AND PHASE versus FREQUENCY

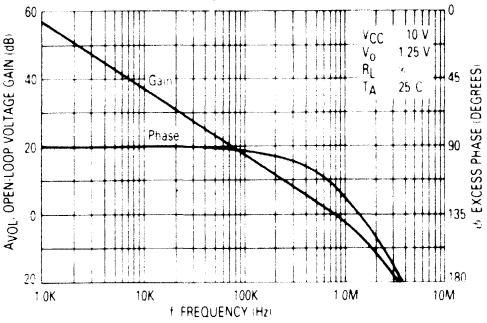


FIGURE 5 — ERROR AMP SMALL-SIGNAL TRANSIENT RESPONSE

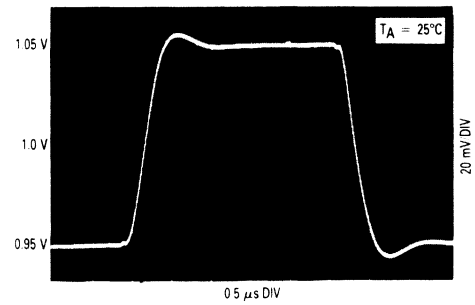
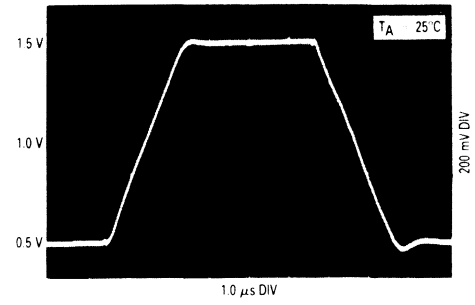


FIGURE 6 — ERROR AMP LARGE-SIGNAL TRANSIENT RESPONSE



3

FIGURE 7 — ERROR AMP OPEN-LOOP DC GAIN versus LOAD RESISTANCE

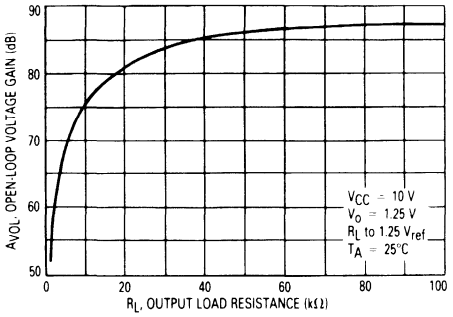


FIGURE 8 — ERROR AMP OUTPUT SATURATION versus SINK CURRENT

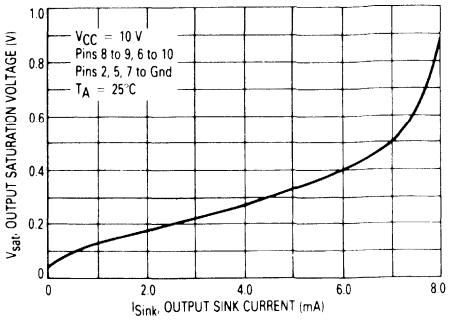


FIGURE 9 — SOFT-START BUFFER OUTPUT SATURATION versus SINK CURRENT

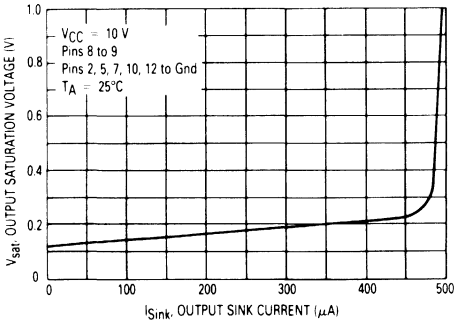


FIGURE 10 — REFERENCE OUTPUT VOLTAGE versus SUPPLY VOLTAGE

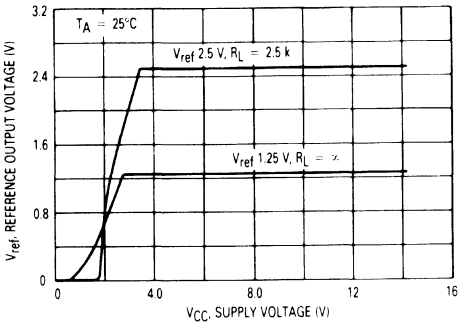


FIGURE 11 — 1.25 V REFERENCE OUTPUT VOLTAGE CHANGE versus SOURCE CURRENT

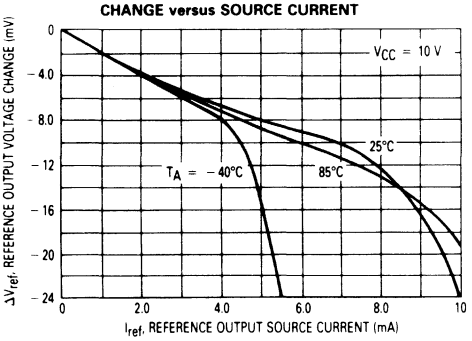


FIGURE 12 — 2.5 V REFERENCE OUTPUT VOLTAGE CHANGE versus SOURCE CURRENT

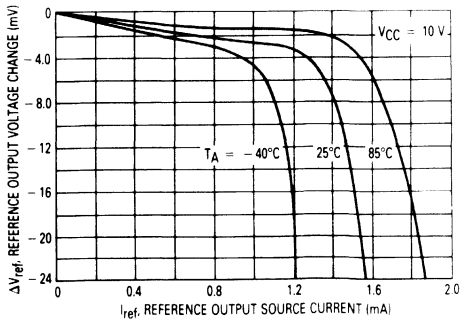


FIGURE 13 — 1.25 V REFERENCE OUTPUT VOLTAGE versus TEMPERATURE

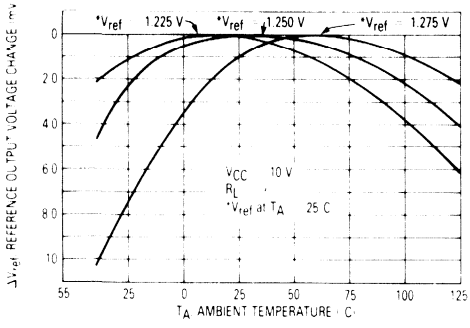
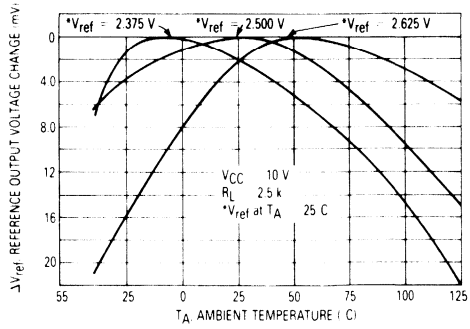


FIGURE 14 — 2.5 V REFERENCE OUTPUT VOLTAGE versus TEMPERATURE



3

FIGURE 15 — DRIVE OUTPUT SATURATION versus LOAD CURRENT

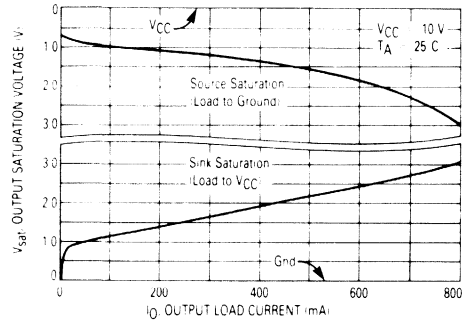


FIGURE 16 — DRIVE OUTPUT WAVEFORM

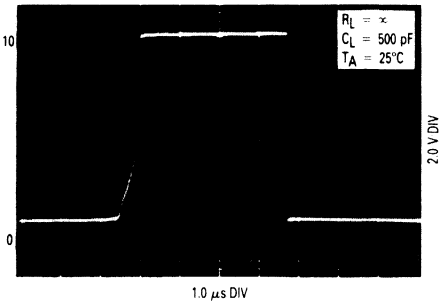
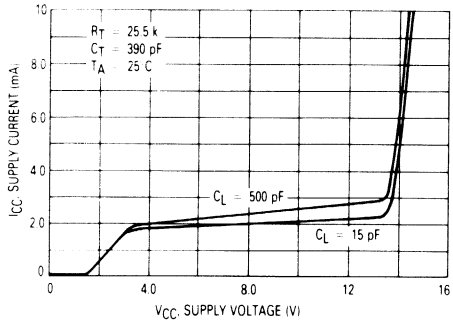


FIGURE 17 — SUPPLY CURRENT versus SUPPLY VOLTAGE



PIN FUNCTION DESCRIPTION

Pin No.	Function	Description
1	Drive Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1.0 A are sourced and sinked by this pin.
2	Drive Ground	This pin is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
3	Ramp Input	A voltage proportional to the inductor current is connected to this input. The PWM uses this information to terminate output switch conduction.
4	Sync/Inhibit Input	A rectangular waveform applied to this input will synchronize the Oscillator and limit the maximum Drive Output duty cycle. A dc voltage within the range of 2.0 V to V_{CC} will inhibit the controller.
5	R_T/C_T	The free-running Oscillator frequency and maximum Drive Output duty cycle are programmed by connecting resistor R_T to V_{ref} 2.5 V and capacitor C_T to Ground. Operation to 300 kHz is possible.
6	V_{ref} 2.50 V	This output is derived from V_{ref} 1.25 V. It provides charging current for capacitor C_T through resistor R_T.
7	Ground	This pin is the control circuitry ground return and is connected back to the source ground.
8	V_{ref} 1.25 V	This output furnishes a voltage reference for the Error Amplifier Non-Inverting Input.
9	Error Amp Non-Inverting Input	This is the non-inverting input of the Error Amplifier. It is normally connected to the 1.25 V reference.
10	Error Amp Inverting Input	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
11	Feedback/PWM Input	This pin is available for loop compensation. It is connected to the Error Amplifier and Soft-Start Buffer outputs, and the Pulse Width Modulator input.
12	$C_{Soft\text{-}Start}$	A capacitor $C_{Soft\text{-}Start}$ is connected from this pin to Ground for a controlled ramp-up of peak inductor current during start-up.
13	Start/Run Output	This output controls the state of an external bootstrap transistor. During the start mode, operating bias is supplied by the transistor from V_{in}. In the run mode, the transistor is switched off and bias is supplied by an auxiliary power transformer winding.
14	V_{CC}	This pin is the positive supply of the control IC. The controller is functional over a minimum V_{CC} range of 4.2 V to 12 V.

OPERATING DESCRIPTION

The MC34129 series are high performance current mode switching regulator controllers specifically designed for use in low power telecommunication applications. Implementation will allow remote digital telephones and terminals to shed their power cords and derive operating power directly from the twisted pair used for data transmission. Although these devices are primarily intended for use in digital telephone systems, they can be used cost effectively in a wide range of converter applications. A representative block diagram is shown in Figure 18.

OSCILLATOR

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T. Capacitor C_T is charged from the 2.5 V reference through resistor R_T to approximately 1.25 V and discharged by an internal current sink to ground. During the discharge of C_T, the oscillator generates an internal blanking pulse that holds the lower input of the NOR gate high. This causes the Drive Output to be in a low state, thus producing a controlled amount of output deadtime. Figure 1 shows Oscillator Frequency versus R_T and Figure 2, Output Deadtime versus Frequency, both for given values of C_T. Note that many values of R_T and C_T will give the same oscillator frequency but only one combination will yield a specific output deadtime at a given frequency. In many noise sensitive applications it may be desirable to frequency-lock one or more switching regulators to an external system clock. This can be accomplished by applying the clock signal to the Sync/Inhibit Input. For reliable locking, the free-running oscillator frequency should be about 10% less than the clock frequency. Referring to the timing diagram shown in Figure 19, the rising edge of the clock signal applied to the Sync/Inhibit Input, terminates charging of C_T and Drive Output conduction. By tailoring the clock waveform, accurate duty cycle clamping of the Drive Output can be achieved. A circuit method is shown in Figure 20. The Sync/Inhibit Input may also be used as a means for system shutdown by applying a dc voltage that is within the range of 2.0 V to V_{CC}.

PWM COMPARATOR AND LATCH

The MC34129 operates as a current mode controller whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches a threshold level established by the output of the Error Amp or Soft-Start Buffer (Pin 11). Thus the error signal controls the peak inductor current on a cycle-by-cycle basis. The PWM Comparator-Latch configuration used, ensures that only a single pulse appears at the Drive Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting the ground-referenced resistor R_S in series with the source of output switch Q_1. The Ramp Input adds an offset of 275 mV to this voltage to guarantee that no pulses appear at the Drive Output when Pin 11 is at its lowest state. This occurs at the beginning of the soft-start interval or when the power supply is operating and the load is removed. The peak inductor current under normal operating conditions is controlled by the voltage at Pin 11 where:

$$I_{pk} = \frac{V_{(Pin\ 11)} - 0.275\ V}{R_S}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the voltage at Pin 11 will be internally clamped to 1.95 V by the output of the Soft-Start Buffer. Therefore the maximum peak switch current is:

$$I_{pk(max)} = \frac{1.95\ V - 0.275}{R_S} = \frac{1.675\ V}{R_S}$$

When designing a high power switching regulator it becomes desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. A simple method which adjusts this voltage in discrete increments is shown in Figure 22. This method is possible because the Ramp Input bias current is always negative (typically −120 μA). A positive temperature coefficient equal to that of the diode string will be exhibited by $I_{pk(max)}$. An adjustable method that is more precise and temperature stable is shown in Figure 23. Erratic operation due to noise pickup can result if there is an excessive reduction of the clamp voltage. In this situation, high frequency circuit layout techniques are imperative.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Ramp Input with a time constant that approximates the spike duration will usually eliminate the instability; refer to Figure 25.

ERROR AMP AND SOFT-START BUFFER

A fully-compensated Error Amplifier with access to both inputs and output is provided for maximum design flexibility. The Error Amplifier output is common with that of the Soft-Start Buffer. These outputs are open-collector (sink only) and are ORed together at the inverting input of the PWM Comparator. With this configuration, the amplifier that demands lower peak inductor current dominates control of the loop. Soft-start is mandatory for stable start-up when power is provided through a high source impedance such as the long twisted pair used in telecommunications. It effectively removes the load from the output of the switching power supply upon initial start-up. The Soft-Start Buffer is configured as a unity gain follower with the non-inverting input connected to Pin 12. An internal 1.0 μA

FIGURE 18 — REPRESENTATIVE BLOCK DIAGRAM

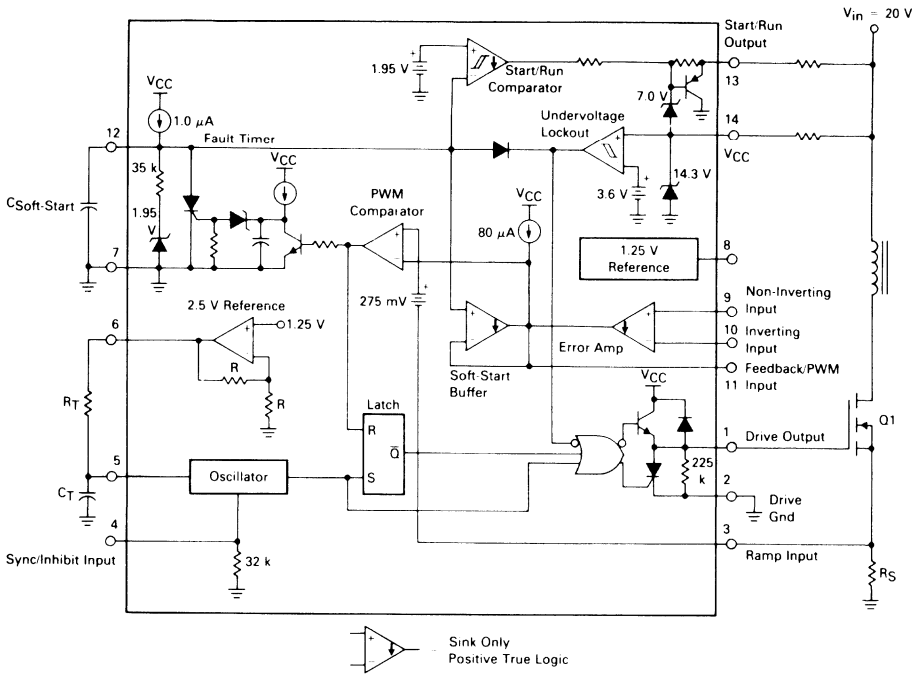
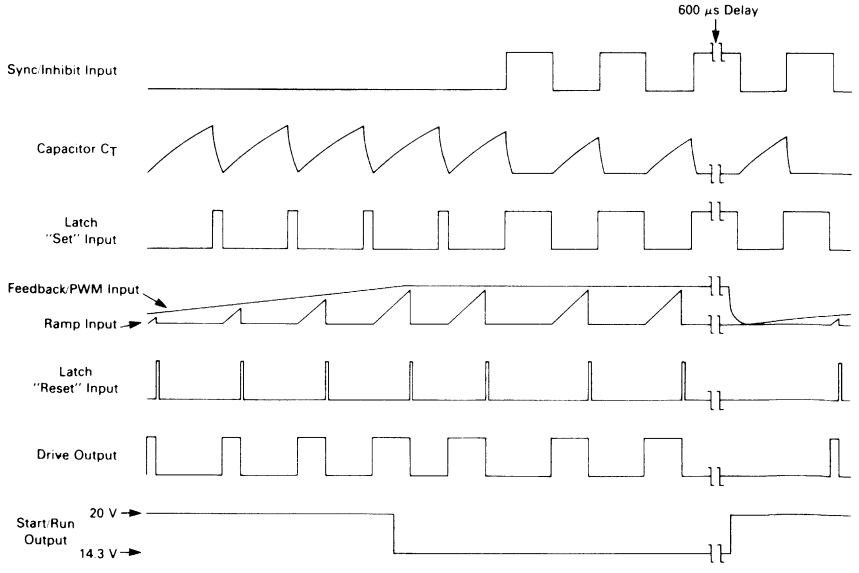


FIGURE 19 — TIMING DIAGRAM



OPERATING DESCRIPTION (continued)

current source charges the soft-start capacitor ($C_{Soft-Start}$) to an internally clamped level of 1.95 V. The rate of change of peak inductor current, during start-up, is programmed by the capacitor value selected. Either the Fault Timer or the Undervoltage Lockout can discharge the soft-start capacitor.

FAULT TIMER

This unique circuit prevents sustained operation in a lockout condition. This can occur with conventional switching control IC's when operating from a power source with a high series impedance. If the power required by the load is greater than that available from the source, the input voltage will collapse, causing the lockout condition. The Fault Timer provides automatic recovery when this condition is detected. Under normal operating conditions, the output of the PWM Comparator will reset the Latch and discharge the internal Fault Timer capacitor on a cycle-by-cycle basis. Under operating conditions where the required power into the load is greater than that available from the source (V_{in}), the Ramp Input voltage (plus offset) will not reach the comparator threshold level (Pin 11), and the output of the PWM Comparator will remain low. If this condition persists for more than 600 μs, the Fault Timer will activate, discharging $C_{Soft-Start}$ and initiating a soft-start cycle. The power supply will operate in a skip cycle or hiccup mode until either the load power or source impedance is reduced. The minimum fault timeout is 200 μs, which limits the useful switching frequency to a minimum of 5.0 kHz.

START/RUN COMPARATOR

A bootstrap start-up circuit is included to improve system efficiency when operating from a high input voltage. The output of the Start/Run Comparator controls the state of an external transistor. A typical application is shown in Figure 21. While $C_{Soft-Start}$ is charging, start-up bias is supplied to V_{CC} (Pin 14) from V_{in} through transistor Q2. When $C_{Soft-Start}$ reaches the 1.95 V clamp level, the Start-Run output switches low (V_{CC} – 50 mV), turning off Q2. Operating bias is now derived from the auxiliary bootstrap winding of the transformer, and all drive power is efficiently converted down from V_{in}. The start time must be long enough for the power supply output to reach regulation. This will ensure that there is sufficient bias voltage at the auxiliary bootstrap winding for sustained operation.

$$t_{Start} = \frac{1.95\ V\ C_{Soft-Start}}{1.0\ \mu A} = 1.95\ C_{Soft-Start\ in\ \mu F}$$

The Start/Run Comparator has 350 mV of hysteresis. The output off-state is clamped to V_{CC} + 7.6 V by the internal zener and PNP transistor base-emitter junction.

DRIVE OUTPUT AND DRIVE GROUND

The MC34129 contains a single totem-pole output stage that was specifically designed for direct drive of power MOSFETs. It is capable of up to ±1.0 A peak drive current and has a typical fall time of 30 ns with a 500 pF load. The totem-pole stage consists of an NPN transistor for turn-on drive and a high speed SCR for turn-off. The SCR design requires less average supply current (I_{CC}) when compared to conventional switching control IC's that use an all NPN totem-pole. The SCR accomplishes this during turn-off of the MOSFET, by utilizing the gate charge as regenerative on-bias, whereas the conventional all transistor design requires continuous base current. Conversion efficiency in low power applications is greatly enhanced with this reduction of I_{CC}. The SCR's low-state holding current (I_H) is typically 225 μA. An internal 225 kΩ pull-down resistor is included to shunt the Drive Output off-state leakage to ground when the Undervoltage Lockout is active. A separate Drive Ground is provided to reduce the effects of switching transient noise imposed on the Ramp Input. This feature becomes particularly useful when the $I_{pk(max)}$ clamp level is reduced. Figure 24 shows the proper implementation of the MC34129 with a current sensing power MOSFET.

UNDERVOLTAGE LOCKOUT

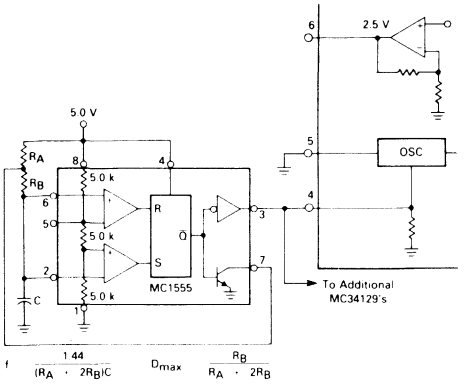
The Undervoltage Lockout comparator holds the Drive Output and $C_{Soft-Start}$ pins in the low state when V_{CC} is less than 3.6 V. This ensures that the MC34129 is fully functional before the output stage is enabled and a soft-start cycle begins. A built-in hysteresis of 350 mV prevents erratic output behavior as V_{CC} crosses the comparator threshold voltage. A 14.3 V zener is connected as a shunt regulator from V_{CC} to ground. Its purpose is to protect the MOSFET gate from excessive drive voltage during system start-up. An external 9.1 V zener is required when driving low threshold MOSFETs. Refer to Figure 21. The minimum operating voltage range of the IC is 4.2 V to 12 V.

REFERENCES

The 1.25 V bandgap reference is trimmed to ±2.0% tolerance at T_A = 25°C. It is intended to be used in conjunction with the Error Amp. The 2.50 V reference is derived from the 1.25 V reference by an internal op amp with a fixed gain of 2.0. It has an output tolerance of ±5.0% at T_A = 25°C and its primary purpose is to supply charging current to the oscillator timing capacitor.

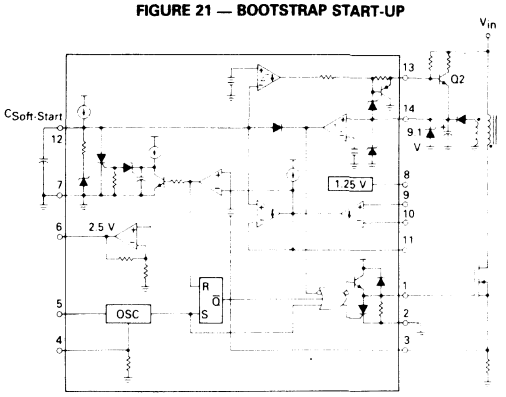
3

FIGURE 20 — EXTERNAL DUTY CYCLE CLAMP AND MULTI UNIT SYNCHRONIZATION



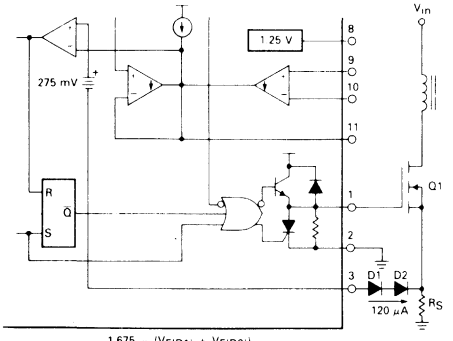
$$f \approx \frac{1.44}{(R_A + 2R_B)C} \qquad D_{max} \approx \frac{R_B}{R_A + 2R_B}$$

FIGURE 21 — BOOTSTRAP START-UP



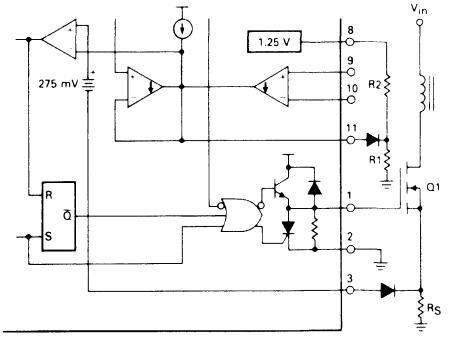
The external 9.1 V zener is required when driving low threshold MOSFETs

FIGURE 22 — DISCRETE STEP REDUCTION OF CLAMP LEVEL



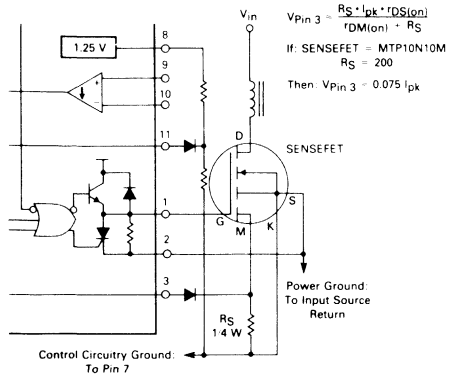
$$I_{pk(max)} \approx \frac{1.675\ (V_{F(D1)} + V_{F(D2)})}{R_S}$$

FIGURE 23 — ADJUSTABLE REDUCTION OF CLAMP LEVEL



If: $\frac{1.25\ V}{R1 + R2} \geq 1.0\ mA$ Then: $I_{pk(max)} \approx \frac{\frac{1.25}{\left(\frac{R2}{R1} + 1\right)} + 0.275}{R_S}$

FIGURE 24 — CURRENT SENSING POWER MOSFET

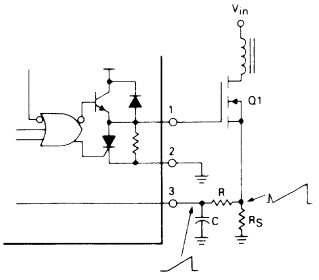


$$V_{Pin\ 3} \approx \frac{R_S \cdot I_{pk} \cdot r_{DS(on)}}{r_{DM(on)} + R_S}$$

If: SENSEFET = MTP10N10M
R_S = 200
Then: $V_{Pin\ 3} \approx 0.075\ I_{pk}$

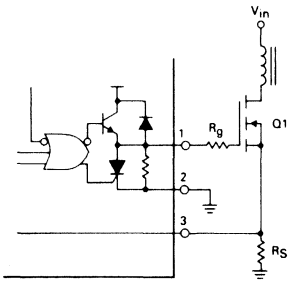
Virtually lossless current sensing can be achieved with the implementation of a SENSEFET power switch

FIGURE 25 — CURRENT WAVEFORM SPIKE SUPPRESSION



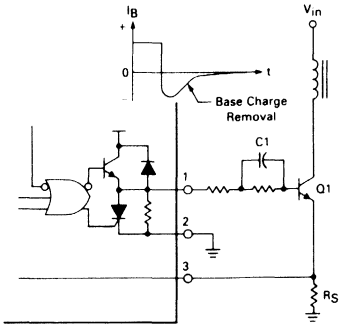
The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform

FIGURE 26 — MOSFET PARASITIC OSCILLATIONS



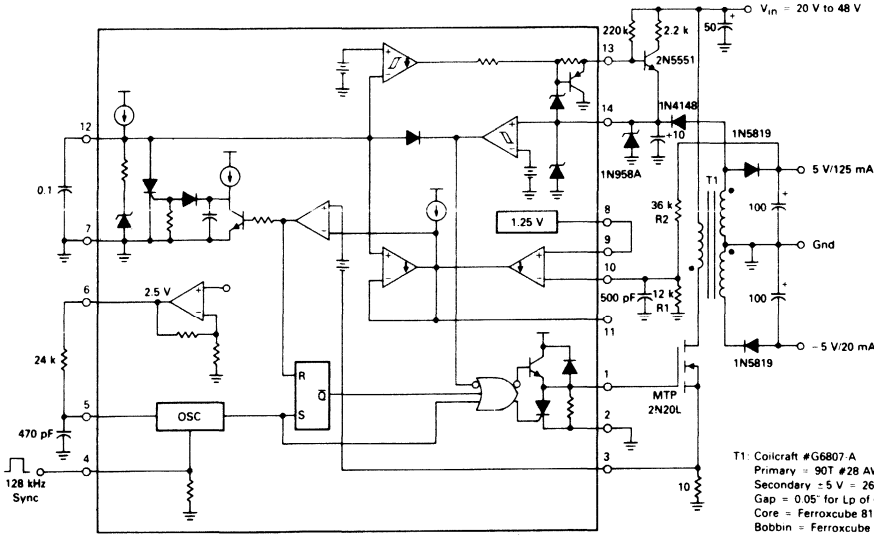
Series gate resistor R_G will damp any high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate-source circuit.

FIGURE 27 — BIPOLAR TRANSISTOR DRIVE



The totem-pole output can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor C1.

FIGURE 28 — NON-ISOLATED 725 mW FLYBACK REGULATOR



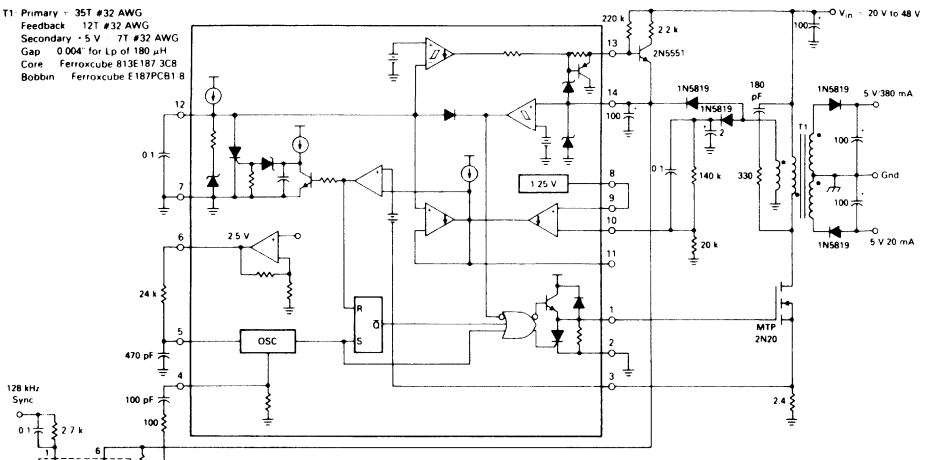
T1: Coilcraft #G6807-A
Primary = 90T #28 AWG
Secondary +5 V = 26T #30 AWG
Gap = 0.05" for Lp of 600 μH
Core = Ferroxcube 813E187-3C8
Bobbin = Ferroxcube E187PCB1-8

Test	Conditions	Results
Line Regulation 5 V	V_{in} = 20 V to 40 V, I_{out} 5 V = 125 mA, I_{out} −5 V = 20 mA	Δ = 1.0 mV
Load Regulation 5 V	V_{in} = 30 V, I_{out} 5 V = 0 mA to 150 mA, I_{out} −5 V = 20 mA	Δ = 2.0 mV
Output Ripple 5 V	V_{in} = 30 V, I_{out} 5 V = 125 mA, I_{out} −5 V = 20 mA	150 mVp-p
Efficiency	V_{in} = 30 V, I_{out} 5 V = 125 mA, I_{out} −5 V = 20 mA	77%

$$V_{out} = 1.25\left(\frac{R2}{R1} + 1\right)$$

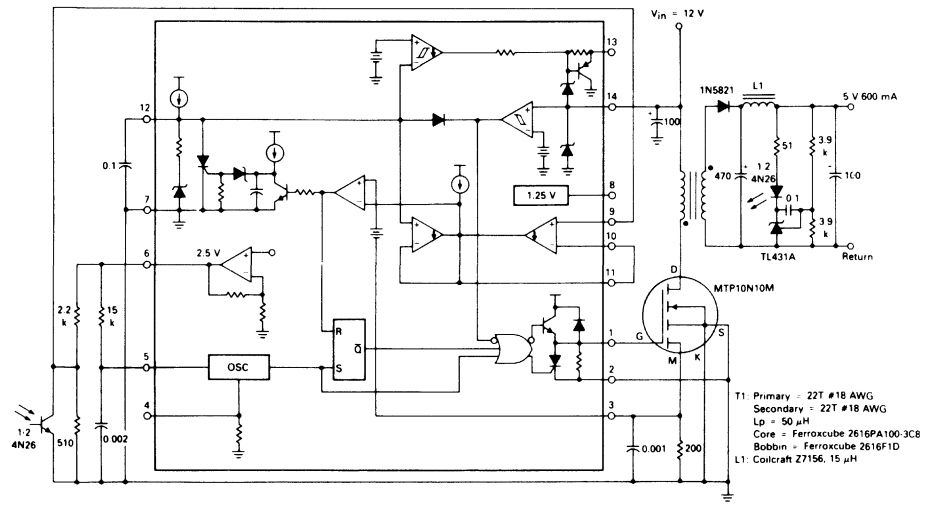
3

FIGURE 29 — ISOLATED 2.0 W FLYBACK REGULATOR



Test	Conditions	Results
Line Regulation 5 V	V_{in} = 20 V to 40 V, I_{out} 5 V = 380 mA, I_{out} – 5 V = 20 mA	Δ = 1 mV
Load Regulation 5 V	V_{in} = 30 V, I_{out} 5 V = 100 mA to 380 mA, I_{out} – 5 V = 20 mA	Δ = 15 mV
Output Ripple 5 V	V_{in} = 30 V, I_{out} 5 V = 380 mA, I_{out} – 5 V = 20 mA	150 mVp-p
Efficiency	V_{in} = 30 V, I_{out} 5 V = 380 mA, I_{out} – 5 V = 20 mA	73%

FIGURE 30 — ISOLATED 3.0 W FLYBACK REGULATOR WITH SECONDARY SIDE SENSING



Test	Conditions	Results
Line Regulation	V_{in} = 8 V to 12 V, I_{out} 600 mA	Δ = 1 mV
Load Regulation	V_{in} = 12 V, I_{out} = 100 mA to 600 mA	Δ = 8 mV
Output Ripple	V_{in} = 12 V, I_{out} = 600 mA	20 mVp-p
Efficiency	V_{in} = 12 V, I_{out} = 600 mA	81%

An economical method of achieving secondary sensing is to combine the TL431A with a 4N26 optocoupler.

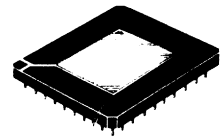
MOTOROLA

MC68605
Technical Summary

X.25 Protocol Controller (XPC)

The MC68605 X.25 Protocol Controller (XPC) is an intelligent HCMOS communications protocol controller that implements the 1984 International Telegraph and Telephone Consultative Committee (CCITT) X.25 Recommendation, data link access procedure (LAPB). It supports full duplex point-to-point serial communication at up to 10 megabits per second (MBPS) and relieves the host processor of managing the communications link by providing sequencing using HDLC framing, error control, retransmission based upon a cyclic redundancy check (CRC), and flow control using the receive not ready supervisory frame. The XPC directly supports the physical level interfaces (Recommendation X.21 physical level, X.21 *bis*, and V-series) and also provides and efficient interface to the packet level for information and control exchange. Key features of the XPC include:

- Fully Implements X.25 Recommendation LAPB Procedure by Independently Generating Link Level Commands and Responses
- Optional Transparent Operation (Monitor Mode) where XPC Provides HDLC/SDLC Framing Functions for User Generated Frames
- Performs DMA Transfer of Information Frames To and From Memory Using Two On-Chip 22-Byte FIFOs
- Primary Communication Through Shared Memory Structures with a Powerful Command Set to Off-Load Data Link Management
- Flexible Rx/Tx Linked Memory Structures Minimize Host Intervention and Simplify Memory Management
- Basic (Modulo 8) and Extended (Modulo 128) Operation
- Automatic Comparison of the Programmable Local and Remote Addresses
- Detection of Programmable Timeout and Retries Limit Conditions
- 16- or 32-Bit CRC Generation and Checking
- Standard Modem Interface
- NRZ or NRZI Encoding/Decoding
- Vectored Interrupts and Status Reporting
- Built-In Diagnostics Provide Local Loopback and External Loopback Testing
- Up to 10 Mbps Synchronous Serial Data Rate
- 12.5 and 10 MHz System Clock Versions
- 8- and 16-Bit Data Bus Support
- 32-Bit Address Bus with Virtual Address Capability
- M68000 Family Asynchronous Bus Structure
- Programmable Byte Ordering of Data for Alternate Memory Organization Schemes



RC SUFFIX
PIN GRID ARRAY
(84 PIN)
CASE 793

PIN ASSIGNMENT

	1	2	3	4	5	6	7	8	9	10
K	TxD	GND	GND	A3	A6	A8	A10	A12	A14	A16
J	$\overline{CD}$	RCLK	GND	A2	A5	A9	A13	A15	A17	A20
H	$\overline{CTS}$	RxD	TCLK	A1	A4	A7	A11	A18	A19	A21
G	$\overline{BEC1}$	$\overline{BEC2}$	$\overline{RTS}$					A22	A23	A24
F	CLK	$\overline{BECO}$	GND					V_{DD}	A25	A26
E	$\overline{BR}$	$\overline{BG}$	GND		BOTTOM VIEW			A27	A29	A28
D	$\overline{BGACK}$	$\overline{IACK}$	V_{DD}					GND	GND	A30
C	$\overline{IRQ}$	$\overline{DTACK}$	GND	D0	D6	D9	D12	$\overline{CS}$	FC1	A31
B	R/$\overline{W}$	GND	$\overline{UDS}$/A0	D2	D5	D8	D11	D15	FC3	FC0
A	$\overline{LDS}$/$\overline{DS}$	$\overline{AS}$	D1	D3	D4	D7	D10	D13	D14	FC2

GENERAL DESCRIPTION

The XPC supports high-speed X.25 communications between host computers, between host computers and remote units, and between remote units. The XPC also supports a transparent operation mode which does not apply the LAPB procedure. Data is passed between the XPC and the host processor through shared memory structures. This permits a minimum command set for host processor/XPC communication. Additionally the XPC is a full M68000 bus master, providing on-chip DMA capability for management of memory tables and frame buffers. Since the XPC data bus interface is configurable, the XPC can handle both 8-bit and 16-bit data transfers.

When the X.25 mode is selected by the user, the XPC is configured as a combined station for full duplex point-to-point communication. The XPC supports a non-operational mode and two operational modes as defined by the LAPB procedure. The non-operational mode is asynchronous disconnect mode (ADM). In this balanced data link mode, the combined station is logically disconnected from the data link and is not permitted to transmit or accept information. Operational modes include asynchronous balanced mode (ABM) and asynchronous mode extended (ABME). A balanced data link allows a combined station to send a command or initiate a response frame transmission without receiving explicit permission from the other station. In ABM/ABME the XPC performs the following operations:

1) Transmission of a chain of information (I) frames when instructed by the host,
2) Transmission of supervisory (S) frames as defined by the X.25 LAPB Recommendation,
3) Transmission of unnumbered (U) commands as required or when instructed by the host, and
4) Transmission of unnumbered (U) responses as defined by the X.25 LAPB Recommendation.

When the transparent mode is selected, the XPC can be configured as a master, a slave or a combined station for full duplex operation. The XPC can support any HDLC/SDLC defined operational mode. All frames are user-generated and are transmitted only when instructed by the host.

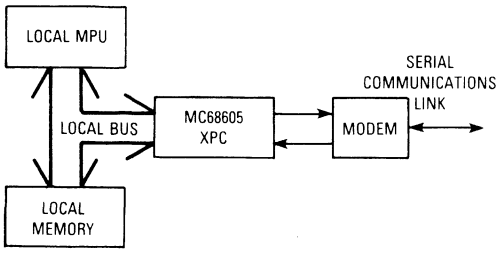


Figure 1. XPC System Configuration

INTERNAL REGISTERS

The XPC has four functional blocks including: serial, DMA, microcode controller, and register-file/ALU. Each of these sections contain user visible and nonvisible registers that define and control the operation of the XPC. A block diagram of the MC68605 is shown in Figure 2.

Because the XPC communicates with the host primarily through shared memory, a minimum number of host processor accessible registers are required. Registers in the XPC fall into two groups. One group is directly accessible by the user and the other group is indirectly accessible through the station table. The directly accessible registers include the command register, semaphore register, interrupt vector register, and data register. The complete register set is shown in Table 1.

SHARED MEMORY STRUCTURES

The host processor communicates with the XPC using three tables located in shared memory (Figure 3). The station table allows the host processor to initialize and update the XPC operating parameters and table pointers, and to receive status and error information. The transmit frame specificaton table queues frames to be transmitted by the XPC, and the receive frame specification table queues available receive buffers for the XPC to store received information frames. The XPC is given a pointer to the station table during initialization. The transmit frame specification table and receive frame specification table pointers are contained in the station table.

STATION TABLE

The station table format is shown in Table 2. The first 19 words of the station table are written by the host processor and are read by the XPC. This portion of the table contains the XPC operating information. The XPC accesses this table area as the result of a host processor command. The next 22 words of the table are written by the XPC and read by the host processor. Some of these entries are written by the XPC as the result of a command while other entries are updated by the XPC when a change occurs. When the XPC accesses the table as the result of a host processor command, it sets the semaphore register to hex 'FF' upon completion of the access. While the XPC is processing a command, the semaphore register is hex 'FE'.

TRANSMIT FRAME SPECIFICATION TABLE

The transmit frame specification table queues transmit frames for the XPC. These frames are stored in memory buffers located throughout memory. The transmit frame specification table contains a sequential list of transmit frame specification blocks. The transmit frame specification blocks describe the location of transmit buffers and provide information about the transmit queue. The transmit table pointer location in the station table points to the first transmit frame specification block. See Figure 4.

When the host processor instructs the XPC to load transmit table pointer, the XPC loads the transmit table

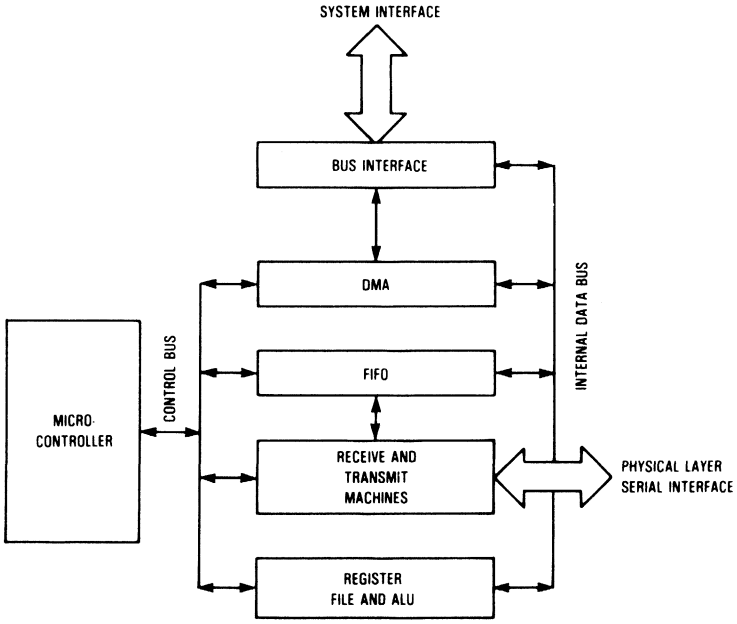


Figure 2. MC68605 Block Diagram

Table 1. XPC Register Set

Register	Description
Directly Accessible Registers	
Command	8-Bit Write Only
Semaphore	8-Bit Read Only
Interrupt Vector	8-Bit Write Only, Read on Host Processor Interrupt Acknowledge Cycle
Data	32-Bit Write Only

Indirectly Accessible Registers	
Register	**Mnemonic**
Station Table Pointer	STP
Station Table Function Code	STFC
Local Address	LA
Remote Address	RA
Hardware Configuration	HC
Station Configuration	SC
Option Bits	OB
Mode Descriptor	MD
Frame Reject Descriptor	FRD
Rx/Host Status	RHS
Tx/Link Status	TLS

Register	Mnemonic
V(S)	V(S)
V(R)	V(R)
Time Scale Divider	TSD
Retries Count	RC
Transmit Table Pointer	TTP
Transmit Table Function Code	TTFC
Transmit Buffer Pointer	TBP
Transmit Buffer Function Code	TBFC
Transmit Buffer Count	TBC
Receive Table Pointer	RTP
Receive Table Function Code	RTFC
Receive Buffer Pointer	RBP
Receive Buffer Function Code	RBFC
Receive Buffer Count	RBC
Time-Out Preset	TOP
Retries Limit	RL
Outstanding Frames Limit	OFL
Pad Time Select	PTS
Last Received N(R)	LRN

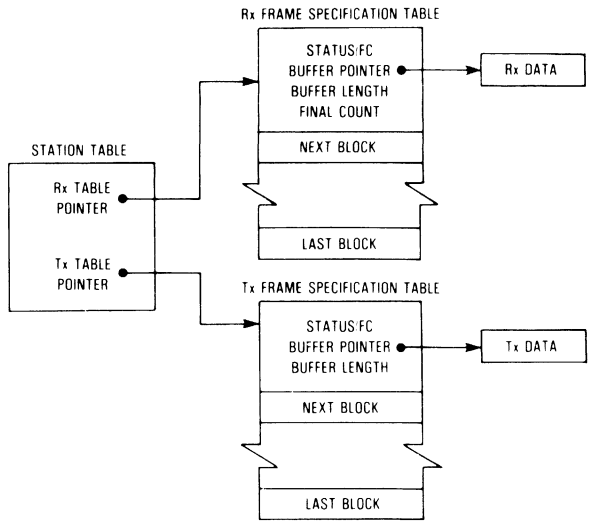


Figure 3. Shared Memory Tables

pointer and transmit table function code registers from the corresponding station table entries. The transmit table pointer register then has the address of the first transmit frame specification block. Before the transmission of each frame, the XPC accesses the current transmit frame specification block to load the transmit buffer function code, transmit buffer address, and the transmit buffer length into the corresponding internal registers. The XPC presents a transmit buffer address and function code to the system to load the information contained in the transmit buffer.

During transparent operation, the XPC accesses the next transmit frame specification block and transmits the corresponding frame buffer until the end of the transmit frame specification table is reached. The XPC updates its internal V(S) register after the transmission of each frame. When all frames have been transmitted, the XPC sets the IFAK bit (information frames acknowledged) in the Tx/ link status register.

During X.25 operation, the XPC accesses the next transmit frame specification block and transmits the corresponding frame buffer according to the X.25 Recommendation until either the outstanding frames limit or the end of the transmit frame specification table is reached. The XPC updates its internal V(S) registers after the transmission of an information frame. The XPC monitors the N(R) of incoming frames until all transmitted frames have been acknowledged. After all frames have been acknowledged, the XPC sets the IFAK bit in the Tx/ link status register.

RECEIVE FRAME SPECIFICATION TABLE

The receive frame specification table queues receive buffers for the XPC. These buffers are stored throughout memory. The receive frame specification table contains a sequential list of receive frame specification blocks. The receive frame specification blocks describe the location of the receive buffers and provide information about the queue. The receive table pointer in the station table points to the first receive frame specification block. See Figure 5.

When the host processor instructs the XPC to load receive table pointer, the XPC loads the receive table function code and receive table pointer registers from the corresponding station table entries. The receive table pointer register then contains the address of the first receive frame specification block. The XPC accesses the receive frame specification block to load the receive buffer function code, receive buffer address, and the receive buffer length into its internal registers. The XPC then presents the receive buffer address and function code to the system to store the received information field in the memory buffer. After reception of a frame, the XPC writes the number of unused bytes in the final count entry in the current receive frame specification block and updates its internal V(R) register. Next the XPC sets the RXI bit (receive information frame) in the Rx/host status register. The XPC accesses the next receive frame specification block to store incoming frames, until the end of the receive frame specification table is reached.

To decrease the possibility of a receive not ready condition due to a lack of available receive buffers, a method is provided for linking receive frame specification tables. When the EOT (end of table) bit is set in a receive frame specification block, the XPC inspects the link bit value. If the link bit is set, then the XPC loads the receive table pointer and FC registers from the corresponding station table locations. The XPC then sets the RTE (receive table ended) bit in the Rx/host status register and issues an

Table 2. Station Table Structure

Word	15 12	11 8	7 4	3 0	
0	Option Bits				
1	Time Out Preset				
2	Time Scale Divider		Pad Time Select		
3	Outstanding Frames Limit		Retries Limit		
4	Rx/Host Mask Bits				
5	Tx/Link Mask Bits				
6	Rx/Host Status Clear Bits				
7	Tx/Link Status Clear Bits				
8	0 0 0 0	0 0 0 0	Local Address		Host Processor Area Read by the XPC Written by Host Processor
9	0 0 0 0	0 0 0 0	Remote Address		
10	0 0 0 0	0 0 0 0	0 0 0 0	RTFC	
11	Receive Table Pointer — High Word				
12	Receive Table Pointer — Low Word				
13	0 0 0 0	0 0 0 0	0 0 0 0	TTFC	
14	Transmit Table Pointer — High Word				
15	Transmit Table Pointer — Low Word				
16	0 0 0 0	0 0 0 0	0 0 0 0	DAFC	
17	Dump Area Pointer — High Word				
18	Dump Area Pointer — Low Word				
19	Rx/Host Status				
20	Tx/Link Status				
21	Mode Descriptor		Frame Reject Descriptor		
22	VS		VR		
23	0 0 0 0	0 0 0 0	0 0 0 0	FUFC	
24	First Unacknowledged Pointer — High Word				
25	First Unacknowledged Pointer — Low Word				
26	0 0 0 0	0 0 0 0	0 0 0 0	NTFC	
27	Next Transmit Pointer — High Word				
28	Next Transmit Pointer — Low Word				XPC Area Read by the Host Processor Written by the XPC
29	0 0 0 0	0 0 0 0	0 0 0 0	NRFC	
30	Next Receive Pointer — High Word				
31	Next Receive Pointer — Low Word				
32	0 0 0 0	0 0 0 0	0 0 0 0	REFC	
33	Receive Bus/Address Error Pointer — High Word				
34	Receive Bus/Address Error Pointer — Low Word				
35	0 0 0 0	0 0 0 0	0 0 0 0	TEFC	
36	Transmit Bus/Address Error Pointer — High Word				
37	Transmit Bus/Address Error Pointer — Low Word				
38	Received FRMR Information Field — Word 1				
39	Received FRMR Information Field — Word 2				
40	Received FRMR Information Field — Word 3				

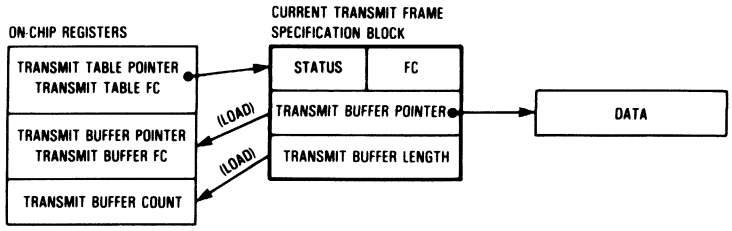


Figure 4. Transmit Frame Specification Table

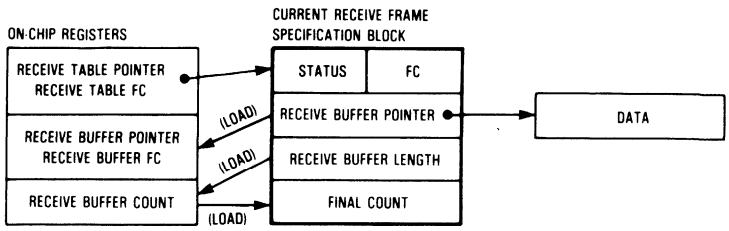


Figure 5. Receive Frame Sepcification Table

3

interrupt if enabled. The link operation can be used to implement a cyclical queue by using the original RTP and FC values in the station table. However, the user must read filled receive buffers expediently to ensure that the XPC does not overwrite the buffers with incoming frames.

During transparent operation, if the link bit is not set in the last receive frame specification block, the XPC sets the RTE bit in the Rx/host status register. If a frame is received before another receive table is assigned via a load RTP command, the XPC sets the NBA (no receive buffer available) bit in the Rx/host register.

During X.25 operation, if the link bit is set in the last receive frame specification block, the XPC transmits a RR frame, and the XPC is ready to receive additional I frames into memory buffers using a new receive frame specification table. If the link bit is not set in the last receive frame specification block, the XPC sets the RTE bit in the Rx/host status register. If an I frame is received before another receive table is assigned via a load RTP command, the XPC sets the NBA (no receive buffer available) bit in the Rx/host status register and transmits a RNR frame.

COMMAND SET

The host processor issues commands to the XPC to perform various functions by writing to the XPC command register. There are 23 commands that fall in the following four categories:

1) Initialization
2) Table Handling
3) Link Handling
4) Test/Diagnostics

INITIALIZATION COMMANDS

Initialization commands configure the XPC for operation after a hardware or software reset. The four initialization commands specify various system attributes, communication protocol options, and the location of the station table in memory.

Reset

The reset command and hardware reset causes the following actions:

- Reset the Receive Channel and Isolate RxD
- Reset the Transmit Channel, Negate $\overline{\text{RTS}}$, and Transmit Ones
- Immediately Relinquish the System Bus
- Set the Interrupt Vector Register to '0F' Hex
- Disable Transmit and Receive Memory Buffers
- Clear all Rx/Host and Tx/Link Status Bits
- Clear all Hardware and Station Configuration Bits
- Clear all Option Bits
- Clear all Mode Descriptor and Frame Reject Descriptor Bits
- Zero Station Table Pointer and Station Table FC Registers
- Zero Transmit Table Pointer and Transmit Table FC Registers
- Zero Receive Table Pointer and Receive Table FC Registers
- Zero Remote Address and Local Address Registers
- Zero V(R), V(S), and Last Received N(R) Registers
- Zero Preset Values and Retries Count Register

Set Station Configuration

The set station configuration command specifies protocol parameters. The command has the following format.

7	6	5	4	3	2	1	0
1	0	1	0	ECRC	0	ECNT	0

ECRC — Extended CRC
- 0 16-Bit CRC
  CRC CCITT ($X^{16}+X^{12}+X^5+1$)
- 1 32-Bit CRC
  ($X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+11$
  $+X^{10}+X^8+X^7+X^5+X^4+X^2+X^1+1$)

ECNT — Extended Control
- 0 Basic Control Field Format (Modulo 8)
- 1 Extended Control Field Format (Modulo 128)

Set Hardware Configuration

The set hardware configuration command defines the data decoding/encoding scheme, DMA burst control, data organization in memory and data bus size. The format of the command is shown below.

7	6	5	4	3	2	1	0
1	1	0	NRZI	BRSC	0	DORGM	BUSW

NRZI — Non-Returned to Zero Invert
- 0 NRZ Decoding/Encoding
- 1 NRZI Decoding/Encoding

BRSC — Burst Control
- 0 DMA Burst is Unlimited
- 1 DMA Burst is Limited to Eight Successive Memory Cycles

DORGM — Data Organization in Memory for a 16-Bit Data Bus System
- 0 Data in Memory is Organized with High-Order Byte in Lower Memory Address (Motorola and IBM Convention)
- 1 Data in Memory is Organized with Low-Order Byte in Lower Memory Address (DEC and Intel Convention)

(This capability is available only for I frame buffers and not for parameters or tables.)

BUSW — Bus Width
- 0 8-Bit Data Bus
- 1 16-Bit Data Bus

Load Function Code

The load FC command writes the function code value in the data register into the station table FC register. This command is issued after the host processor has written the function code to the data register.

Load Station Table Pointer

The load station table pointer command writes the station table address from the data register into the station table pointer register. This command is issued after the host processor has written the station table pointer to the data register.

TABLE HANDLING COMMANDS

The 11 table handling commands cause the XPC to access the station table, transmit frame specification table, or receive frame specification table.

Load Option Bits

The load option bits command loads the option set from the station table into the option bits register.

F	E	D	C	B	A	9	8
0	0	0	0	0	0	0	X.75

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	CRCNOA

X.75 — X.75 Option
- 0 X.25 Operation
- 1 X.75 Operation

CRCNOA — CRC Bypass Option
- 0 Non-octet aligned frames or frames with a CRC error are not accepted
- 1 Non-octet aligned frames or frames with a CRC error are accepted

Load Addresses

The load addresses command loads the local and remote addresses from the station table into the internal XPC registers. After these registers are loaded, the XPC is ready to establish the link. The XPC monitors the receive line and transmits continuous flags.

Load Preset Values

The load preset values command loads the time out preset value, time scale divider, pad time select, outstanding frames limit, and retries limit from the station table into the respective XPC internal registers.

Load Transmit Table Pointer

The load transmit table pointer command loads the transmit table pointer and the transmit table FC from the station table into the corresponding XPC registers and enables the transmission of a chain of information frames.

Continue Transmit

The continue transmit command (hex '95') is used to extend the transmit queue after adding entries to the transmit frame specification table. The user should set the EOT bit in the transmit status location of the last added entry and then clear the EOT bit at the previous end of table. Finally, the user should instruct the XPC to "continue transmit". This command is useful in the case where the XPC has already detected the previous EOT and will not read a new table entry. Instead, it is waiting for all transmitted frames to be acknowledged, and during this period, it will not accept a new load transmit table pointer command.

Load Receive Table Pointer

The load receive table pointer command loads the receive table pointer and the receive table FC from the station table into the corresponding XPC registers and enables the reception of information frames.

Load Station Parameters

This command combines the load option bits, load preset values, and load addresses commands.

Update Status

The update status command allows the host to request current XPC status information.

Clear Tx/Link Status

The clear Tx link status command clears the status bits in the Tx link status register as specified by the Tx link status clear bits in the station table.

3

Clear Rx/Host Status

The clear Rx link status command clears the Rx host status register as specified by the Rx host status clear bits in the station table.

Clear Status

The clear status command clears both the Tx link and Rx host status bits in the respective XPC registers as specified by the Tx link status clear bits and the Rx host status clear bits in the station table.

Dump Parameters

The dump parameters command writes the following XPC parameters into the corresponding status table locations in the order given: Rx host status, Tx link status, mode descriptor, frame reject descriptor, V(R), V(S), first unacknowledged transmit block FC and pointer, next transmit block FC and pointer, and next receive block FC and pointer.

LINK HANDLING COMMANDS

The two link handling commands cause the XPC to set the link to a new operation mode and to automatically handle communication on both channels according to the predefined configuration and option bits.

Start Link

The start link command initiates the link setup procedure.

Stop Link

The stop link command initiates the link disconnect procedure.

TEST/DIAGNOSTICS

The five commands in the text diagnostics category test the XPC circuit and run diagnostics on the link.

Dump Registers

The dump registers command writes the XPC registers to a user specified dump area in external memory.

DMA Transfer

The DMA transfer command tests the handling of parallel data. The XPC reads the data from a transmit memory buffer and writes it to a receive memory buffer. The XPC transfers data from the transmit buffer to the receive buffer via the data register without using the internal transmit or receive FIFOs. The serial link is not affected by this operation.

Serial Loopback

The serial loopback command tests the handling of parallel and serial data. The XPC reads data from the transmit memory buffer into the transmit FIFO. The data is then serialized and shifted internally into the receive FIFO and onto the TxD line. Finally the data is stored in the receive memory buffer. $\overline{\text{RTS}}$ is not active during serial loopback.

Monitor

The monitor command allows the XPC to check the communication channel by reading/writing the entire frame from/to memory. The monitor command may be used to perform an external loopback test of the system or to implement any HDLC/SDLC operation mode where all frames are user generated. The XPC transmits and/or receives multiple information frames using the transmit and receive frame specification tables until an end monitor command is received.

In each transmit buffer the user places the address, control, and data (if any) fields. The XPC only provides framing, zero insertion, and CRC for each frame. On the receive side, the XPC strips off flags, handles zero deletion, and writes the address control and data fields into the receive buffer. The received CRC is also appended to the end of each memory buffer and is verified by the XPC.

End Monitor

The end monitor command terminates the monitor command.

XPC IMPLEMENTATION OF LAPB PROTOCOL

INITIALIZATION PROCEDURE

The XPC enters the initialization procedure as the result of a hardware or software reset. During this initialization, the station table address and function code (FC), system configuration information, and the XPC interrupt vector are loaded by the XPC under the direction of the host, as shown in the sample program below. Internal XPC registers directly accessed during the initialization procedure are the command register (CR), data register (DR), interrupt vector register (IV), and semaphore register (SR).

RESET

Repeat: Read Semaphore Register Until it is 'FF'
Write CR: Set Hardware Configuration
Repeat: Read Semaphore Register Until it is 'FF'
Write CR: Set Station Configuration
Repeat: Read Semaphore Register Until it is 'FF'
Write DR: 4-Bit Function Code Value for Station Table Access
Write CR: Load Function Code
Repeat: Read Semaphore Register Until it is 'FF'
Write DR: 32-Bit Address of Station Table
Write CR: Load Station Table Pointer (STP)
Repeat: Read Semaphore Register Until it is 'FF'
Write IV: Load Interrupt Vector
Write CR: Load Station Table Parameters
Repeat: Read Semaphore Register Until it is 'FF'

INFORMATION FRAME TRANSMISSION

After the XPC enters asynchronous balanced mode (ABM) or asynchronous balanced mode extended (ABME), the host processor can instruct the XPC to transmit a chain of information frames by issuing the load transmit table pointer command. In response the XPC loads the transmit table pointer and the transmit table function code from the station table into its internal registers. Next the XPC loads the first transmit buffer pointer, transmit buffer function code, and transmit buffer count from the transmit frame specification table into the corresponding XPC registers. Now the XPC is ready to build the first frame.

The remote address is copied from the remote address register into the XPC transmit FIFO. Next the control field is generated and placed in the FIFO. The information field pointed to by the transmit buffer pointer register is then read from the memory buffer into the transmit FIFO until the transmit buffer count is satisfied. A frame check sequence is attached to complete the frame. Zero insertion is performed throughout the transmission. After frame transmission the send state variable, V(S), is updated and timer T1 is started (if it is not already running) to determine when the programmed time period permitted for a reply to be received has elapsed.

This transmission sequence repeats for each frame until the end of the transmit chain is reached, or until the outstanding frames limit is reached. The XPC continues to transmit any available information frames even when the XPC receiver is in the busy condition. The XPC prematurely terminates frame transmission if a link command interrupts the information frame transmission or an error condition arises.

Transmission begins when six bytes are present in the transmit FIFO. Transmission can begin when less than six bytes are present in the FIFO if the entire frame is less than six bytes in length. Between frames the XPC transmits the user selected number of pad flags. Additional flags are transmitted if the required number of bytes are not present in the transmit FIFO. While transmitting an information frame, the XPC requests the bus when there are at least six empty bytes in the transmit FIFO.

INFORMATION FRAME RECEPTION

The host processor enables information reception by instructing the XPC to load receive table pointer. The XPC will load the receive table pointer and function code into its internal registers. Next the receive buffer pointer and function code, and the receive buffer count are loaded into the corresponding XPC registers. The XPC is now ready to receive information frames.

The address field of an incoming I frame is compared to the local address register and the remote address register. If the address does not match the local or remote address, the frame is ignored. If the address field matches the remote address, a frame reject (FRMR) is transmitted and the W (invalid or unimplemented control field) bit of the frame reject descriptor register (FRD) is set. If the address field matches the local address, the frame is accepted by the XPC and the received N(R) acknowledges previously transmitted I frames.

Next, the send sequence number N(S) of the incoming frame is compared to the XPC internal receive state variable V(R). If the frame is in sequence, then the information field is transferred through the receive FIFO to the receive memory buffer. Out-of-sequence frames are rejected.

Lastly, the XPC performs a CRC check on the incoming information frame. If an error-free frame is received, the XPC acknowledges the frame reception with a supervisory frame (receive ready RR or receive not ready RNR) or with an updated receive sequence number N(R) in the next information frame.

Zero deletion is performed throughout the reception process. The XPC requests the bus when there are six bytes in the receive FIFO. Only a single frame can reside in the receive FIFO. Frames are received in sequence as long as memory buffers are available.

STATE TABLE

The XPC state table (Figure 6 which is located on the last page of this document) is a detailed description of the XPC implementation of the LAPB procedure. The state table defines the various XPC states based on command frames received (no errors), response frames received (no errors), and miscellaneous inputs received. For example, referring to Figure 6, if the command received was an RR with the poll bit set to one while in the remote station busy condition (state 9), then the XPC responds with an RR with the final bit set to a one and changes to information transfer (state 5).

XPC TRANSPARENT MODE OF OPERATION

The XPC transparent mode of operation can be used to implement a variety of bit oriented protocols. The following paragraphs describe the XPC transparent mode of operation.

INITIALIZATION PROCEDURE

The XPC enters the initialization procedure as the result of a hardware or software reset. During initialization, the station table address and function code, system configuration information, and the XPC interrupt vector should

be loaded by the XPC under the direction of the host, as shown in the sample program below. Note that the XPC will not come out of hardware or software reset without the system clock and the transmit clock. The transmit clock is used to initialize the serial section of the chip.

ENTERING TRANSPARENT OPERATION

Transparent operation is entered when the host issues the monitor command. After the monitor command, the XPC asserts $\overline{RTS}$, transmits flags, and monitors RxD. Since handshaking between nodes is not possible before the monitor command is executed, the host processor at each node must issue the monitor command in order for the two nodes to communicate.

3

FRAME TRANSMISSION

After the monitor command is issued, the XPC begins transmission of frames only after receiving a load transmit table pointer command from the host. All frames are user-generated and may contain user-provided address, control, and data fields or may contain only a data field. After the host issues the load transmit table pointer command, the XPC loads the transmit table pointer and the transmit table funtion code from the station table into its internal registers. Next, the XPC loads the first trasmit buffer pointer, transmit buffer function code, and transmit buffer count from the transmit frame specification table into the corresponding XPC registers. Now the XPC is ready to transmit the first frame.

The frame pointed to by the transmit buffer pointer register is read from the memory buffer into the transmit FIFO until the transmit buffer count is satisfied. An XPC-generated frame check sequence is then attached to complete the frame. After each frame transmission, the internal V(S) register is incremented without regard to the frame type. This transmission sequence repeats for each frame until the end of the transmit chain is reached. Zero insertion is performed throughout the transmission process.

In transparent operation, the XPC transmits frames until the end of the transmit specification table is reached. After the last frame is transmitted, the XPC sets the IFAK (information frames acknowledged) bit in the Tx/link status register to indicate the end of the transmit table. The XPC does not analyze any incoming frames for acknowledgements or link control information during transparent operation. The only errors reported in the Tx/link status register are address error, bus error, clear-to-send lost, and underrun.

Transmission begins when six bytes are present in the transmit FIFO. Transmission can begin when less than six bytes are present in the FIFO, if the entire frame is less than six bytes in length. Between frames, the XPC transmits the user-selected number of pad flags. Additional pad flags are transmitted if the required number of bytes are not present in the transmit FIFO for transmission to begin. While transmitting a frame, the XPC requests the bus when there are at least six empty bytes in the transmit FIFO.

FRAME RECEPTION

The host processor enables frame reception by instructing the XPC to load receive table pointer. The XPC then loads the receive table pointer and function code into its internal registers. Next, the receive buffer pointer and function code, and the receive buffer count are loaded into the corresponding XPC registers. The XPC is now ready to receive frames.

The XPC does not analyze the address and control fields of incoming frames, but does perform a CRC check on incoming frames. After the flags are stripped off, the entire frame including CRC is written into the current receive buffer and the RXI (received information frame) bit is set in the Rx/host status register. If a frame is received with a CRC error, the XPC sets the E bit in that frame's receive specification block. After a frame is received, the XPC increments V(R) without regard to frame type. Zero deletion is performed throughout the reception process.

In transparent operation, the XPC continues to receive frames until the end of the receive specification table is reached. The XPC then sets the RTE (receive table ended) bit in the Rx/host status register.

The XPC requests the bus when there are six bytes in the receive FIFO. Only a single frame can reside in the receive FIFO. Frames are received in sequence as long as memory buffers are available.

STATE	I FRAME WITH POLL	I FRAME W/O POLL	RR WITH POLL	RR W/O POLL	REJ WITH POLL	REJ W/O POLL	RNR WITH POLL	RNR W/O POLL	SABM WITH OR W/O POLL	DISC WITH OR W/O POLL	RR WITH FINAL	RR W/O FINAL	REJ WITH FINAL	REJ W/O FINAL	RNR WITH FINAL
S1 DISCONNECTED	DM, F = 1		DM, F = 1		DM, F = 1		DM, F = 1		UA, F = P TO S5	DM, F = P					
S2 LINK SETUP									UA, F = P	DM, F = P TO S1					
S3 FRAME REJECT	FRMR, F = 1	FRMR, F = 0	FRMR, F = 1	FRMR, F = 0	FRMR, F = 1	FRMR, F = 0	FRMR, F = 1	FRMR, F = 0	UA, F = P TO S5	UA, F = P TO S1					
S4 DISCONNECT REQUEST									DM, F = P TO S1	UA, F = P					
S5 INFORMATION TRANSFER	RR, F = 1	••	RR, F = 1	••	RR, F = 1	••	RR, F = 1 TO S9	RR, F = 0 TO S9	UA, F = P	UA, F = P TO S1	(UNXF) SABM TO S2	•••	(UNXF) SABM TO S2	•••	(UNXF) SABM TO S2
S6 REJ FRAME SENT	RR, F = 1 TO S5	•• TO S5	RR, F = 1	••	RR, F = 1	••	RR, F = 1 TO S14	RR, F = 0 TO S14	UA, F = P TO S5	UA, F = P TO S1	(UNXF) SABM TO S2	•••	(UNXF) SABM TO S2	•••	(UNXF) SABM TO S2
S7 WAITING ACKNOWLEDGE MENT	RR, F = 1	RR, F = 0	RR, F = 1	RR, F = 0	RR, F = 1	• RR, F = 0	RR, F = 1 TO S12	RR, F = 0 TO S12	UA, F = P TO S5	UA, F = P TO S1	••• TO S5		••• TO S5		TO S9
S8 STATION BUSY	RNR, F = 1	RNR, F = 0	RNR, F = 1	•N	RNR, F = 1	•N	RNR, F = 1 TO S10	RNR, F = 0 TO S10	UA, F = P	UA, F = P TO S1	(UNXF) SABM TO S2	•••	(UNXF) SABM TO S2	•••	(UNXF) SABM TO S2
S9 REMOTE STATION BUSY	RR, F = 1	RR, F = 0	RR, F = 1 TO S5	•• TO S5	RR, F = 1 TO S5	•• TO S5	RR, F = 1	RR, F = 0	UA, F = P TO S5	UA, F = P TO S1	(UNXF) SABM TO S2	••• TO S5	(UNXF) SABM TO S2	••• TO S5	(UNXF) SABM TO S2
S10 BOTH STATIONS BUSY	RNR, F = 1	RNR, F = 0	RNR, F = 1 TO S8	•N TO S8	RNR, F = 1 TO S8	•N TO S8	RNR, F = 1	RNR, F = 0	UA, F = P TO S8	UA, F = P TO S1	(UNXF) SABM TO S2	••• TO S8	(UNXF) SABM TO S2	••• TO S8	(UNXF) SABM TO S2
S11 WAITING ACK AND STATION BUSY	RNR, F = 1	RNR, F = 0	RNR, F = 1	RNR, F = 0	RNR, F = 1	RNR, F = 0	RNR, F = 1 TO S13	RNR, F = 0 TO S13	UA, F = P TO S8	UA, F = P TO S1	••• TO S8		••• TO S8		TO S10
S12 WAITING ACK AND REMOTE STATION BUSY	RR, F = 1	RR, F = 0	RR, F = 1 TO S7	RR, F = 0 TO S7	RR, F = 1 TO S7	RR, F = 0 TO S7	RR, F = 1	RR, F = 0	UA, F = P TO S5	UA, F = P TO S1	••• TO S5	TO S7	••• TO S5	TO S7	TO S9
S13 WAITING ACK AND BOTH STATIONS BUSY	RNR, F = 1	RNR, F = 0	RNR, F = 1 TO S11	RNR, F = 0 TO S11	RNR, F = 1 TO S11	RNR, F = 0 TO S11	RNR, F = 1	RNR, F = 0	UA, F = P TO S8	UA, F = P TO S1	••• TO S8	TO S11	••• TO S8	TO S11	TO S10
S14 REJ FRAME SENT AND REMOTE STATION BUSY	RR, F = 1 TO S9	RR, F = 0 TO S9	RR, F = 1 TO S6	•• TO S6	RR, F = 1 TO S6	•• TO S6	RR, F = 1	RR, F = 0	UA, F = P TO S5	UA, F = P TO S1	(UNXF) SABM TO S2	••• TO S6	(UNXF) SABM TO S2	••• TO S6	(UNXF) SABM TO S2

•• If I available then Tx I frame else Tx RR, F = 0
••• If I available then Tx I frame else do nothing
•N If I available then Tx I frame else Tx RNR, F = 0
••N If P = 1 then Tx RNR, F = 1 else if I available then Tx I frame else Tx RNR, F = 0
•FR If P = 1 then Tx FRMR, F = 1 else if P = 0 then Tx FRMR, F = 0 else do nothing
•DM If P = 1 then Tx DM, F = 1 else do nothing
•J If no REJ FRAME is outstanding then transmit REJ, F = P else if P = 1 then Tx RR, F = 1 else do nothing
••J If the I field of a correctly received frame has been discarded (due to the busy condition) then Tx REJ, F = 0 else Tx RR, F = 0
— Do nothing
X This event never occurs in this state
UNXF Unexpected final bit

Figure 6. XPC State Diagram

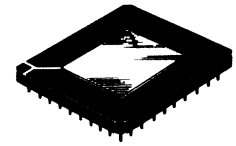
RNR W/O FINAL	UA WITH OR W/O FINAL	DM WITH FINAL	DM W/O FINAL	FRMR WITH OR W/O FINAL	LOCAL START COMMAND	LOCAL STOP COMMAND	STATION BECOMES BUSY	BUSY CONDITION CLEAR	T1 EXPIRES	N2 - T1 IS EXCEEDED	NS SEQUENCE ERROR	INVALID NR RECEIVED	UNRECOGNIZED FRAME RECEIVED
—	—	SABM TO S2	SABM TO S2	—	SABM TO S2	DISC TO S4	X	—	X	X	*DM	*DM	*DM
—	TO S5	TO S1	—	—	X	X	X	—	SABM	TO S1	—	—	—
—	-	SABM TO S2	SABM TO S2	SABM TO S2	SABM TO S2	DISC TO S4	X	—	FRMR	SABM TO S2	*FR	*FR	*FR
—	TO S1	TO S1	-	-	X	X	X	-	DISC	TO S1		—	—
TO S9	SABM TO S2	SABM TO S2	SABM TO S2	SABM TO S2	SABM TO S2	DISC TO S4	RNR, F = P TO S8	X	RR, P = 1 TO S7	SABM TO S2	*J TO S6	FRMR(Z) TO S3	FRMR(W) TO S3
TO S14	SABM TO S2	SABM TO S2	SABM TO S2	SABM TO S2	SABM TO S2	DISC TO S4	RNR, F = P TO S8	X	RR, P = 1 TO S7	SABM TO S2	IF P = 1 Tx RR, F = 1	FRMR(Z) TO S3	FRMR(W) TO S3
TO S12	SABM TO S2	SABM TO S2	SABM TO S2	SABM TO S2	SABM TO S2	DISC TO S4	RNR, F = P TO S11	X	RR, P = 1	SABM TO S2	*J	FRMR(Z) TO S3	FRMR(W) TO S3
TO S10	SABM TO S2	SABM TO S2	SABM TO S2	SABM TO S2	SABM TO S2	DISC TO S4	X	**J TO S5	RNR, P = 1 TO S11	SABM TO S2	RNR, F = P	FRMR(Z) TO S3	FRMR(W) TO S3
—	SABM TO S2	SABM TO S2	SABM TO S2	SABM TO S2	SABM TO S2	DISC TO S4	RNR, F = P TO S10	X	RR, P = 1 TO S12	SABM TO S2	*J TO S14	FRMR(Z) TO S3	FRMR(W) TO S3
	SABM TO S2	SABM TO S2	SABM TO S2	SABM TO S2	SABM TO S2	DISC TO S4	X	**J TO S9	RNR, P = 1 TO S13	SABM TO S2	RNR, F = P	FRMR(Z) TO S3	FRMR(W) TO S3
TO S13	SABM TO S2	SABM TO S2	SABM TO S2	SABM TO S2	SABM TO S2	DISC TO S4	X	**J TO S7	RNR, P = 1	SABM TO S2	RNR, F = P	FRMR(Z) TO S3	FRMR(W) TO S3
—	SABM TO S2	SABM TO S2	SABM TO S2	SABM TO S2	SABM TO S2	DISC TO S4	RNR, F = P TO S13	X	RR, P = 1	SABM TO S2	*J	FRMR(Z) TO S3	FRMR(W) TO S3
—	SABM TO S2	SABM TO S2	SABM TO S2	SABM TO S2	SABM TO S2	DISC TO S4	X	**J TO S12	RNR, P = 1	SABM TO S2	RNR, F = P	FRMR(Z) TO S3	FRMR(W) TO S3
—	SABM TO S2	SABM TO S2	SABM TO S2	SABM TO S2	SABM TO S2	DISC TO S4	RNR, F = P TO S10	X	RR, P = 1 TO S12	SABM TO S2	IF P = 1 Tx RR, F = 1	FRMR(Z) TO S3	FRMR(W) TO S3

Figure 6. XPC State Diagram

MOTOROLA

MC68606
Technical Summary

Multi-Link LAPD (MLAPD) Protocol Controller



RC SUFFIX
PIN GRID ARRAY
(84 PIN)
CASE 793

3

The Motorola MC68606 Multi-Link LAPD (MLAPD) protocol controller is an integrated circuit implementing the link access procedure (LAPD) protocol. LAPD is the proposed protocol for use at the link layer (ISO-Layer 2) for both signalling and data transfer applications in Integrated Services Digital Network (ISDN) configurations. The LAPD protocol is specified in CCITT Recommendation Q.920/Q.921.

Current product implementations of this link level protocol are accomplished with firmware. This significantly loads the local processor, and presents limitations to both the maximum potential throughput of data and to the number of logical links which may be supported by such packet data interfaces. A generic view of where the MLAPD device can be used to interconnect a diversity of data endpoints in a high speed packet switch network is shown in Figure 1. The data links illustrated could differ functionally and provide data rates in the range of 64 kbps to 2.048 Mbps.

The MLAPD functions as an intelligent peripheral device to a central processing unit (CPU) in a microcomputer system. An on-chip DMA controller transfers data packets to and from a buffer memory. A microcoded buffer management scheme queues packets during transmission and reception. All link management duties are handled by the MLAPD device to maximize the bandwidth available for CPU operation and to increase the throughput for packet data transfer. This VLSI implementation provides a cost effective solution, while encouraging a universal implementation of the LAPD protocol. Key features of the MLAPD device include:

- Full Implementation of CCITT Recommendation Q.920/Q.921 Link Access Procedure (LAPD) with Independent Generation of Commands and Responses for Each Logical Link
- Control of up to 8192 Logical Links Using a Memory-Based Architecture, Wherein the Protocol Controller and the Supervising Microprocessor Communicate Through Shared Memory
- Reliable, Interleaved Data Transfers for Multiple Logical Links with the Following Protocol Actions:
  - HDLC framing with zero-bit insertion/deletion for a serial bit stream; or optional parallel assist mode where zero insertion/deletion is disabled and frame delineation is provided by external pins for supporting a parallel interface to the physical level.
  - Error control using a 16-bit CRC.
  - Flow control to prevent data from accumulating at the receiving end faster than the data can be processed.
- Termination of a Non-Channelized Serial Bit Stream with an Aggregate Rate in Excess of 2.048 Mbps or Optional Memory-to-Memory Operation Allowing the MLAPD to Act as a LAPD Controller Independent of the System's Physical Level Characteristics

PIN GRID ARRAY

	1	2	3	4	5	6	7	8	9	10
K	CLK	GND	RxD	V_{DD}	RCLK	V_{DD}	A23	A21	GND	A18
J	V_{DD}	GND	MOTO/$\overline{INT}$	$\overline{RTS}$/$\overline{TSTART}$	TxD	V_{DD}	A20	A19	A17	A15
H	$\overline{RESET}$	$\overline{RETRY}$	GND	$\overline{CTS}$/$\overline{RSTART}$	GND	TCLK	A22	A16	V_{DD}	A14
G	$\overline{IACK}$ ($\overline{INTA}$)	$\overline{BERR}$	$\overline{HALT}$					A13	A12	GND
F	$\overline{BG}$ (HOLDA)	$\overline{BR}$ (HRQ)	$\overline{IRQ}$ (INTR)		BOTTOM VIEW			A9	A11	A10
E	R/$\overline{W}$ ($\overline{WR}$)	GND	$\overline{DTACK}$ (READY)					A8	V_{DD}	GND
D	$\overline{BGACK}$ ($\overline{RD}$)	V_{DD}	$\overline{UDS}$/A0 (A0)					V_{DD}	A5	A7
C	$\overline{LDS}$ ($\overline{BHE}$)	$\overline{CS}$	$\overline{AS}$	GND	V_{DD}	D10	D12	A1	GND	A6
B	GND	D0	D2	D5	GND	D9	GND	D15	A2	A4
A	D1	D3	D4	D6	D7	D8	D11	D13	D14	A3

This document contains information on a new product. Specifications and information herein are subject to change without notice.

NP426

- Supports User Prioritization of I Frame and XID/UI Frame Transmission
- Supports Optional Receive and Transmit of a User-Defined, Non-Standard LAPD Unnumbered (U) Frame
- On-Chip, Content-Addressable Memory (CAM) Provides Address Translation for Up to 16 Logical Links. When Supporting More Than 16 Logical Links, Translation is Provided Via a Translation Table in Shared Memory
- Provides Error/Statistical Counters and Maskable Interrupts to the Level 3 Process
- Supports Optional Non-Protocol Mode on a Per-Logical Link Basis, Which Allows the Host to Receive and Transmit Frames Without Application of the LAPD Procedures by the MLAPD
- Supports Promiscuous Receive Mode in Which the MLAPD Receives All Frames From the Line and Transfers the Entire Frame to Memory
- System Interface Tailored for Different Microprocessor System Implementations:
  - Motorola M68000 and Intel iAPX86 Family Bus Interface Options
  - 8- and 16-Bit Data Bus Support
  - Direct Addressing of 16 Mbytes of System Memory
- Available in 12.5 MHz and 16.67 MHz System Clock Versions
- 84 Lead PGA and PLCC J-Lead Surface Mount Packages
- 1.5 Micron HCMOS Technology

3

GENERAL DESCRIPTION

SUBSYSTEM ENVIRONMENT

The MLAPD protocol controller provides simultaneous control of a maximum of 8192 logical links, while under the overall supervision of a microprocessor. Refer to Figure 2. The host can be any 8- or 16-bit microprocessor that supports general multimaster bus capability, operating with either the Motorola M68000 family or the Intel iAPX86 family bus interface definition. The desired MLAPD bus operation mode is determined by the level on the Motorola/Intel Mode pin.

The MLAPD serial interface provides HDLC-type framing functions for the bit stream entering/exiting the full duplex serial interface. NRZ data encoding/decoding is implemented. The MLAPD may also be optionally configured to interface to a physical level which implements a parallel interface, such as a backplane in a switching controller or host computer system. In this mode zero insertion/deletion is disabled and flag sequences are not generated. Instead, the $\overline{RTS}$ and $\overline{CTS}$ signals function as $\overline{TSTART}$ and $\overline{RSTART}$, respectively, to delineate a frame for the transmit and receive data lines.

Shared Memory Control Components

The communication between the microprocessor and the protocol controller is established through command and data block structures stored in shared memory. The shared memory

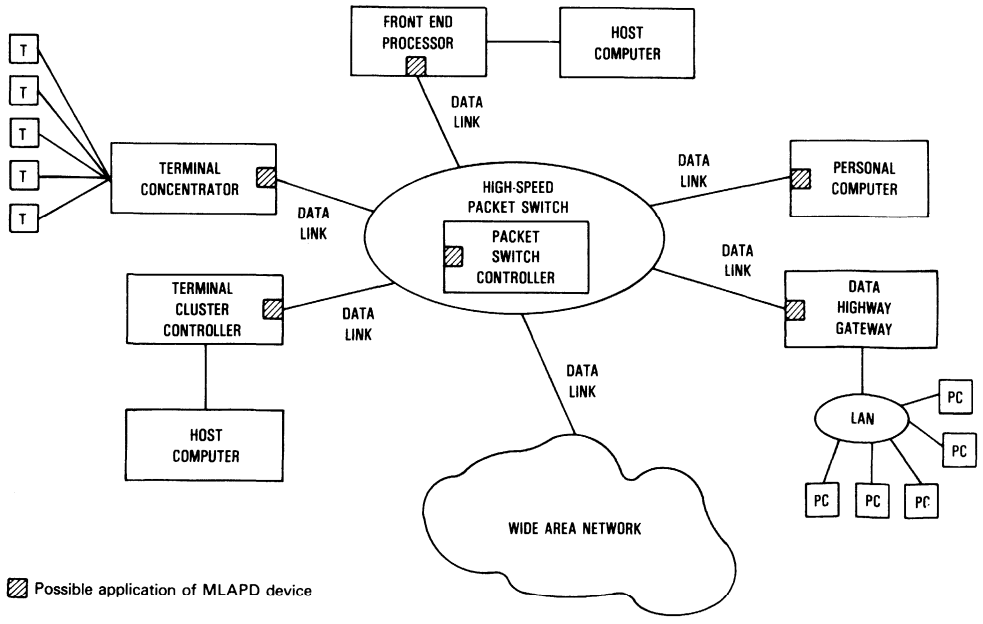


Figure 1. High Speed Data Switching

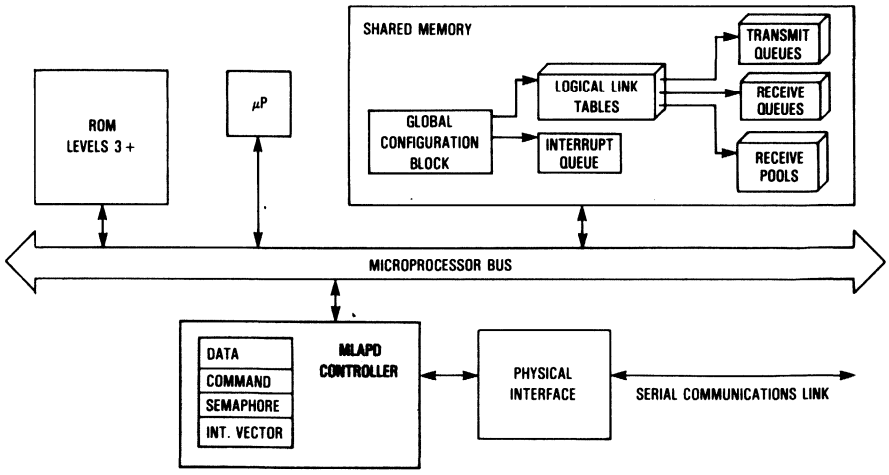


Figure 2. MLAPD System Environment

structures include the Global Configuration Block (GCB), Logical Link Tables (LLTs), receive and transmit data structures, and an Interrupt Queue. In addition to these structures, there are also four memory tables required for the implementation of the LAPD procedure. These tables include the Match Table, LLID-LLT Table, Timer Table, and the Level 2 Queue. Figure 3 shows a concise summary of the functions performed by these blocks.

BLOCK TYPE	PURPOSE
GLOBAL CONFIGURATION BLOCK	CONTAINS POINTERS TO OTHER MEMORY TABLES. CONTAINS GLOBAL INFORMATION FOR ALL LOGICAL LINKS. CONTAINS USER SYSTEM AND LINK OPTIONS.
LOGICAL LINK TABLES	CONTAINS SPECIFIC LINK CONTROL PARAMETERS FOR THE GIVEN LINK. ALSO CONTAINS POINTERS TO THE RECEIVE/TRANSMIT QUEUES. CONTAINS WORKING PROTOCOL STATUS FOR THE LINK.
RECEIVE AND TRANSMIT QUEUES	CONTAINS LINKED LIST OF RECEIVE AND TRANSMIT FRAME DESCRIPTORS FOR I, UI, AND XID FRAMES.
RECEIVE POOLS	LINKED LIST OF AVAILABLE RECEIVE FRAME DESCRIPTORS WITH ASSOCIATED DATA BUFFERS.
INTERRUPT QUEUE	CONTAINS TIME SEQUENTIAL LIST OF INTERRUPT STATUS FOR EACH INTERRUPT EVENT.
MATCH TABLE	CONTAINS TRANSLATION FROM DATA LINK CONNECTION IDENTIFIER (DLCI) TO LOGICAL LINK IDENTIFIER (LLID) FOR INCOMING FRAMES (EXPANDED OPERATION MODE).
LLID TO LLT TABLE	TRANSLATES LLID INTO THE ADDRESS OF THE CORRESPONDING LOGICAL LINK TABLE.
LEVEL 2 TRANSMIT QUEUE	CONTAINS LEVEL 2 SUPERVISORY AND UNNUMBERED FRAMES GENERATED BY THE MLAPD.
TIMER TABLE	IMPLEMENTS T200/T203 FOR ALL LOGICAL LINKS THAT ARE IN MULTIPLE FRAME ESTABLISHED MODE OF OPERATION.

Figure 3. Shared Memory Guide

During initialization, the host processor specifies protocol and system parameters and the addresses of the various memory tables via the Global Configuration Block. Then the host programs the MLAPD controller with the address of the Global Configuration Block and commands the MLAPD to initialize itself by loading its internal registers from the shared memory tables. After this point, the host and the MLAPD communicate primarily via software flags and an Interrupt Queue in shared memory.

Command Structure Overview

The host issues a command to the MLAPD by first writing the command arguments (if any) into the command parameter fields in the Global Configuration Block in shared memory. Next, the host performs a write operation to enter the command into the on-chip command register. Upon reception of a command, the MLAPD sets its on-chip semaphore register to the value 'FE' hex. After either command completion or command acceptance, depending on the specific command, the MLAPD sets the value of the semaphore register to 'FF' hex. The host must always read the semaphore register before writing a new command.

There are 32 commands which belong to one of the following five categories:

Initialization—These commands configure the MLAPD for operation after a hardware or software reset by specifying the system data bus width and the location of the Global Configuration Block in memory.

Host/MLAPD Interface—These commands instruct the MLAPD to perform operations that are not explicitly named in the LAPD protocol, but which are required by the host to interface with the MLAPD.

Protocol Handling—These commands are the primitives explicitly defined in the LAPD protocol. The protocol commands allow the host to set-up and resume link operation, as well as to control the flow of frames on the link.

Protocol Extension Handling—These commands are not defined in the LAPD protocol. These commands allow the host to intercede in the normal flow of the MLAPD protocol processing.

Test/Diagnostics—These commands allow the host to access all internal MLAPD registers or to test the DMA interface.

Figure 4 summarizes the MLAPD command set.

Exception Processing

An Interrupt Queue is located in shared memory to support the speed requirement of reporting many interrupting events occurring in rapid succession across the various active logical links. Each entry in this Interrupt Queue consists of a logical link identification number (LLID) if applicable, and a cause indication. Each of the 31 potential interrupt sources, with the exception of bus error/address error and interrupt queue overflow, may be individually masked by the host to prevent the reporting of a specific event.

After the MLAPD has written an entry into the Interrupt Queue, a hardware interrupt request may be activated. If polled operation is desired, this external interrupt indication is disabled by the host during MLAPD initialization. If an interrupt acknowledgement cycle is to be implemented in an interrupt driven system, the interrupt_vector register must be programmed by the host during the initialization procedure. The interrupt_vector register is located on-chip and allows the MLAPD to return an indication of the interrupt cause as part of an interrupt acknowledgement cycle on the system bus. The two possible vectors reported across the bus are:

The two possible vectors reported across the bus are:

- Normal Interrupt
- Severe Interrupt (bus error/address error)

Interrupt information is written into the Interrupt Queue to fully identify the specific cause of the interrupt in either a polled or interrupt driven system. Interrupts are the principle mechanism to report protocol events and errors (including error thresholds exceeded). Since the Interrupt Queue is circular and of limited size, the host is responsible for "reading" the interrupt information and maintaining free entries to record new interrupt events.

Initialization Overview

As a part of initialization, the host must:

- Prepare the Global Configuration Block (GCB). The host specifies the addresses of the various memory tables in the GCB. The GCB is also programmed with several global parameters that are required to process the LAPD protocol for all links.
- Clear these tables: Match Table, Interrupt Queue, and Timer Table.
- Prepare the Logical Link Table(s) (LLT) with the local parameters for the link(s) in service.
- Construct receive pool(s) of frame descriptors.

COMMAND GROUP	COMMAND	FUNCTIONAL DESCRIPTION
INITIALIZATION	RESET	SOFTWARE RESET.
	SET_BUS_WIDTH_8	DATA BUS WIDTH IS 8 BITS.
	SET_BUS_WIDTH_16	DATA BUS WIDTH IS 16 BITS.
	INIT	MLAPD LOADS REGISTERS FROM THE GCB.
HOST/MLAPD INTERFACE	OFF-LINE	MLAPD ONLY EXECUTES HOST COMMANDS.
	ON-LINE	MLAPD EXECUTES COMMANDS, RECEIVES FRAMES, AND TRANSMITS FRAMES.
	RELOAD	MLAPD LOADS REGISTERS FROM RELOADABLE AREA OF GCB.
	DUMP_STATISTICS	MLAPD WRITES GLOBAL COUNTERS TO SPECIFIED MEMORY AREA.
	PRESET_STATISTICS	MLAPD LOADS GLOBAL COUNTERS FROM STATISTICS THRESHOLD AREA OF GCB.
	ENABLE_IRQ	ALL PENDING INTERRUPT ENTRIES HANDLED. ENABLE EXTERNAL INTERRUPT SIGNAL.
	ASSIGN_POOL_POINTER	HOST HAS CREATED A NEW RECEIVE POOL.
PROTOCOL	MDL_ASSIGN_REQUEST	PLACE SPECIFIED LOGICAL LINK IN THE TEI_ASSIGN STATE.
	DL_ESTABLISH_REQUEST	SET-UP LINK. LINK ENTERS MULTIPLE FRAME ESTABLISHED MODE.
	DL_DATA_REQUEST	REQUEST TRANSMISSION OF AN I FRAME QUEUE FOR THE SPECIFIED LOGICAL LINK.
	RELINK_REQUEST	FRAMES WERE ADDED TO A QUEUE IN WHICH ALL FRAMES WERE 'Tx AWAITING ACK'.
	GLOBAL_XID/UI_REQUEST	REQUEST TRANSMISSION OF XID/UI FRAMES IN THE GLOBAL XID/UI QUEUE.
	XID/UI_QUEUE_0_REQUEST	REQUEST TRANSMISSION OF XID/UI FRAMES IN XID/UI_QUEUE_0.
	XID/UI_QUEUE_1_REQUEST	REQUEST TRANSMISSION OF XID/UI FRAMES IN XID/UI_QUEUE_1.
	MDL_ERROR_RESPONSE	INDICATION THAT NO DLCI ASSIGNED. THE LOGICAL LINK IS IN TEI_UNASSIGN STATE.
	DL_RELEASE_REQUEST	RELEASE LINK FROM THE MULTIPLE FRAME ESTABLISHED MODE.
	MDL_REMOVE_REQUEST	REMOVE SPECIFIED LOGICAL LINK FROM LAPD SERVICE.
PROTOCOL EXTENSION	ACTIVATE_LL	PLACE SPECIFIED LOGICAL LINK IN THE TEI_UNASSIGN STATE.
	DEACTIVATE_LL	REMOVE DLCI-LLID PAIR. PLACE LOGICAL LINK IN TEI_UNASSIGN STATE.
	REMOTE_STATUS_REQUEST	SEND FRAME WITH P BIT SET TO CHECK REMOTE STATION STATUS FOR SPECIFIED LINK.
	SET_LOCAL_BUSY	SPECIFIED LOGICAL LINK ENTERS THE LOCAL BUSY CONDITION.
	CLEAR_LOCAL_BUSY	SPECIFIED LOGICAL LINK EXITS THE LOCAL BUSY CONDITION.
	STOP_TX_I	STOP TRANSMISSION OF THE SPECIFIED LOGICAL LINK'S I TRANSMIT QUEUE.
	STOP_GLOBAL_XID/UI	STOP TRANSMISSION OF FRAMES IN THE GLOBAL XID/UI QUEUE.
	STOP_XID/UI_QUEUE_0	STOP TRANSMISSION OF FRAMES IN THE XID/UI_QUEUE_0.
	STOP_XID/UI_QUEUE_1	STOP TRANSMISSION OF FRAMES IN THE XID/UI_QUEUE_1.
TEST/ DIAGNOSTIC	DMA TEST	TEST DMA OPERATION.
	DUMP	DUMP ALL INTERNAL MLAPD REGISTERS AND CAM.

Figure 4. Command Set Summary

- Construct the necessary entry(s) in the LLID-LLT Table.
- Issue a RESET command to the MLAPD.
- Issue a SET_BUS_WIDTH_16,(8) command to the MLAPD, which specifies an 8- or 16-bit data bus configuration.
- Load the interrupt_vector register in the MLAPD device.
- Load the address of the Global Configuration Block into the data register in the MLAPD device.
- Issue the INIT command to the MLAPD.

The directly addressible MLAPD registers are shown in Figure 5.

A1	A2	15 — 8	7 — 0
0	0	UNDEFINED/RESERVED	COMMAND/SEMAPHORE
0	1	UNDEFINED/RESERVED	INTERRUPT_VECTOR
1	0	DATA	
1	1		

Figure 5. Directly Accessible Registers

Frame transmission and reception is enabled for a specific logical link after initialization by performing a Data Link Connection Identifier (DLCI) assignment procedure. (The DLCI is contained in the address field of LAPD frames. The DLCI is formed by the concatenation of the 6-bit service access point identifier, SAPI, and the 7-bit terminal endpoint identifier, TEI.) This logical link then enters a protocol-defined state in which it can receive and transmit unnumbered information frames. After the exchange of SABME and UA frames, the link set-up procedure is complete and the data connection is established. The MLAPD device is now ready to receive and transmit numbered information (I) frames that contain the assigned DLCI.

RECEIVE PROCESS

RECEIVE DATA STRUCTURES

The host maintains receive pools that contain free receive frame descriptors with associated data buffers. The host can create up to 8192 receive pools and can assign any number of logical links to the same receive pool. The data buffers in a pool must be of a length at least equal to the largest N201_value specified for any logical link assigned to the pool. The receive data structure is shown in Figure 6. The format of a receive frame descriptor is shown in Figure 7.

A receive pool must always contain at least one frame descriptor. The last frame descriptor in the pool is the pool_dummy frame descriptor and the last_in_pool bit in this frame descriptor's control_bits entry is set. When the receive_pool_pointer points to this pool_dummy frame descriptor, the receive pool is defined to be empty.

The host can add frame descriptors to a receive pool dynamically. The host maintains a user_Rx_pool tail_pointer for each receive pool, which points to the pool_dummy frame descriptor, for this operation. The host may also request a red_line interrupt when the MLAPD uses a frame descriptor near the end of the receive pool, allowing the host to add frame descriptors to avoid a receive busy condition.

After creating a receive pool, the host specifies a receive_pool_pointer, which is the address of the first frame descriptor in the receive pool, and issues an ASSIGN_POOL_POINTER command to cause the MLAPD to load the receive_pool_pointer into the Receive Pool Pointers Table. The MLAPD stores the first sixteen receive_pool_pointers (0 to 15) on-chip and stores any additional receive_pool_pointers (16 to 8191) in the Receive Pool Pointers Table in shared memory. The address of the memory table is specified by the host in the Global Configuration Block.

The host assigns each logical link to a receive pool via the receive_pool_number entry in the link's LLT. During frame reception, the MLAPD uses the receive_pool_number entry for the addressed link as an offset into the Receive Pool Pointers Table to locate the first receive frame descriptor in the assigned pool. Refer to Figure 8. When the frame is successfully received, the MLAPD indicates the frame type and stores the associated LLID in the receive frame descriptor. Then the MLAPD reads the next_rx_frame descriptor entry in this frame descriptor and updates the receive_pool_pointer for this pool in the Receive Pool Pointers Table. Although the linkage to the receive pool is not broken, the frame descriptor can now be considered part of a receive queue. All logical links that share the same receive pool will also share a common receive queue. It is the responsibility of higher level software to remove valid frames from the receive queue and eventually return the frame descriptors to the receive pool.

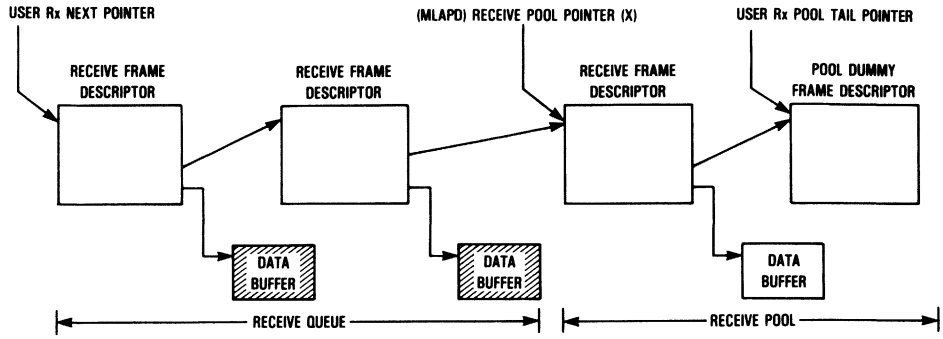


Figure 6. Receive Structures

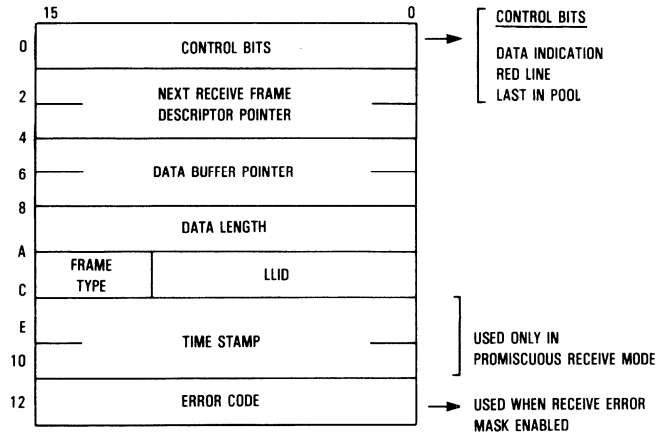


Figure 7. Receive Frame Descriptor

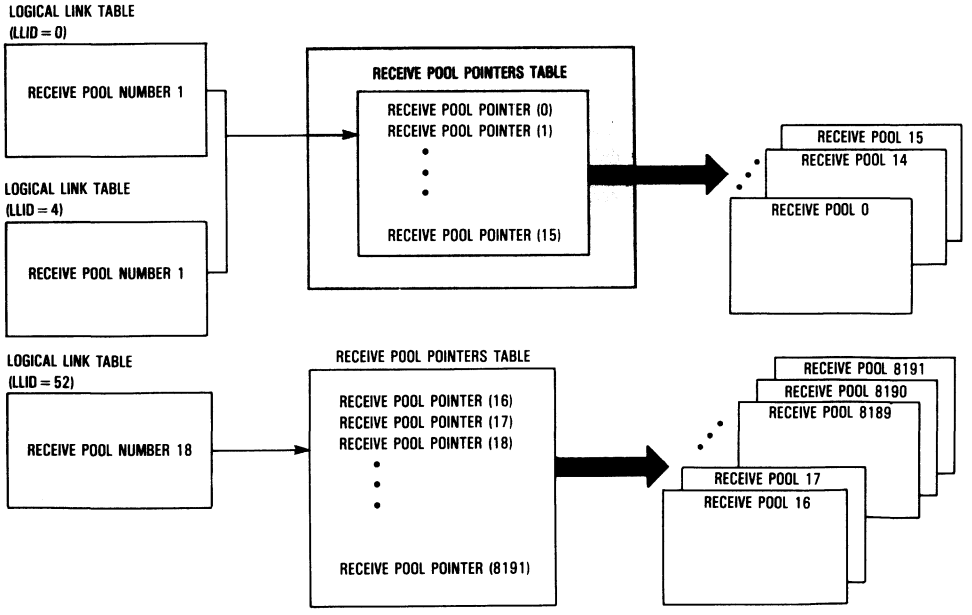


Figure 8. Receive Pool Lookup

Information Frame Reception

As the first step in the receive process, the MLAPD must determine whether the DLCI in an incoming frame has been assigned to an active logical link by Level 3. When the expanded system operation mode is selected by the host, the MLAPD uses the incoming DLCI as an offset into the external Match Table. If this entry is marked as invalid, then the incoming DLCI has not been assigned to a logical link and the frame is ignored. An error counter is also incremented. The receive process for expanded system operation mode is shown in Figure 9.

If the DLCI entry is marked as valid, then the entry also contains an associated logical link identification number (LLID). (Level 3 defines a 13-bit logical link identification number corresponding to each active DLCI. The LLID is used during link level processing and is only of local significance. The LLID serves to reduce the external memory requirements for LAPD processing.) The MLAPD uses the LLID as an offset into the LLID-LLT Table to locate this link's Logical Link Table (LLT). The MLAPD accesses the link's LLT to obtain the specific protocol parameters for this link which are required for subsequent protocol processing of the received frame. In the case

of an information bearing frame, the MLAPD uses the receive_pool_number entry in the LLT as an offset into the Receive Pool Pointers Table to locate the first available receive frame descriptor for this logical link. (The first 16 pool pointers are stored on-chip to reduce the number of memory accesses for the receive operation.) If the receive pool associated with this logical link is empty or the link's local_busy flag is set, then a Level 2 frame (RNR) is queued for transmission and the data is ignored. Otherwise the MLAPD continues to process the I frame by comparing the N(S) to the logical link's state variable V(R), also contained in the LLT. If the frame is in sequence, then the information field is transferred through the receive FIFO into the receive buffer. An out-of-sequence frame causes a Level 2 frame (REJ) to be queued for transmission and the out-of-sequence frame's information field is discarded. A frame received with an invalid N(R) causes a Level 2 frame (FRMR) to be queued for transmission (when the Tx_FRMR_select option is enabled) and the information field of the frame with an invalid N(R) is discarded.

Lastly the MLAPD checks the CRC of the incoming frame. If no CRC error is detected, the MLAPD updates the LLT state variable V(R) and acknowledges the frame reception by queuing a RR or RNR frame for transmission.

Zero deletion is performed throughout the reception process. The MLAPD requests the system bus when there are at least four words in the receive FIFO. Frames are received in sequence as long as memory buffers are available and adequate bandwidth is provided for DMA on the system bus.

When the application is limited to supporting 16 logical links or less, the host selects on-chip system operation mode. In the on-chip operation mode, the DLCI match operation is performed by an internal CAM circuit, reducing external memory requirements. Figure 10 shows how the MLAPD uses the received DLCI field to search the CAM as part of the receive process.

3

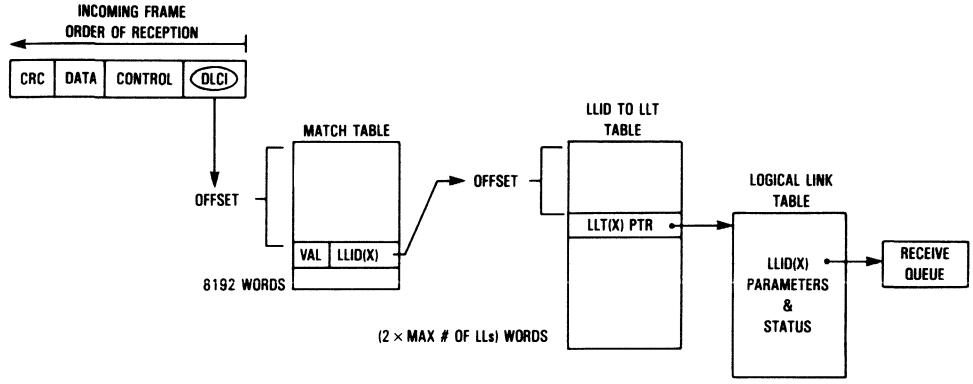


Figure 9. Receive Process for Expanded Mode

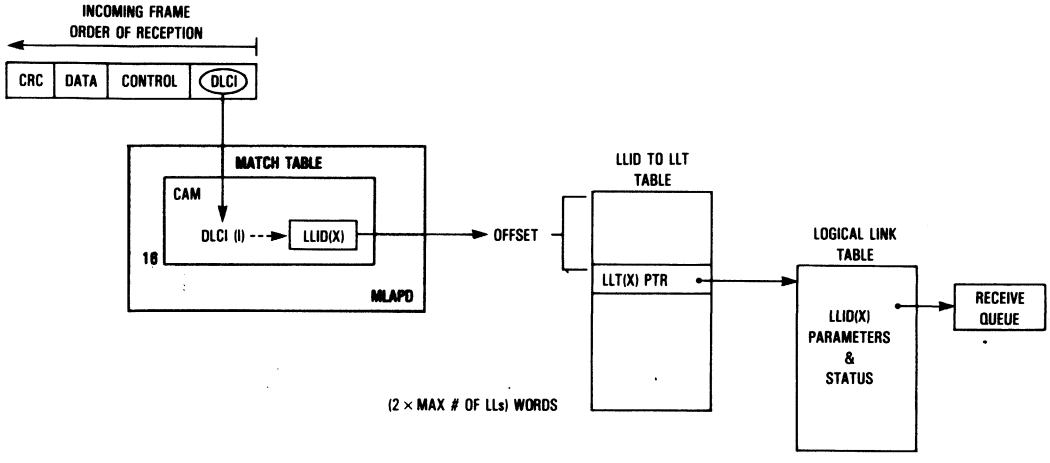


Figure 10. Receive Process for On-Chip Mode

XID/UI Frame Reception

The MLAPD handles reception of exchange identification (XID) frames, unnumbered information (UI) frames, and frames containing a user-defined non-standard control field in a similar manner as I frame reception. Received XID, UI, and non-standard_control frames are placed in the logical link's receive queue. To differentiate between types of received frames in the receive queue, the MLAPD encodes the frame_type bits in each receive frame descriptor.

Collecting Received Frames

The user must maintain a user_Rx_next_pointer for each queue that points to the first receive frame to be collected by the host. The host collects received frames by traversing the linked list of frame descriptors until a frame descriptor is reached with frame_type bits indicating that this frame descriptor still belongs to the receive pool and has not been used for frame reception. The host may set the data_indication bit in this frame descriptor to request an interrupt on the removal of this frame descriptor from the receive pool. After collecting receive frames, the host should update the user_Rx_next_pointer.

FRAME TRANSMISSION OVERVIEW

TRANSMIT SERVICING SCHEME

The MLAPD services several transmit queues. The frames in any single queue can be categorized as: Level 2 generated frames, XID/UI frames (including non-standard_control frames), or numbered information (I) frames. A fixed internal servicing scheme determines when each transmit queue is handled.

The highest priority transmit queue is the Level 2 Transmit Queue. The Level 2 Queue contains unnumbered (U) and supervisory (S) frames generated by the MLAPD in response to received frames and host commands. These frames are referred to as "Level 2 frames".

The next lower priority transmit queue contains XID and UI frames for transmission on the logical link specified in the frame descriptor. It is recommended that system implementations use this Global XID/UI Queue for frames generated by the Level 3 management entity.

The lowest priority transmit queues contain either I frames or XID/UI frames. The MLAPD supports up to four transmit I frame queues (I frame Queues_0-3) and up to two XID/UI queues (XID/UI Queues_0,1). The user defines the relative servicing for these six queues by the MLAPD transmit task by programming a scan length for each queue. The scan length defines the maximum number of frames to be transmitted from the queue before switching to service the next queue. When a scan length of zero is programmed, the corresponding queue is never serviced. In this way the user can implement zero, one, two, three, or four queues for I frame transmission, and zero, one, or two queues for XID/UI frame transmission.

Before each frame from the lowest priority queues is transmitted, the MLAPD transmits all frames in the Level 2 Queue and all frames in the Global XID/UI Queue. The MLAPD services the lowest priority queues in round robin fashion. The MLAPD transmit servicing scheme is shown in flowchart form in Figure 11.

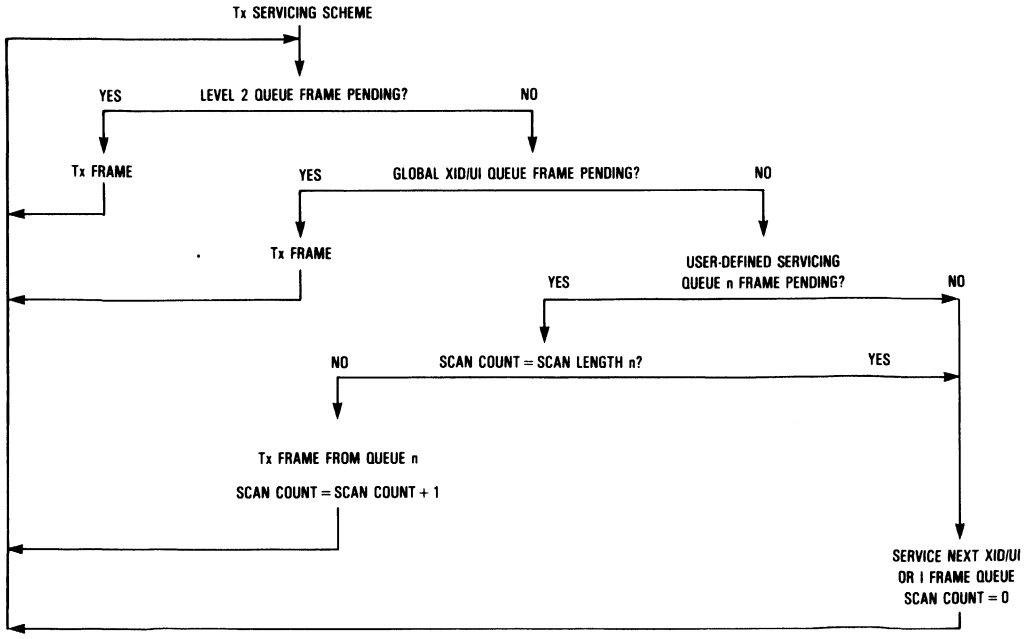


Figure 11. Transmit Servicing Scheme

I FRAME TRANSMISSION PROCESS

I Frame Queues and Logical Link Transmit Queues

Each I frame Queue is organized as a linked list, where the linkage mechanism is implemented by each queued link's Tx_next_LLT entry in its associated Logical Link Table (LLT). To minimize context switching, each link has its own transmit queue for I frames. The Tx_next_pointer entry in each LLT points to the first frame descriptor in the link's transmit queue. An I frame Queue is shown in Figure 12.

The host assigns each logical link to one of the four I frame Queues for all its numbered information frame transmissions. When the logical link's transmit queue is linked to its assigned I frame Queue, the pending I frames can be transmitted as part of the MLAPD transmit servicing scheme.

I Frame Transmission Queueing

When the host has data ready for transmission on a logical link, the host prepares one or more frame descriptors which contain information required by the MLAPD to transmit the associated frame(s). The format of a transmit I frame descriptor is shown in Figure 13. The host then links the frame descriptor(s) to the desired logical link's transmit queue. The transmit queue structure for numbered I frames is shown in Figure 14. If the logical link's transmit queue is empty when the new frame descriptor(s) is (are) linked to the queue, the host must issue a DL_DATA_REQUEST command for this link and specify the head of the transmit queue. This command causes the MLAPD to place this logical link into its assigned I frame Queue for transmit servicing. However, if frames are waiting for transmission in the link's transmit queue when the new frame descriptor(s) is (are) added, the linking of the descriptor(s) is sufficient for the associated frame(s) to be transmitted. If all the frames for this logical link were already transmitted but there are still some frames awaiting acknowledgement, the host must issue a RELINK_REQUEST command to enable transmission.

MLAPD I Frame Queue Processing

When an information frame is to be transmitted from an I frame Queue, the MLAPD first fetches the link's context from its associated Logical Link Table (LLT). This context information is used to build the address and control fields for the frame, which are then placed in the transmit FIFO. The Tx_next_pointer entry in the LLT identifies the address of the next I frame descriptor to be handled. The MLAPD uses information contained in this frame descriptor to locate the data to be sent, and then transfers this data into its transmit FIFO. As the MLAPD sends the frame, zeros are inserted when necessary for transparency and the MLAPD attaches a frame check sequence to complete the frame. After frame transmission, V(S) is updated and T200 is started if it is not already running. The MLAPD sets the transmit bit in the frame descriptor and updates the Tx_next_pointer entry.

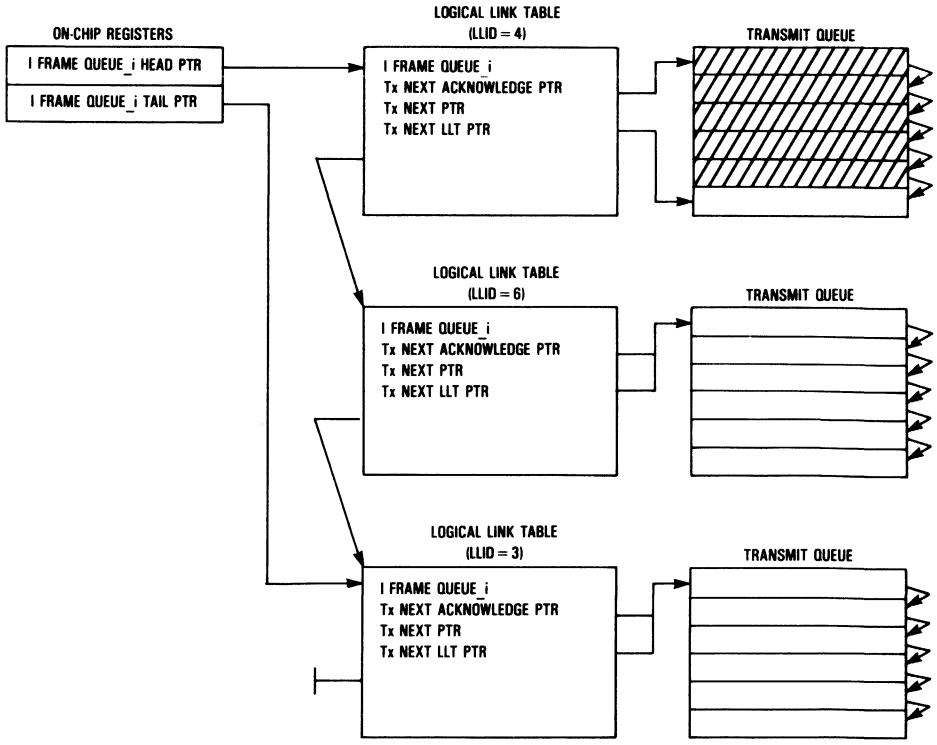
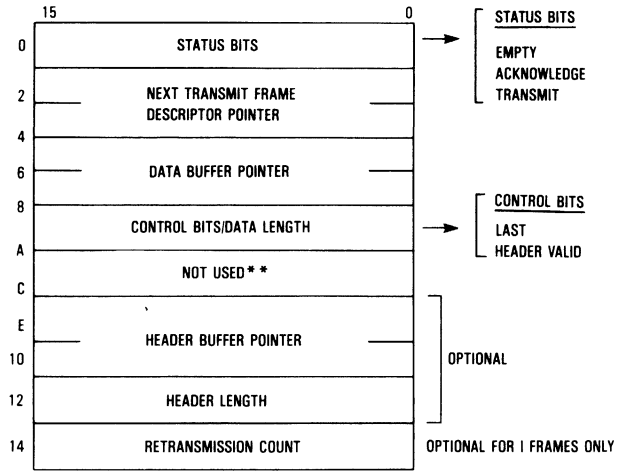


Figure 12. I Frame Queue Structure



**Contains frame type and LLID for XID/UI frames.
Contains CRC enable and address enable bits for non-protocol links.

Figure 13. Transmit Frame Descriptor

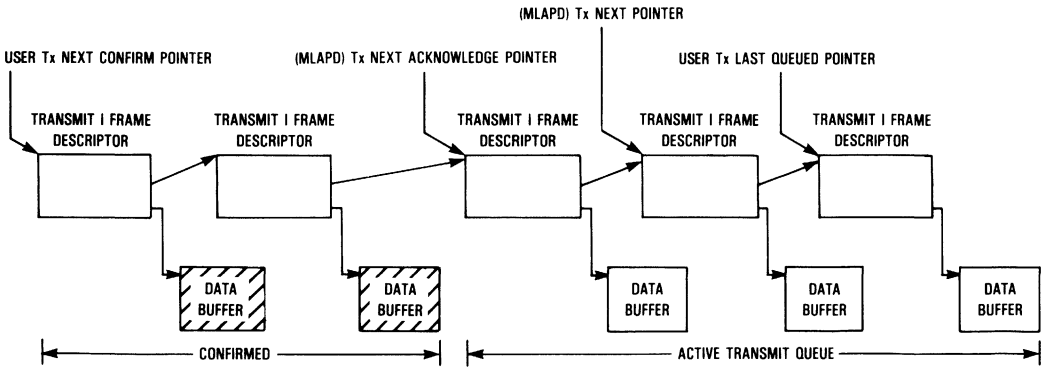


Figure 14. Logical Link Transmit Queue Structure

Transmission begins when ten bytes are present in the transmit FIFO, in addition to the address and control fields, or when the entire frame is present in the transmit FIFO. Between frames the MLAPD transmits the user selected number of pad flags. Additional flags may be transmitted, until the requirements for start of transmission are met. While transmitting a frame, the MLAPD requests the system bus when there are six to eight empty bytes in the transmit FIFO.

The MLAPD continues transmitting frames for the same logical link until one of the following events occur:

- The logical link's transmit queue is exhausted;
- The MLAPD transmitter switches to service another queue according to the transmit servicing scheme.

The MLAPD may also temporarily remove this link's transmit queue from its I frame Queue as the result of link conditions and host commands. The link conditions that cause removal are:

- Remote busy condition;
- Outstanding remote status request (command frame sent with poll bit set to one);
- Outstanding frames limit (K);
- Link reset;
- Timer recovery condition.

Stopping I Frame Transmission

At any time, the host may instruct the MLAPD to immediately suspend all transmit activity for a logical link's transmit queue by issuing a STOP_TX_I command. Upon receiving this command, the MLAPD aborts any current frame transmission for this link and removes the specified link from its assigned I frame Queue. The host is later notified when all outstanding acknowledgments have been received. At this point, the host is free to manipulate the transmit queue as desired, since the MLAPD is deactivated for that queue. This stop mechanism may be used to provide faster servicing of certain I frames or this mechanism may be necessary for various types of error recovery.

Collecting Acknowledged I Frames

To collect acknowledged frames, the host reads the status_bits in each frame descriptor, beginning with the frame descriptor indicated by the user_Tx_next_confirm_pointer. When the acknowledge bit is set, the associated data buffer has been transmitted and acknowledged. Acknowledged frames may be collected by the host dynamically (while other frames await acknowledgement) or after being notified by the MLAPD that all frames in the queue are acknowledged via a DL_data_confirmation interrupt. The host should update the user_Tx_next_confirm_pointer after each frame is collected.

XID/UI FRAME TRANSMISSION PROCESS

XID/UI Transmit Servicing

An XID/UI frame may be an unnumbered information (UI) frame, an exchange identification (XID) frame, or a frame with a user-defined non-standard_control field. In most ISDN applications it is anticipated that these frames will be used infrequently by Level 3 entities. However in some applications, such as bridges which interface to connectionless-oriented networks, UI frames may be used heavily for data transfer. To address the varying usage of XID, UI, and non-standard_control frames, the MLAPD provides two methods of servicing XID/UI queues. When frames are queued to the Global XID/UI Queue, the MLAPD will transmit all pending frames each time this queue is serviced. When frames are queued to either XID/UI Queue_0 or XID/UI Queue_1, the MLAPD will transmit only the number of frames specified by the corresponding user-defined scan length. It is recommended that the Global XID/UI Queue be reserved for management information exchange.

All XID/UI queues are linked lists of frame descriptors, where the frame descriptor specifies the logical link associated with the queued frame and the frame type. The structure of the XID/UI queues is shown in Figure 15.

XID/UI Frame Transmission Queueing

When XID/UI (or non-standard_control) information is ready for transmission on a logical link, the host prepares one or more frame descriptors which contain the information required by the MLAPD to transmit the frame(s). Then the host links the frame descriptor(s) to the appropriate XID/UI queue, depending on the servicing desired by the host for these frames. If the queue is empty when the new frame descriptor(s) is (are) linked, the host must issue the appropriate command (GLOBAL_XID/UI_REQUEST, XID/UI_QUEUE_0_REQUEST, or XID/UI_QUEUE_1_REQUEST) and specify the head of this queue. When this command is issued, the MLAPD places the corresponding XID/UI queue into the transmit servicing scheme. If frames are awaiting transmission when the new frame descriptor(s) is (are) added, the linking of the frame descriptor(s) is sufficient for the associated frame(s) to be transmitted.

MLAPD XID/UI Queue Processing

When an XID/UI or non-standard_control frame is to be transmitted, the MLAPD uses the LLID entry in the frame descriptor to index into the LLID-LLT Table to obtain the appropriate DLCI for the frame. The MLAPD places this DLCI and the correct control field into its transmit FIFO. Next, the address of the frame data is read from the frame descriptor and the MLAPD transfers this data into the transmit FIFO. As the frame is transmitted, zeros are inserted when necessary for transparency. CRC is calculated and appended to complete the frame.

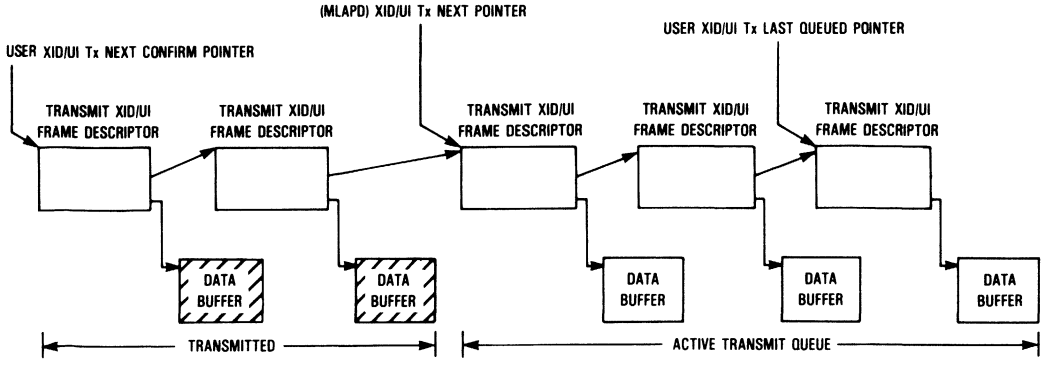


Figure 15. XID/UI Queue Structure

Stopping XID/UI Frame Transmission

At any time the host may instruct the MLAPD to immediately suspend all transmit activity for the Global XID/UI Queue, for XID/UI Queue_0 or for XID/UI Queue_1. This result is produced by the corresponding STOP_TRANSMIT command (STOP_GLOBAL_XID/UI, STOP_XID/UI_QUEUE_0, or STOP_XID/UI_QUEUE_1). Upon receiving one of these commands, the MLAPD aborts any current XID/UI (or non-standard_control) frame transmission and does not service additional XID/UI frame descriptors in the specified queue. At this point, the host is free to manipulate the queue as desired, since the MLAPD is deactivated for that queue. This stop mechanism may be used to provide faster servicing of certain XID, UI, or non-standard_control frames for a particular logical link, or this mechanism may be necessary for various types of error recovery.

Collecting Transmitted XID/UI Frames

The collection of transmitted XID/UI frames is the same for all three XID/UI Queues. To collect transmitted frames, the host reads the status_bits in each frame descriptor, beginning with the frame descriptor indicated by the user_XID/UI_Tx_next_confirm_pointer associated with the queue. When either the positive_confirmation bit or the negative_confirmation bit is set, the associated data buffer has been handled by the MLAPD.

The positive_confirmation bit indicates that the associated data buffer has been transmitted, while the negative_confirmation bit indicates that the associated data buffer cannot be transmitted. A negative indication is generated when a frame transmission is requested in conflict with the services available in the current link state (TEI_UNASSIGN or EST_WAIT_TEI). The host should later resubmit the DL_UI frame for transmission.

Transmitted frames may be collected by the host dynamically (while other frames await transmission) or after being notified by the MLAPD via an XID/UI_confirmation interrupt that all frames in the queue have been sent. After each frame is collected from an XID/UI queue, the host should update the associated user XID/UI_Tx_next_confirm_pointer.

MLAPD IMPLEMENTATION OF SPECIAL MODES

NON-PROTOCOL LINKS

The MLAPD can simultaneously support links which operate according to the LAPD protocol and links which do not operate according to the LAPD protocol. The host specifies that the link will operate in non-protocol mode by programming the non-protocol_select bit in the link's Logical Link Table. When supporting a non-protocol link, the MLAPD functions as a HDLC framer with DMA capability.

Queueing Frames for Transmission

To queue frames for transmission on a non-protocol link, the host first creates a transmit queue. The structure of the transmit queue is identical to a transmit queue which is used for I frames for LAPD links. To enable transmission of the transmit queue for a non-protocol link, the host issues a DL_DATA_REQUEST command which causes the MLAPD to place this logical link into its assigned I frame Queue for transmit servicing. If the host adds frames to a non-empty transmit queue, the linking of the frame descriptor(s) is sufficient for the associated frames to be transmitted. Note that for non-protocol links, the MLAPD does not recognize any incoming acknowledgements and the RELINK_REQUEST command is not meaningful.

MLAPD Frame Transmission

When a frame is to be transmitted for a non-protocol link, the MLAPD first fetches the link's context from its LLT. Then, based upon the transmit_address_enable bit in the frame descriptor, the MLAPD may or may not append the DLCI associated with this logical link to the beginning of the transmit frame. Next the MLAPD uses the information contained in the frame descriptor to locate the transmit memory buffer, and then transfers this information into its transmit FIFO. The MLAPD transmits the frame inserting zeros when necessary for transparency. After the transmit buffer is transmitted, the MLAPD may or may not append a CRC to the frame, based upon the transmit_CRC_enable bit in the frame descriptor.

Transmission begins when ten bytes are present in the transmit FIFO or when the entire frame is present in the transmit FIFO. Between frames the MLAPD transmits the user selected number of pad flags. Additional flags may be transmitted, until the requirements for start of transmission are met. While transmitting a frame, the MLAPD requests the system bus when there are six to eight empty bytes in the transmit FIFO.

Once the MLAPD begins handling a non-protocol link's transmit queue, the MLAPD will continue servicing the queue until all frames are transmitted or until the scan length associated with the I frame Queue is exhausted.

Stopping Frame Transmission

At any time, the host may instruct the MLAPD to immediately suspend all transmit activity on a non-protocol link by issuing a STOP_TX_I command. Upon receiving this command, the MLAPD aborts any current frame transmission for this link and does not service additional frame descriptors. At this point, the host is free to manipulate the transmit queue as desired, since the MLAPD is deactivated for this link. This stop mechanism may be used to provide faster servicing of certain frames for this link or this mechanism may be necessary for various types of error recovery.

Collecting Transmitted Frames

To collect transmitted frames, the host reads the status_bits in each frame descriptor, beginning with the frame descriptor indicated by the user_Tx_next_confirm_pointer. When the transmit bit is set, the associated data buffer has been transmitted. Transmitted frames may be collected by the host dynamically (while other frames await transmission) or after being notified by the MLAPD that all frames in the queue are transmitted via a DL_data_confirmation interrupt. The host should update the user_Tx_next_confirm_pointer after each frame is collected.

Receive Structures

The receive structures for a non-protocol link are identical to the structures for a LAPD link. A non-protocol link is assigned to a receive pool by the host using the receive_pool_number entry in the link's LLT. Any number of links may share a receive pool, although it is anticipated that most system

implementations will not assign LAPD links and non-protocol links to the same receive pool. Note that the N201_value specified for a non-protocol link defines the maximum length for a received frame.

MLAPD Frame Reception

As an incoming frame is received in on-chip system operation mode, the DLCI field in the frame is compared to the on-chip CAM to identify the corresponding logical link, if any. In expanded system operation mode, the MLAPD accesses the external Match Table to determine the associated logical link. If no DLCI match is found, then the incoming DLCI has not been assigned to a logical link, and the frame is ignored.

If a DLCI match is found, the corresponding entry in the Match Table or CAM specifies both the LLID and whether the link is assigned to LAPD protocol operation or non-protocol operation. If the frame is for a non-protocol link, the MLAPD proceeds to locate a free buffer to store the information between the opening and closing flags of the frame, minus the 16-bit address field. (The associated LLID is written into the frame descriptor.) The MLAPD locates the link's receive pool by using the link's receive_pool_number LLT entry to index into the Receive Pool Pointers Table. If the receive pool associated with this logical link is empty, then the frame is ignored and a local_busy interrupt is generated.

Otherwise the MLAPD begins to transfer the frame into the memory buffer. During frame reception, the MLAPD performs zero deletion, checks for receive errors, and calculates the CRC. The host may save erroneous frames for inspection based upon a non-protocol_error_mask. For non-protocol links, the host may also choose to have the MLAPD access multiple receive buffers as needed to store a received frame.

PROMISCUOUS RECEIVE MODE

Promiscuous receive mode is a special case of non-protocol link operation. This mode only affects the MLAPD receiver operation; the MLAPD transmitter operation is not affected. When promiscuous receive mode is selected, the MLAPD does not perform LAPD frame processing on the incoming serial bit stream. The MLAPD strips flags, performs zero deletion, and checks the frame CRC. No address matching or control field analysis is performed. The entire frame, as delineated by the HDLC flag characters, is stored in memory. The MLAPD uses the receive pool assigned by the host to the logical link associated with DLCI = 0.

The host may choose to accept erroneous frames based upon the non-protocol_error_mask. The host may also choose to have the MLAPD access multiple receive buffers as needed to store a received frame. As each receive buffer is filled, the MLAPD writes a time stamp into the associated frame descriptor. This time stamp indicates the "time", with respect to an internal 32-bit timer, when the MLAPD completed transferring the incoming frame to the receive buffer. When the MLAPD is in promiscuous receive mode, the host may enable a filtering option which allows the host to selectively receive frames from the serial link based upon the first 32 bits of each frame. This provides a built-in logic analyzer trigger-type diagnostic capability.

LINE MONITOR

This mode allows the user to monitor all the bits on the data link. When the $\overline{\text{RSTART}}$ pin is asserted, the receive operation begins. As long as $\overline{\text{RSTART}}$ remains asserted, the chip will pack all received bits to words and write them into receive buffers from a single receive pool. This mode may be very useful in analyzing line problems, bit errors, zero insertion errors and special bit patterns such as flags, abort, and idle sequences, that are not normally dumped into memory.

SYSTEM LOOPBACK TESTING

To allow the MLAPD to perform the LAPD procedures during a system loopback test, the MLAPD provides a "flip" option. When enabled, the MLAPD will invert the least significant bit of the DLCI field for each received frame. To implement this mode, the host activates pairs of logical links with DLCIs that differ only in the least significant bit position. For each pair, one link is assigned as network and the other link is assigned as user. Then when a frame is transmitted for one logical link, it is received for the other logical link. Thus enabling the MLAPD to implement the LAPD procedures while in loopback mode.

The system loopback can be internal or external. When internal loopback is selected, the host may also specify that any bits received on RxD should be echoed back to the network on TxD. Note that when the flip option is not enabled, the host may only operate non-protocol links under the internal or external loopback configuration.

MEMORY-TO-MEMORY OPERATION

The MLAPD can be configured for operation in systems which do not implement a non-channelized serial interface, such as channelized T1 networks or LANs. It is assumed that a device in the system, labeled "Device A" in Figure 16, directly interfaces to the physical level. Received frames are placed into memory and transmit frames are placed into Device A using either DMA or host I/O capabilities. In memory-to-memory operation, the MLAPD performs the LAPD procedures on these memory resident receive and transmit frames. This mode allows the system designer to select the MLAPD to implement the LAPD procedures independent of the physical level characteristics of the system.

To enable memory-to-memory operation, the host sets an option_bit in the Global Configuration Block. In this configuration, the MLAPD transmitter and receiver are internally connected. The RxD and TxD pins are not used. The MLAPD on-chip DMA controller feeds the receive and transmit machines via their associated FIFOs. The host activates a logical link with DLCI = 0 as a non-protocol link and assigns this link to I frame Queue_0. Note that I frame Queue_0 should be reserved for use only by this logical link associated with DLCI = 0.

As frames are received from the physical level, the host is responsible for placing these received frames into the memory format defined for a MLAPD transmit queue. Each transmit buffer contains an entire received frame. The host then issues a DL_DATA_REQUEST with the LLID associated with DLCI = 0 as command argument 1 and the address of the first transmit frame descriptor as command argument 2. In response, the MLAPD begins transmitting frames from I frame Queue_0 according to the transmit servicing scheme described in **Transmit Servicing Scheme**. Since the logical link associated with DLCI = 0 is assigned to non-protocol operation, the MLAPD acts as a simple HDLC framer. The MLAPD may optionally

add the frame CRC as described in **MLAPD Frame Transmission**. The frame address should be contained in the transmit data buffer (passed through from the physical level). When the frame is received via the internal loopback path, the MLAPD analyzes the address field, determines whether the addressed logical link is assigned to LAPD or non-protocol operation and then handles the frame as described in **Information Frame Reception, XID/UI Frame Reception,** and **MLAPD Frame Reception**. The MLAPD continues to transmit frames from I frame Queue_0 until the scan length specified for I frame Queue_0 is exhausted or until all queued frames are transmitted. A DL_data_confirmation interrupt is issued to the host when all frames are transmitted. This interrupt indicates that all frames received from the physical level have been handled by the MLAPD. Level 3 collects the received I, XID, UI, and non-standard_control frames for the various logical links as described in **Collecting Received Frames**.

The memory-to-memory operation mode does not affect the procedure for passing transmit frames from Level 3 to the MLAPD for Level 2 handling. Level 3 queues I, XID, UI, and non-standard_control frames to the Global XID/UI Queue, I frame Queues_1-3, and XID/UI Queues_0,1. The MLAPD independently generates U and S frames and places them on the Level 2 Queue. The transmit servicing scheme for these transmit queues and the protocol actions provided by the MLAPD are unchanged. During the transmit process, the MLAPD appends the appropriate DLCI, control field and CRC to queued transmit frames for LAPD links, and the MLAPD may optionally append the DLCI and CRC for non-protocol links. As each transmitted frame is received via the internal loopback path, the MLAPD receiver handles the frame as for promiscuous receive mode. The entire frame is stored in memory. The MLAPD uses the receive pool assigned by the host to the logical link associated with DLCI = 0. It is the responsibility of the host to enable transmission of these frames by the physical level.

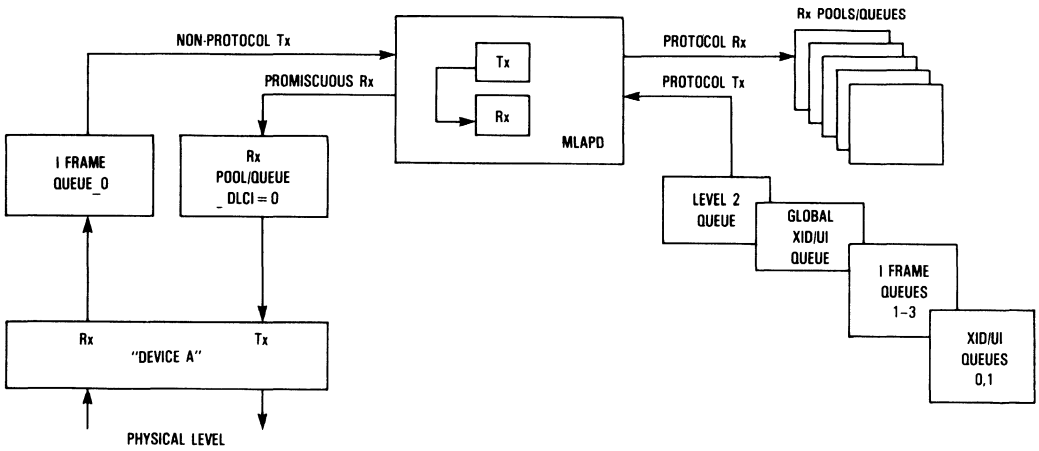


Figure 16. Memory-to-Memory Operation

MOTOROLA

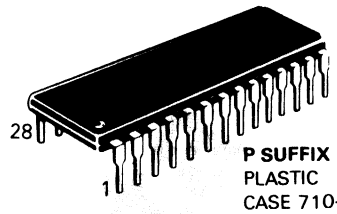
MC141500

Product Preview

VOICE MEMORY ADDRESS CONTROLLER
SILICON-GATE CMOS

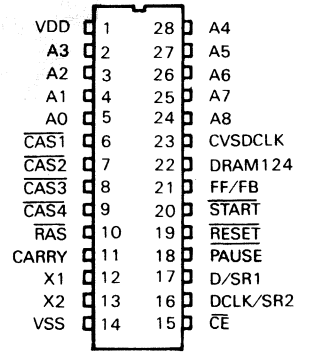
The MC141500 Voice Memory Address Controller (VMAC) is a CMOS IC specially designed for controlling the addressing of DRAMs used as the voice storage for the Motorola CVSD (Continuous Variable Slope Delta Modulation/Demodulation) IC, such as the MC34115, MC3417 and MC3418. Up to 256 pieces of 256K DRAMs can be controlled for a maximum recording time of 102 minutes.

- 5 volt supply.
- Supports 256K DRAM.
- Different memory configurations.
- Start, reset, pause, fast forward, fast backward controls.
- DRAM refreshing provided.
- 11K, 16K, 21K or 32K BPS sample rates available.
- Uses low cost 3.58 MHz crystal.
- Serial MCU interface.
- Start and stop addresses set by MCU.
- Current address can be read by MCU.



P SUFFIX
PLASTIC
CASE 710-02

PIN ASSIGNMENT



This document contains information on a new product specification and information herein is subject to change without notice.

3

MOTOROLA

MC142100
MC145100

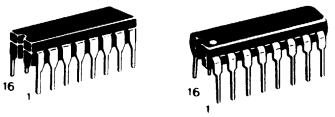
4 × 4 CROSSPOINT SWITCH WITH CONTROL MEMORY

The MC142100 and MC145100 consist of 16 crosspoint switches (analog transmission gates) organized in 4 rows and 4 columns. Both devices have 16 latches, each of which controls the state of a particular switch. Any of the 16 switches can be selected by applying its address to the device and a pulse to the strobe input. The selected crosspoint will turn on if during strobe, Data In was a one and will turn off if during strobe, Data In was a zero. In addition the MC145100 will reset all non-selected switches in the same row as the selected switch. Other switches are unaffected. In the MC145100, an internal power-on reset turns off all switches as power is applied.

- Internal Latches Control State of Switches
- Power-On Reset (MC145100 Only)
- Low On Resistance – Typically on 110 Ω @ 10 Vdc
- Large Analog Range ($V_{DD} - V_{SS}$)
- All Pins Are Diode Protected
- Matched Switch Characteristics
- High CMOS Noise Immunity
- MC142100 Pin-for-Pin Replacement for CD22100

CMOS MSI
(LOW-POWER COMPLEMENTARY MOS)

4 × 4 CROSSPOINT SWITCH WITH CONTROL MEMORY

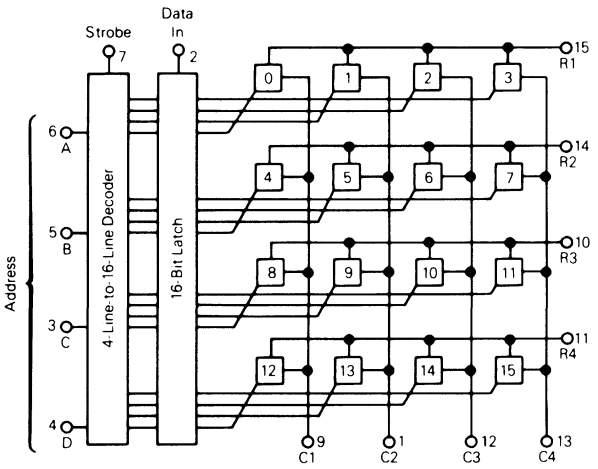


L SUFFIX
CERAMIC PACKAGE
CASE 620

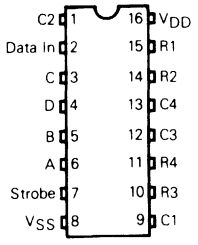
P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range



PIN ASSIGNMENTS



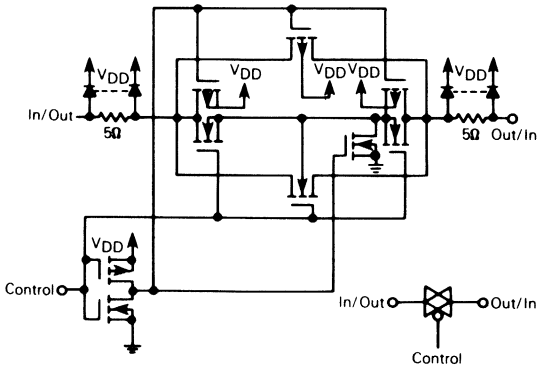
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

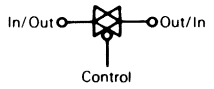
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} + 0.5	Vdc
Through Current	I	25	mAdc
Operating Temperature Range AL Device CL/CP Device	T_A	 −55 to +125 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.
Unused control inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

DS9804R1

ANALOG TRANSMISSION GATE
(CROSSPOINT) SCHEMATIC





ELECTRICAL CHARACTERISTICS (V_{SS} = 0 V)

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Operating Voltage MC145100	V_{DD}	–	4.25	18	4.25	–	18	4.25	18	Vdc
MC142100			3	18	3	–	18	3	18	
Input Voltage (Logic) "0" Level	V_{IL}									Vdc
Control Input		5	–	1.5	–	2.25	1.5	–	1.5	
		10	–	3.0	–	4.50	3.0	–	3.0	
		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
		5	3.5	–	3.5	2.75	–	3.5	–	
		10	7.0	–	7.0	5.50	–	7.0	–	
See Figure 1		15	11.0	–	11.0	8.25	–	11.0	–	
Input Current AL	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μA
Pins 2, 3, 4, 5, 6, 7 CL, CP	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	
Input Capacitance (V_{in} = 0)	C_{in}									pF
Digital Inputs		10	–	–	–	7	15	–	–	
Switch Inputs/Outputs		10	–	–	–	50	75	–	–	
Feedthrough Capacitance	$C_{in/out}$	–	–	–	–	0.4	–	–	–	pF
Quiescent Current (AL) MC145100	I_{DD}	5	–	200	–	55	110	–	70	μA
		10	–	400	–	115	230	–	100	
		15	–	600	–	170	340	–	200	
MC142100	I_{DD}	5	–	5	–	0.003	5	–	150	μA
		10	–	10	–	0.004	10	–	300	
		15	–	20	–	0.005	20	–	600	
Quiescent Current MC145100	IDD	5	–	250	–	55	150	–	80	μA
(CL, CP Device)		10	–	500	–	115	300	–	150	
		15	–	800	–	170	600	–	300	
MC142100	I_{DD}	5	–	5	–	0.003	5	–	150	μA
		10	–	10	–	0.004	10	–	300	
		15	–	20	–	0.005	20	–	600	
On-State See Figures 6-10	R_{on}	5	–	270	–	250	300	–	375	Ω
Resistance		10	–	140	–	110	170	–	230	
$V_{in} = \frac{V_{DD} - V_{SS}}{2}$		15	–	90	–	85	115	–	145	
On-State Resistance Difference	$\triangle R_{on}$	5	–	–	–	25	30	–	–	Ω
Between Any Two Switches		10	–	–	–	15	25	–	–	
$V_{in} = \frac{V_{DD} - V_{SS}}{2}$ See Figure 6		15	–	–	–	15	20	–	–	
Input/Output Leakage AL	$I_{in/out}$	15	–	±100	–	±0.4	+100	–	±1000	nA
Current, Switch Off CL, CP		15	–	±300	–	±0.4	±300	–	±1000	

* T_{low} = 55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, ±85°C for CL/CP Device.

SWITCHING CHARACTERISTICS (V_{SS} = 0, T_A = 25°C, C_L = 50 pF)

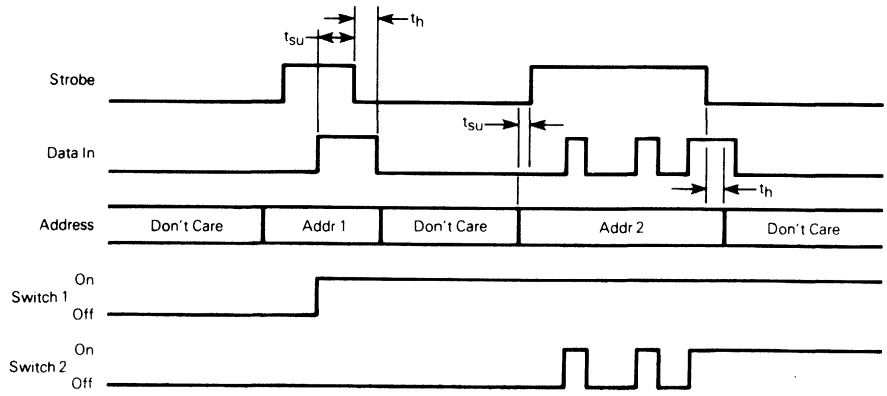
Characteristics		Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Propagation Delay Times	V_{SS} = 0 Vdc						
Input to Output		t_{PLH}, t_{PHL}	5	–	30	60	ns
			10	–	15	30	
			15	–	10	20	
Strobe to Output							
Output "1" to High Impedance	MC142100	t_{PLZ}, t_{PHZ}	5	–	350	700	ns
Output "0" to High Impedance			10	–	175	350	
			15	–	125	250	
Output "1" to High Impedance	MC145100	t_{PLZ}, t_{PHZ}	5	–	520	1040	ns
Output "0" to High Impedance			10	–	215	430	
			15	–	140	280	
High Impedance to Output "1"	MC142100	t_{PZH}, t_{PZL}	5	–	300	600	ns
High Impedance to Output "0"			10	–	150	250	
			15	–	80	160	
High Impedance to Output "1"	MC145100	t_{PZH}, t_{PZL}	5	–	550	1100	ns
High Impedance to Output "0"			10	–	200	400	
			15	–	130	260	
Data In to Output	MC142100	t_{PZH}, t_{PHZ}	5	–	300	600	ns
		t_{PZL}, t_{PLZ}	10	–	110	220	
			15	–	75	150	
Data In to Output	MC145100	t_{PZH}, t_{PHZ}	5	–	500	1000	ns
		t_{PZL}, t_{PLZ}	10	–	200	400	
			15	–	120	240	
Address to Output	MC142100	t_{PZH}, t_{PHZ}	5	–	350	700	ns
		t_{PZL}, t_{PLZ}	10	–	135	270	
			15	–	90	180	
Address to Output	MC145100	t_{PZL}, t_{PLZ}	5	–	500	1000	ns
		t_{PZH}, t_{PHZ}	10	–	180	360	
See Figure 2			15	–	115	230	
Minimum Setup Time							
Data In to Strobe	MC142100	t_{su}	5	–	50	190	ns
			10	–	10	50	
			15	–	0	30	
Data In to Strobe	MC145100	t_{su}	5	–	100	200	ns
			10	–	40	80	
			15	–	25	50	
Minimum Hold Time							
Data In to Strobe	MC142100	t_h	5	–	50	250	ns
			10	–	20	150	
			15	–	10	50	
Data In to Strobe	MC145100	t_h	5	–	40	400	ns
			10	–	10	200	
			15	–	0	80	
Minimum Set Up Time	MC142100	t_{su}	5	–	0	180	ns
Address to Strobe	MC145100		10	–	0	50	
			15	–	0	30	ns
Minimum Hold Time	MC142100	t_h	5	–	0	110	ns
Address to Strobe	MC145100		10	–	0	45	
			15	–	0	30	
Minimum Strobe Pulse Width	MC142100	t_{WH}	5	–	150	320	ns
	MC145100		10	–	50	160	
			15	–	40	80	

SWITCHING CHARACTERISTICS (continued) (V_{SS} = 0, T_A = 25°C, C_L = 50 pF)

Characteristics		Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Sine Wave Distortion (R_L = 1 kΩ, f = 1 kHz)	See Figure 3	–	10	–	0.5	–	%
Frequency Response (Switch On) (R_L = 1kΩ, 20 Log_{10} V_{out}/V_{in} = – 3.0 dB)	See Figure 3	–	10	–	15	–	MHz
Feedthrough Attenuation (Switch Off) (V_{in} = 10 Vpp, F = 1.6 kHz, R_L = 1 kΩ, C_L = 15 pF)	See Figure 3	–	10	–	– 80	–	dB
Frequency for Signal Crosstalk (V_{in} = 10 Vpp, Switch A	– 40 dB	–	10	–	1500	–	kHz
On, Switch B Off, R_L = 1 kΩ, C_L = 15 pF)	– 110 dB See Figure 4	–	–	–	0.1	–	kHz
Crosstalk Controls to Output (R_L = 10 kΩ)	See Figure 5	–	10	–	70	–	mV

Address				Switch Selected		MC145100 Only Switches Cleared			Address				Switch Selected		MC145100 Only Switches Cleared		
A	B	C	D						A	B	C	D					
0	0	0	0	C1R1	0	1	2	3	0	0	0	1	C1R3	8	9	10	11
1	0	0	0	C2R1	1	0	2	3	1	0	0	1	C2R3	9	8	10	11
0	1	0	0	C3R1	2	0	1	3	0	1	0	1	C3R3	10	8	9	11
1	1	0	0	C4R1	3	0	1	2	1	1	0	1	C4R3	11	8	9	10
0	0	1	0	C1R2	4	5	6	7	0	0	1	1	C1R4	12	13	14	15
1	0	1	0	C2R2	5	4	6	7	1	0	1	1	C2R4	13	12	14	15
0	1	1	0	C3R2	6	4	5	7	0	1	1	1	C3R4	14	12	13	15
1	1	1	0	C4R2	7	4	5	6	1	1	1	1	C4R4	15	12	13	14

TIMING DIAGRAM
MC145100/MC142100



TEST CIRCUITS

FIGURE 1 – INPUT VOLTAGE

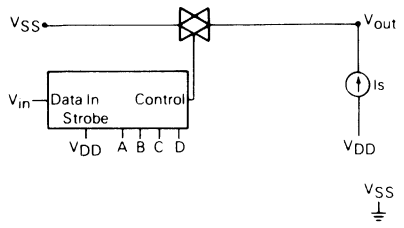


FIGURE 2 – PROPAGATION DELAY TIME

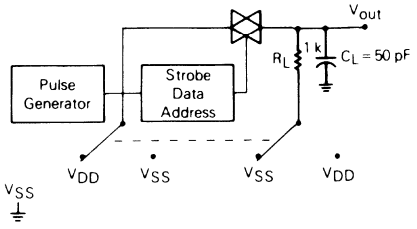


FIGURE 3 – BANDWIDTH AND FEEDTHROUGH ATTENUATION

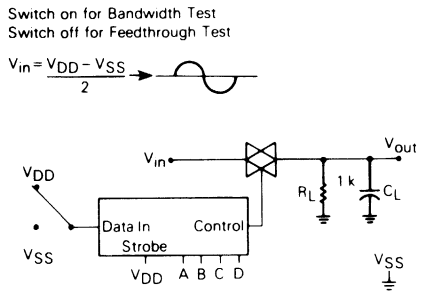


FIGURE 4 – CROSSTALK BETWEEN ANY TWO SWITCHES

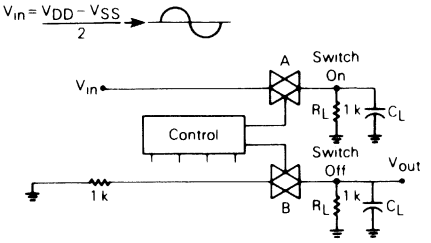


FIGURE 5 – CROSSTALK CONTROL TO OUTPUT

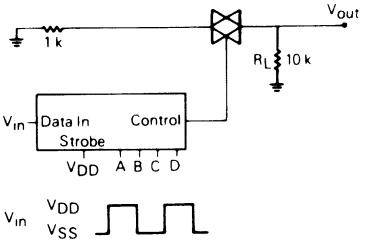
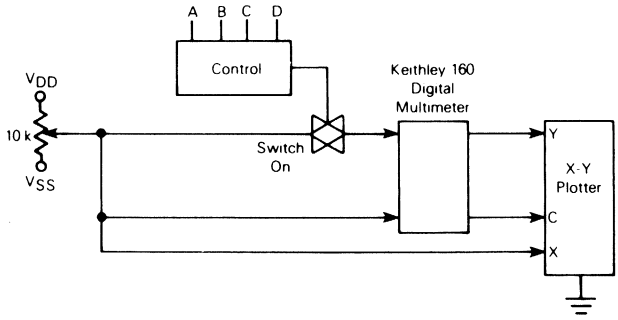


FIGURE 6 – CHANNEL RESISTANCE (R_{ON}) TEST CIRCUIT



TYPICAL RESISTANCE CHARACTERISTICS

FIGURE 7 – COMPARISON AT 25°C

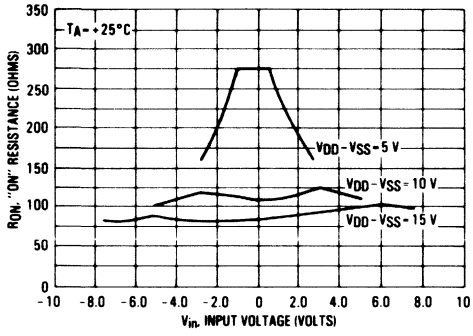


FIGURE 8 – V_{DD} = 2.5 V, V_{SS} = −2.5 V

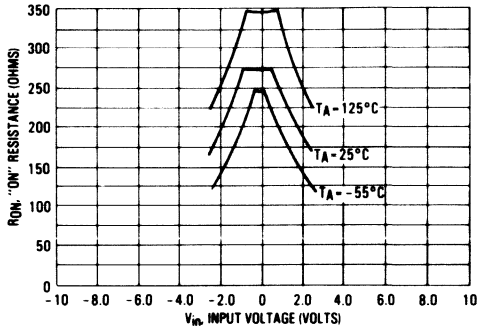


FIGURE 9 – V_{DD} = 5.0 V, V_{SS} = −5.0 V

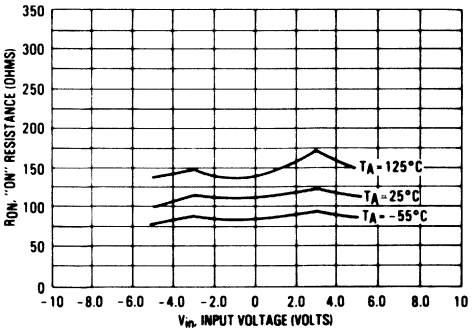
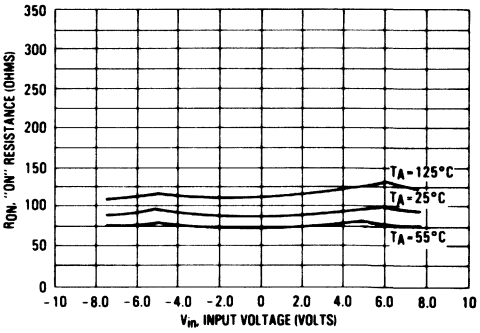


FIGURE 10 – V_{DD} = 7.5 V, V_{SS} = −7.5 V



MOTOROLA

MC143403
MC143404

Advance Information

CMOS MSI

QUAD LINE DRIVER

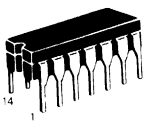
3

QUAD LINE DRIVER

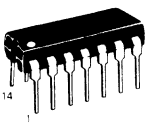
The MC143403 and MC143404 are low power, quad line drivers with true differential inputs. The device has electrical characteristics similar to the popular MC1741 and MC3403. However, the MC143403 has several distinct advantages over standard operational amplifier types. The low power quad driver, MC143403, draws only 1.5 mA (typ) and the micro power quad driver, MC143404, draws only 400 μA (typ) and provides high output drive capabilities. The common mode rejection ratio is typically 80 dB.

These units are excellent building blocks for communications, consumer, industrial and instrument applications where low power is required, particularly in telecommunications equipment. These units are useful in both battery operated communications systems and phone line powered equipment.

- Low Power and Micropower Communication Devices
- True Differential Input Stage
- Single or Split Supply Operation
- High Input Impedance
- Very Low Input Bias Current: 10 nA
- Four Drivers per Package
- Pinout Compatible with LM324 and MC3403
- Wide Input Voltage Range
- High Output Current Drive, MC143403



L SUFFIX
CERAMIC PACKAGE
CASE 632



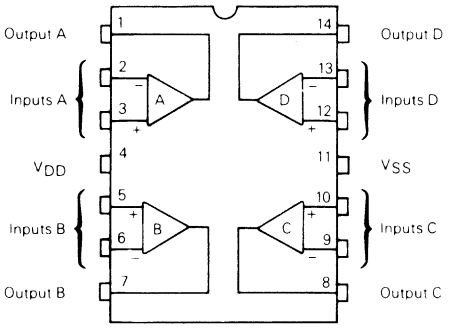
P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXX

Suffix	Denotes
L	Ceramic Package
P	Plastic Package

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ADI1027

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +15	V
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} + 0.5	V
DC Current Drain per Pin	I	10	mA
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	−65 to 150	°C

RECOMMENDED OPERATING CONDITIONS

DC Supply Voltage	V_{DD}	+4.75 to +12.6	V

3

ELECTRICAL CHARACTERISTICS (V_{SS} = 0 V, T_A = 0 to 70°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}	10	–	–	±30	mV
Input Offset Current	I_{IO}	10	–	–	200	pA
Open Loop Voltage Gain, R_L = 10 kΩ	A_{OL}	12 10 5	60 60 60	85 85 85	– – –	dB
Open Loop Voltage Gain, MC143403 Only, R_L = 600 Ω	A_{VOL}	10	45	55	–	
Common Mode Rejection Ratio	CMRR	10	60	80	–	dB
Input Bias Current	I_{IB}	10	–	–	1	nA
Output Voltage Range MC143404: R_L = 10 kΩ MC143403: R_L = 600 Ω	V_{OR}	12 10 5	1.5 1.0 1.0	– – –	10.5 8.5 4.0	V
Input Common Mode Voltage Range	V_{ICR}	12 10 5	0 0 0	– – –	10 8 3	V
Power Supply Current, MC143403	I_{DC}	12 5	– –	1.5 1.5	3.0 3.0	mA
Power Supply Current, MC143404	I_{DC}	12	–	0.4	0.8	

ELECTRICAL CHARACTERISTICS (V_{SS} = 0 V, T_A = 0 to 70°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Small Signal Bandwidth A_V = 1, R_L = 10 kΩ, V_O = 50 mV	BW	10	–	800	–	kHz
Slew Rate A_V = 1, R_L = 10 kΩ, 200 pF R_L = 600 Ω, 200 pF	SR	10	–	1 1.5	–	V/μs
Phase Margin MC143404: A_V = 1, R_L = 10 kΩ, 200 pF MC143403: R_L = 600 Ω, 200 pF	ϕ_m	10	–	75	–	deg
Power Supply Rejection Ratio	PSRR	10	–	60	–	dB
Average Temperature Coefficient of V_{IO}		10	–	20	–	μV/°C

FIGURE 1 – TYPICAL OPEN LOOP FREQUENCY RESPONSE

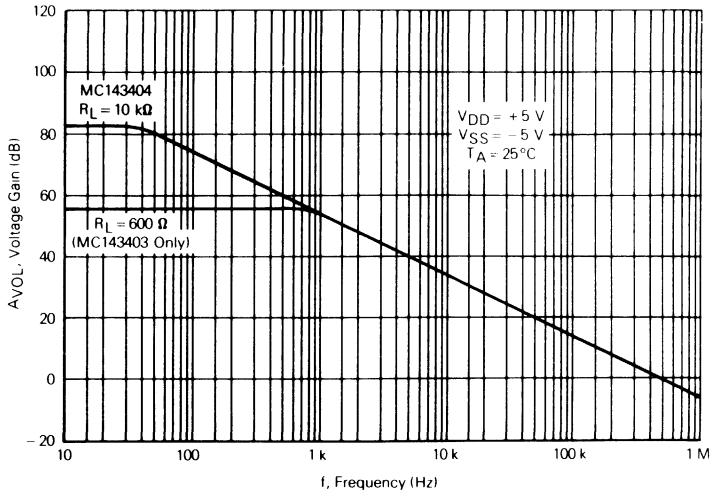


FIGURE 2 – TYPICAL POWER BANDWIDTH
(Large Signal Swing vs. Frequency)

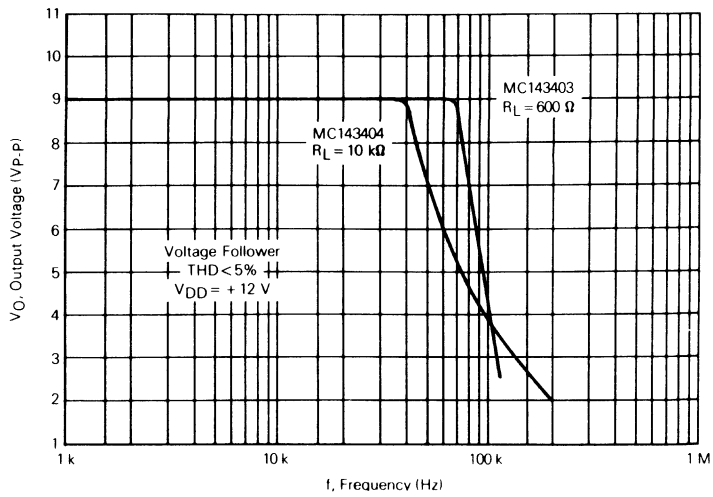


FIGURE 3 – GENERAL PURPOSE DUPLEXER (2 Wire to 4 Wire Converter)

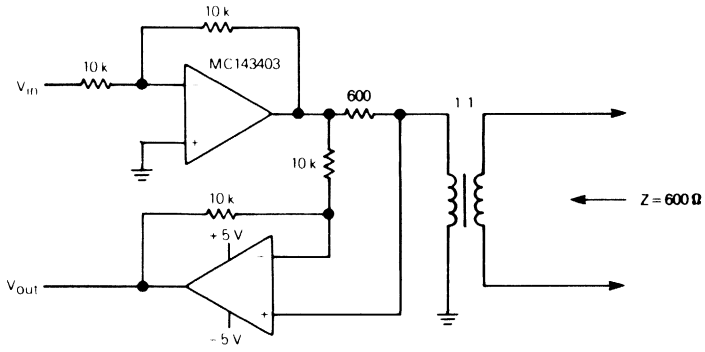
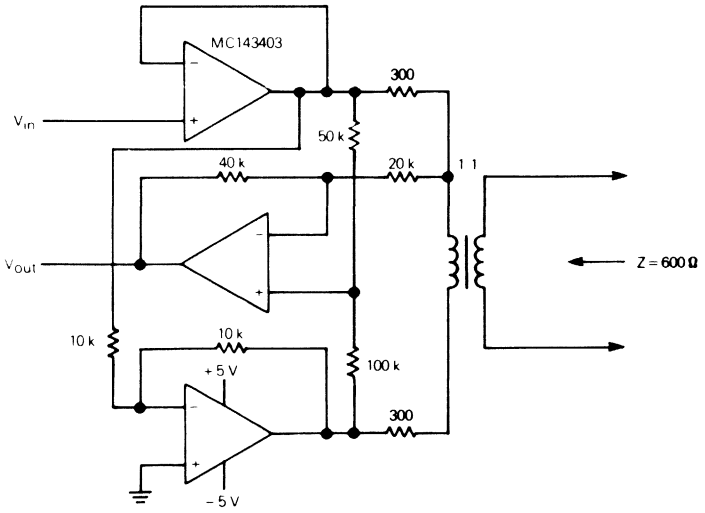


FIGURE 4 – HIGH POWER DUPLEXER (2 Wire to 4 Wire Converter)



MOTOROLA

MC145402

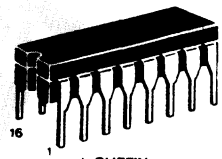
Product Preview

SERIAL 13-BIT LINEAR CODEC

- Provides both 13-Bit Monotonic A/D and D/A Conversion for Signal Processing Systems in a Single IC.
- 9-Bit Linearity.
- On-Chip Precison Voltage Reference
- Serial Data Ports.
- 2's Complement Coding.
- ±5 to 6 Volt Supply Operation.
- Input Sample and Hold Provided On-Chip.
- 5 Volt CMOS Inputs: Outputs capable of driving two LSTTL loads.
- Low Power Consumption: 50 mW typical, 3 mW Power Down.
- Sample Rates from 100 Hz to 20 kHz (both A/D and D/A). 26.67 kHz (A/D only) and 128 kHz (D/A only).

CMOS LSI
LOW-POWER COMPLEMENTARY MOS

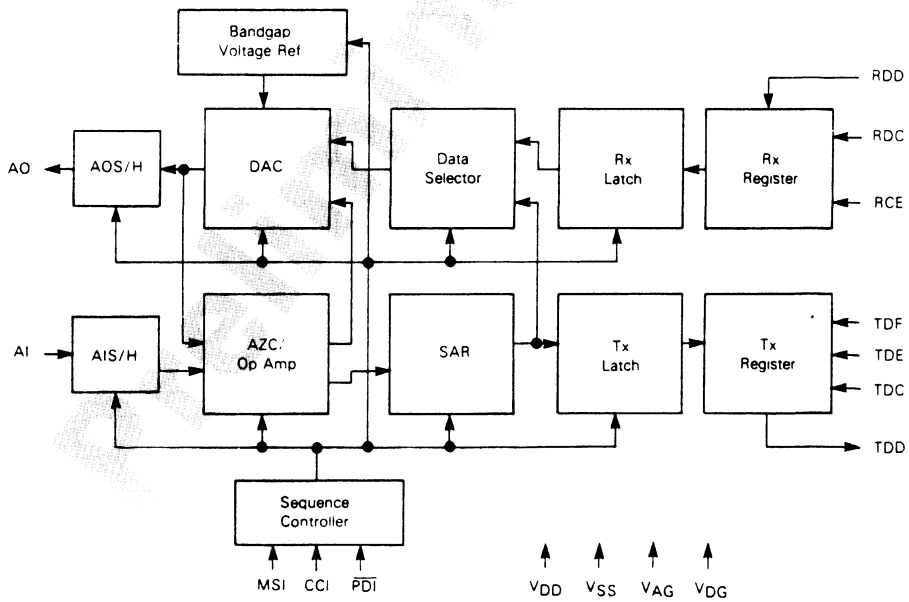
SERIAL 13-BIT LINEAR CODEC



L SUFFIX
CERAMIC PACKAGE
CASE 620

3

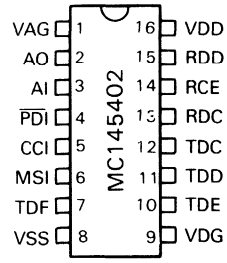
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Voltages References to V_{SS})

Rating	Symbol	Value	Unit
DC Supply voltage	$V_{DD} - V_{SS}$	-0.5 to 13.2	V
Voltage, Any Pin to V_{SS}	V	-0.5 to V_{DD} +0.5	V
DC Current Drain per Pin (Excluding V_{DD}, V_{SS})	I	10	mAdc
Operating Temperature Range	Ta	-40 to +85	°C
Storage Temperature Range	Tstg	-85 to +150	°C

PIN ASSIGNMENT



The device contains circuitry to protect the inputs against damage due to high static voltages or electrical fields. However, it is advised that normal precautions be taken to avoid applications of any voltage higher than the maximum rated voltages for this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} < (V_{in}$ or $V_{out}) < V_{DD}$. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}).

3

RECOMMENDED OPERATING CONDITIONS

Parameter	Pins	0 to 70°C Min	25°C Typ	0 to 70°C Max	Unit
DC Supply Voltage	V_{DD} to V_{SS}	9.5	10 to 12	13.2	V
Power Dissipation, $\overline{PDI}$ = "1"	V_{DD} to V_{SS}	-	50	80	mW
Power Dissipation, $\overline{PDI}$ = "0"	V_{DD} to V_{SS}	-	3	5	mW
Conversion Rate					
Full Cycle A/D & D/A	MSI	0.1	-	20	kHz
Short Cycle A/D	MSI	0.1	-	26.67	kHz
Short Cycle D/A	MSI	0.1	-	128	kHz
Conversion Sequence Rate	fcci	3.2	-	1024	kHz
Data Rate	TDC, RDC	ICCI	-	2560	kHz
Full Scale Analog Levels	AI, AO	-	3.27	-	V_{p}
(Referred to 600 Ω)		-	9.5	-	dBm

CODER AND DECODER PERFORMANCE

$V_{DD} - V_{SS}$ = 9.5 to 13.2 V, T_A = 0 to 70°C

	Coder (A/D)			Decoder (D/A)			
Parameter	Min	Typ	Max	Min	Typ	Max	Unit
Resolution	13	-	-	13	-	-	Bits
Conversion Time							
Full cycle A/D & D/A	50	-	10,000	50	-	10,000	μS
Short Cycle A/D	37.5	-	-	-	-	-	μS
Short Cycle D/A	-	-	-	7.8	-	-	μS
Differential Nonlinearity	-	-	±1	-	-	±1	LSB
Gain Error	-0.25	-	0.25	-0.25	-	0.25	dB
Offset	-	-	±10	-	-	±20	LSB
Signal to Noise Ratio							
9.5 to -10 dBm	-	54	-	-	54	-	dB
-30 dBm	-	34	-	-	34	-	dB
-50 dBm	-	14	-	-	14	-	dB

ANALOG ELECTRICAL CHARACTERISTICS

$V_{DD} - V_{SS}$ = 9.5 to 13.2 V, V_{AG} = ½ ($V_{DD} - V_{SS}$), T_A = 0 to 70°C, Z_L = 10 kΩ ‖ 50 pF

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Input Current	AI	I_{in}	-	-	±30	nA
AC Input Impedance	AI	Z_{in}	1.5	-	-	MΩ
Output Voltage Range, RL = 10 kΩ	AO	V_{or}	-3.4	-	3.4	V
Output Current	AO	I_{out}	0.35	-	-	mA
Power Supply Rejection Ratio	AO, T_{DD}	PSRR	-	30	-	dB
Crosstalk, AI to AO and R_{DD} to T_{DD}	AO, T_{DD}	-	-	-80	-	dB
Slew Rate	AO	SR	-	3	-	V/μS
Settling Time	AO	T_s	-	15	-	μS

3

DIGITAL ELECTRICAL CHARACTERISTICS

V_{DD} = 5 V, V_{SS} = -5 V, V_{AG} = V_{DG} = 0 V, T_A = 0 to 70°C

Characteristic		Symbol	Min	Max	Unit
High Level Input Voltage		V_{ih}	3.5	-	V
Low Level Input Voltage		V_{il}	-	1.5	V
Input Current		I_{in}	-	±1.0	μA
Input Capacitance		C_{in}	-	7.5	pF
High Level Output Voltage	I_{out} = -20 μA I_{out} = -1 mA	V_{oh}	4.9 4.3	- -	V
Low Level Output Voltage	I_{out} = 20μA I_{out} = 2 mA	V_{ol}	- -	0.1 0.4	V

SWITCHING CHARACTERISTICS

V_{DD} = 5 V, V_{SS} = -5 V, V_{AG} = V_{DG} = 0 V, T_A = 0 to 70°C, C_L = 50 pF, (See Figures 1 & 2)

Characteristic		Symbol	Min	Max	Unit
Input Rise Time		T_{ir}	-	100	nS
Input Fall Time		T_{if}	-	100	nS
Output Rise Time		T_{or}	-	80	nS
Output Fall Time		T_{of}	-	80	nS
Pulse Width High	MSI, CCI, TDC, RCE, RDC	T_{wh}	100	-	nS
Pulse Width Low	MSI, CCI, TDE, TDC, RCE, RDC	T_{wi}	100	-	nS
MSI Clock Frequency		fMSI	0.1	32	kHz
CCI Clock Frequency		fCCI	3.2	1024	kHz
TDC and RDC Clock Frequency		fDC	fCCI	2560	kHz

FIGURE 1 - MC145402 FULL & SHORT CYCLE TIMING

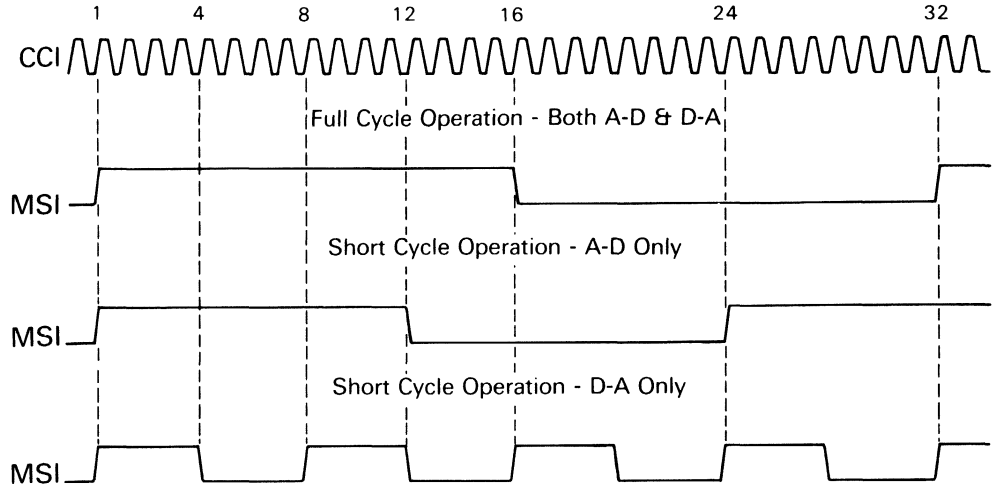
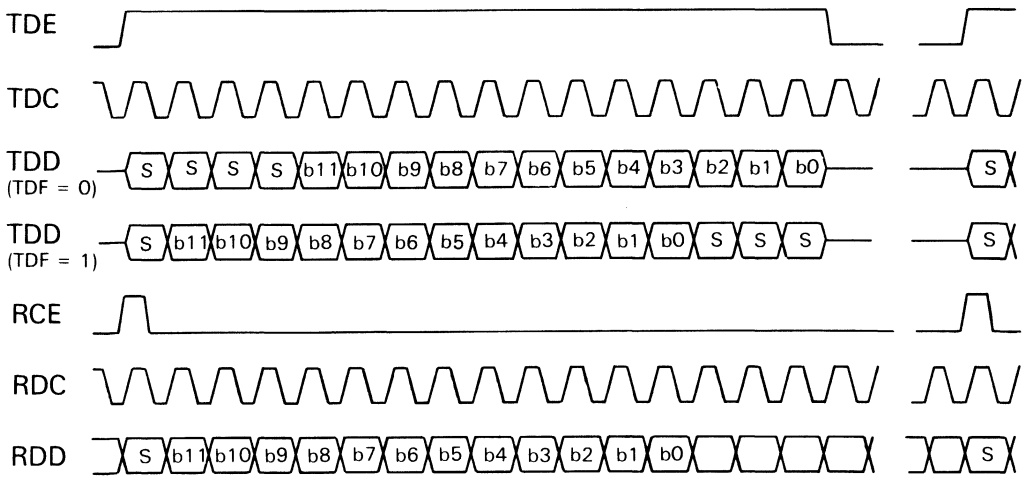


FIGURE 2 - MC145402 DIGITAL TIMING



PIN DESCRIPTION

V_{DD} - Positive Supply - The most positive power supply, typically +5 to +6 volts in split power supply configurations of +10 to +12 volts in single supply systems.

V_{SS} - Negative Supply - The most negative power supply, typically -5 to -6 volts in split power supply configurations or 0 volts in single supply systems.

V_{AG} - Analog Ground - The Analog signal reference point, this pin is normally tied to 0 volts in split supply operation.

V_{DG} - Digital Ground - This is the ground reference for all of the digital input and output pins. CMOS compatible logic signals swing from V_{DG} to V_{DD} where V_{DG} can be established anywhere from V_{DD} -4.75 volts to V_{SS}.

AO - Analog Output - This is the output of the decoder's sample and hold circuit and is a 100 percent duty cycle analog output of the last digital word received and decoded by the decoder. The analog output is updated shortly after the nearest rising edge of CCI to the rising edge of MSI and is capable of driving a 10 kohm, 50 pF load.

AI - Analog Input - This is the high impedance input to the coder and is sampled shortly after the nearest rising edge of CCI to the rising edge of MSI.

$\overline{PDI}$ - Power Down Input - In normal operation this input should be tied high. A logic low on this input puts the device into a minimum power dissipation mode. Transitions on this pin should be synchronised with the rising edge of MSI. See Figure 3 below. During power-down, all functions stop. One complete MSI conversion cycle is required to establish normal operation after leaving the power down mode.

CCI - Convert Clock Input - This input controls the complete conversion sequence during one MSI cycle and must receive a clock which is 32 times the frequency of MSI. The only exception to 32 times the frequency of MSI is during short-cycle operation. See "Modes of Operation". CCI must be synchronous and rising edge aligned with MSI.

MSI - Master Sync Input - This pin determines the conversion rate for both the coder and the decoder. One A/D and D/A conversion takes place during each period of the digital clock applied to this input (except in short-cycle operation, see "Modes of Operation"). MSI must be synchronous and rising edge aligned with CCI.

TDF - Transmit Data Format - The 13-bit digital output of the coder is available in one of two sixteen-bit two's complement formats as determined by the state of this pin. A logic zero at this pin causes the data from TDD to be in a 16-bit sign-extended format as follows: SSSSM . . . L where S, M, and L represent the sign, most significant magnitude bit, and the least significant magnitude bit, respectively. A logic one on this pin formats the data as follows: SM . . . LSSS.

TDE - Transmit Data Enable - This pin is used to initiate the serial transfer of data from the coder once during each MSI period and, in addition, provides three-state control of the TDD pin. A rising clock edge on TDE signals the start of data transfer from the TDD pin. A resulting high logic level on TDE also releases TDD from Its high-impedance state. TDE must remain high throughout the data transfer to keep TDD in the low-impedance state and must return to a low state prior to each data transfer. New data becomes available on the rising edge of MSI. Data transfers may not be in progress during this transition without loss of data.

TDD - Transmit Digital Data - This is the three-state output data pin from the coder and is controlled by the TDE and TDC pins. TDD is in the high-impedance state whenever TDE is a logic low. The first data bit is output from TDD on the rising edge of TDE (or TDC if it follows TDE) and each subsequent bit is output on rising edges of TDC. Two output data formats are available as described in the TDF pin description above.

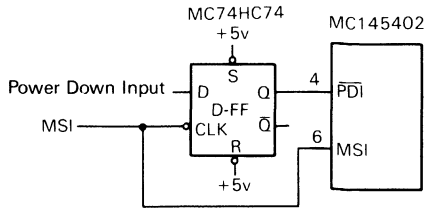
TDC - Transmit Data Clock - Digital data from the coder is serially transmitted from TDD on rising TDC edges whenever TDE is a logic high. TDC must be approximately rising edge aligned with TDE. Generally, if TDC is low when TDE rises, the first rising edge of TDC clocks the first data bit. If TDC is high when TDE rises, the first bit will be clocked by TDE and the first rising edge of TDC after TDE rises will clock out the second data bit.

RDC - Receive Data Clock - Receive digital data is accepted by the decoder on the first thirteen falling edges of RDC after an RCE rising edge.

RCE - Receive Clock Enable - This pin identifies the beginning of a data transfer into the RDD pin of the decoder. The first thirteen falling edges of RDC after an RCE rising edge will clock data into the decoder data input, RDD. RCE must return low prior to each data transfer. Data transfers may not span the rising edge of MSI without loss of data.

RDD - Receive Digital Data - This pin is the data input to the decoder and is controlled by the RDC and RDE pins described above. Two's complement data are loaded in the following sequence: SM . . .L where S, M, and L represent the sign, most significant magnitude bit, and the least significant magnitude bit, respectively. Only the first thirteen bits clocked by RDC after RCE rises will be accepted for decoding. Any additional bits will be ignored.

FIGURE 3 - PDI SYNC CIRCUIT



MODES OF OPERATION

GENERAL

The MC145402 has three modes of operation, a "full" cycle mode and two "short" cycle modes. The full cycle mode allows simultaneous Analog to Digital (A/D) and Digital to Analog (D/A) operation. The short cycle modes allow either A/D only or D/A only operation.

FULL CYCLE OPERATION

When operating in the full cycle mode, the MC145402 performs a 13-bit A/D conversion followed by a 13-bit D/A conversion. Full cycle operation is selected by using a CCI frequency that is 32 times the frequency of MSI. MSI is the sample rate frequency.

SHORT CYCLE ANALOG TO DIGITAL OPERATION

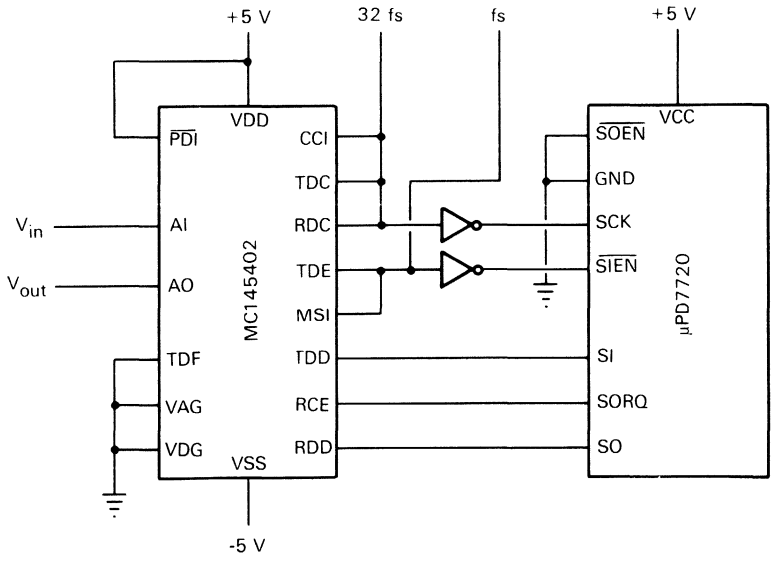
If CCI is 24 times the frequency of MSI, short cycle Analog to Digital operation is selected. This allows a 13-bit A/D conversion only. In this mode, the D/A is not operational.

SHORT CYCLE DIGITAL TO ANALOG OPERATION

Short cycle Digital to Analog operation is selected by using a CCI clock frequency that is 8 times the MSI sample rate. During short cycle D/A operation, A/D operation is disabled and digital data read from TDD is not valid.

3

FIGURE 4 - THE MC145402, 13-BIT LINEAR CODEC, INTERFACED TO A NEC μPD7720 SIGNAL PROCESSOR'S SERIAL PORT



MOTOROLA

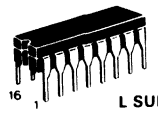
EIA-232-D/V.28 Driver/Receiver
(Formerly RS-232-C)

The MC145406 is a silicon-gate CMOS IC that combines 3 drivers and 3 receivers to fulfill the electrical specifications of standards EIA-232-D and CCITT V.28. The drivers feature true TTL input compatibility, slew-rate-limited output, 300 ohms power-off source impedance, and output typically switching to within 25 percent of the supply rails. The receivers can handle up to ±25 volts while presenting 3 to 7 kilohms impedance. Hysteresis in the receivers aids reception of noisy signals. By combining both drivers and receivers in a single CMOS chip, the MC145406 provides efficient, low-power solutions for EIA-232-D and V.28 applications.

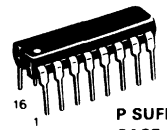
3

Drivers
- ±5 to ±12 V Supply Range
- 300 Ohms Power-Off Source Impedance
- Output Current Limiting
- TTL Compatible
- Maximum Slew Rate = 30 V/μs

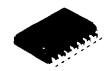
Receivers
- ±25 V Input Voltage Range When V_{DD} = 12 V, V_{SS} = −12 V
- 3 to 7 Kilohms Input Impedance
- Hysteresis on Input Switchpoint



L SUFFIX
CASE 620
CERAMIC

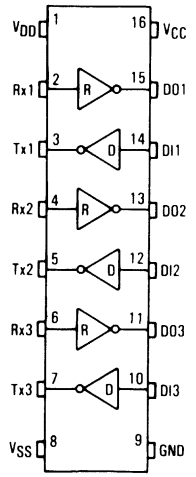


P SUFFIX
CASE 648
PLASTIC



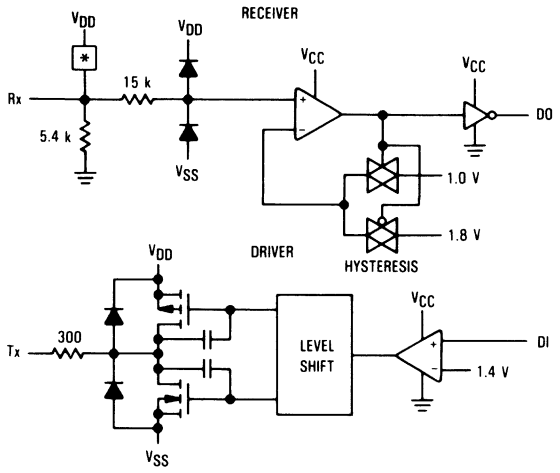
DW SUFFIX
CASE 751G
SOIC

PIN ASSIGNMENT



D = DRIVER
R = RECEIVER

FUNCTION DIAGRAM



*Protection circuit

MAXIMUM RATINGS (Voltage polarities referenced to GND)

Rating	Symbol	Value	Unit
DC Supply Voltages ($V_{DD} \geq V_{CC}$)	V_{DD} V_{SS} V_{CC}	−0.5 to +13.5 +0.5 to −13.5 −0.5 to 6.0	V
Input Voltage Range Rx1-3 Inputs DI1-3 Inputs	V_{IR}	 (V_{SS} − 15) to (V_{DD} + 15) −0.5 to (V_{CC} + 0.5)	V
DC Current Per Pin		± 100	mA
Power Dissipation	P_D	1.0	W
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−85 to +150	°C

This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, it is recommended that the voltages at the DI and DO pins be constrained to the range $GND \leq V_{DI} \leq V_{DD}$ and $GND \leq V_{DO} \leq V_{CC}$. Also, the voltage at the Rx pin should be constrained to $(V_{SS} - 15\ V) \leq V_{Rx1\text{-}3} \leq (V_{DD} + 15\ V)$, and Tx should be constrained to $V_{SS} \leq V_{Tx1\text{-}3} \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., GND or V_{CC} for DI, and V_{SS} or V_{DD} for Rx.)

DC ELECTRICAL CHARACTERISTICS (All polarities referenced to GND = 0 V, T_A = −40 to 85°C)

Parameter	Symbol	MC145406			Unit
		Min	Typ	Max	
DC Supply Voltage					V
V_{DD}	V_{DD}	4.5	5 to 12	13.2	
V_{SS}	V_{SS}	−4.5	−5 to −12	−13.2	
V_{CC} ($V_{DD} \geq V_{CC}$)	V_{CC}	4.5	5.0	5.5	
Quiescent Supply Current					μA
(Outputs unloaded, inputs low)					
V_{DD} = +12 V	I_{DD}	−	140	400	
V_{SS} = −12 V	I_{SS}	−	340	600	
V_{CC} = +5 V	I_{CC}	−	300	450	

RECEIVER ELECTRICAL SPECIFICATIONS (Voltage polarities referenced to GND = 0 V, V_{DD} = +5 to +12 V, V_{SS} = −5 to −12 V, $V_{DD} \geq V_{CC}$, T_A = −40 to 85°C)

Characteristic		Symbol	MC145406			Unit
			Min	Typ	Max	
Input Turn-on Threshold $V_{DO1\text{-}3} = V_{OL}$, V_{CC} = 5.0 V ±5%	Rx1-3	V_{on}	1.35	1.80	2.35	V
Input Turn-off Threshold $V_{DO1\text{-}3} = V_{OH}$, V_{CC} = 5.0 V ±5%	Rx1-3	V_{off}	0.75	1.00	1.25	V
Input Threshold Hysteresis V_{CC} = 5.0 V ±5%	Rx1-3	V_{on}-V_{off}	0.6	0.8	−	V
Input Resistance (V_{SS} − 15 V) ≤ $V_{Rx1\text{-}3}$ ≤ (V_{DD} + 15 V)	Rx1-3	R_{in}	3.0	5.4	7.0	kΩ
High-Level Output Voltage $V_{Rx1\text{-}3}$ = −3 V to (V_{SS} − 15 V)*	DO1-3	V_{OH}				V
I_{OH} = −20 μA, V_{CC} = +5.0 V			4.9	4.9	−	
I_{OH} = −1 mA, V_{CC} = +5.0 V			3.8	4.3	−	
Low-Level Output Voltage $V_{Rx1\text{-}3}$ = +3 V to (V_{DD} + 15 V)*	DO1-3	V_{OL}				V
I_{OL} = +20 μA, V_{CC} = +5.0 V			−	0.01	0.1	
I_{OL} = +2 mA, V_{CC} = +5.0 V			−	0.02	0.5	
I_{OL} = +4 mA, V_{CC} = +5.0 V			−	0.5	0.7	

*This is the range of input voltages as specified by EIA-232-D to cause a receiver to be in the high or low logic state.

DRIVER ELECTRICAL SPECIFICATIONS (Voltage polarities referenced to GND = 0 V, V_{CC} = +5 V ±5%, T_A = −40 to 85°C)

Characteristic		Symbol	MC145406			Unit
			Min	Typ	Max	
Digital Input Voltage	DI1-3					V
Logic 0		V_{IL}	—	—	0.8	
Logic 1		V_{IH}	2.0	—	—	
Input Current	DI1-3	I_{in}	—	—	±1.0	μA
$V_{DI1-3} = V_{CC}$						
Output High Voltage	Tx1-3	V_{OH}				V
V_{DI1-3} = Logic 0, R_L = 3.0 kΩ						
V_{DD} = +5.0 V, V_{SS} = −5.0 V			3.5	3.9	—	
V_{DD} = +6.0 V, V_{SS} = −6.0 V			4.3	4.7	—	
V_{DD} = +12.0 V, V_{SS} = −12.0 V			9.2	9.5	—	
Output Low Voltage*	Tx1-3	V_{OL}				V
V_{DI1-3} = Logic 1, R_L = 3.0 kΩ						
V_{DD} = +5.0 V, V_{SS} = −5.0 V			−4.0	−4.3	—	
V_{DD} = +6.0 V, V_{SS} = −6.0 V			−4.5	−5.2	—	
V_{DD} = +12.0 V, V_{SS} = −12.0 V			−10.0	−10.3	—	
Off Source Resistance	Tx1-3		300	—	—	Ω
(Figure 1)						
$V_{DD} = V_{SS} = GND = 0$ V, V_{Tx1-3} = ±2.0 V						
Output Short-Circuit Current	Tx1-3	I_{SC}				mA
V_{DD} = +12.0 V, V_{SS} = −12.0 V						
Tx1-3 shorted to GND**			—	±22	±60	
Tx1-3 shorted to ±15.0 V***			—	±60	±100	

*The voltage specifications are in terms of absolute values.

**Specification is for one Tx output pin to be shorted at a time. Should all three driver outputs be shorted simultaneously, device power dissipation limits will be exceeded.

***This condition could exceed package limitations.

SWITCHING CHARACTERISTICS (V_{CC} = +5 V ±5%, T_A = −40 to 85°C; See Figures 2 and 3)

Characteristic		Symbol	MC145406			Unit
			Min	Typ	Max	
Drivers						
Propagation Delay Time	Tx1-3					ns
Low-to-High		t_{PLH}				
R_L = 3 kΩ, C_L = 50 pF			—	300	500	
High-to-Low		t_{PHL}				
R_L = 3 kΩ, C_L = 50 pF			—	300	500	
Output Slew Rate	Tx1-3	SR				V/μs
Minimum Load						
R_L = 7 kΩ, C_L = 0 pF, V_{DD} = 6 to 12 V, V_{SS} = −6 to −12 V			—	±6	±30	
Maximum Load						
R_L = 3 kΩ, C_L = 2500 pF						
V_{DD} = 12 V, V_{SS} = −12 V			—	±3.0	—	
V_{DD} = 5 V, V_{SS} = −5 V			—	—	—	
Receivers (C_L = 50 pF)						
Propagation Delay Time	DO1-3					ns
Low-to-High		t_{PLH}	—	150	425	
High-to-Low		t_{PHL}	—	150	425	
Output Rise Time	DO1-3	t_r	—	250	400	ns
Output Fall Time	DO1-3	t_f	—	40	100	ns

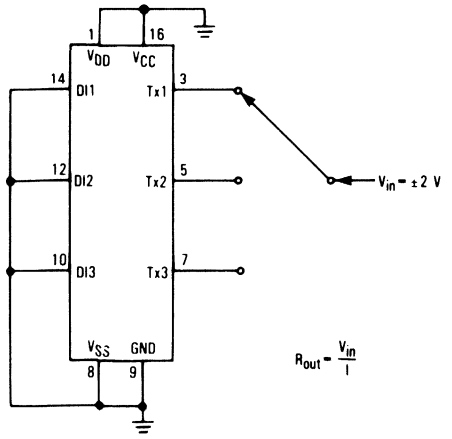


Figure 1. Power-Off Source Resistance (Drivers)

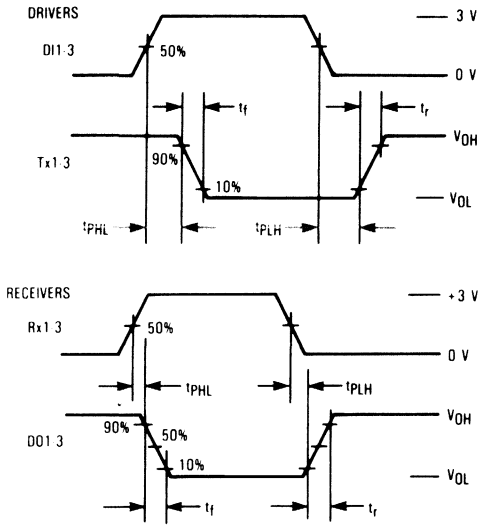


Figure 2. Switching Characteristics

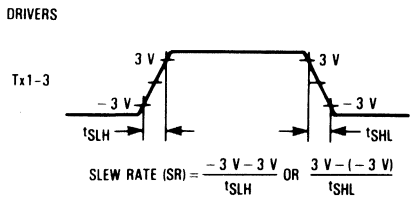


Figure 3. Slew Rate Characterization

PIN DESCRIPTIONS

V_{DD} – POSITIVE POWER SUPPLY (PIN 1)

The most positive power supply pin, which is typically 5 to 12 volts.

V_{SS} – NEGATIVE POWER SUPPLY (PIN 8)

The most negative power supply pin, which is typically −5 to −12 volts.

V_{CC} – DIGITAL POWER SUPPLY (PIN 16)

The digital supply pin, which is connected to the logic power supply (maximum +5.5 volts). V_{CC} *must* be less than or equal to V_{DD}.

GND – GROUND (PIN 9)

Ground return pin is typically connected to the signal ground pin of the EIA-232-D connector (connector pin 7) as well as to the logic power supply ground.

Rx1, Rx2, Rx3 – RECEIVE DATA INPUT (PINS 2, 4, 6)

These are the EIA-232-D receive signal inputs whose voltages can range from (V_{DD} + 15 V) to (V_{SS} − 15 V). A voltage between +3 and (V_{DD} + 15 V) is decoded as a space and causes the corresponding DO pin to swing to ground (0 V); a voltage between −3 and (V_{SS} − 15 V) is decoded as a mark and causes the DO pin to swing up to V_{CC}. The actual turn-on input switchpoint is typically biased at 1.8 volts above ground, and includes 800 millivolts of hysteresis for noise rejection. The nominal input impedance is 5 kilohms. An open or grounded input pin is interpreted as a mark, forcing the DO pin to V_{CC}.

DO1, DO2, DO3 – DATA OUTPUT (PINS 11, 13, 15)

These are the receiver digital output pins, which swing from V_{CC} to ground. A space on the Rx pin causes DO to produce a logic zero; a mark produces a logic one. Each output pin is capable of driving one LSTTL input load.

DI1, DI2, DI3 – DATA INPUT (PINS 10, 12, 14)

These are the high-impedance digital input pins to the drivers. TTL compatibility is accomplished by biasing the input switchpoint at 1.4 volts above ground. However, 5-volt CMOS compatibility is maintained as well. Input voltage levels on these pins must be between V_{CC} and ground.

Tx1, Tx2, Tx3 – TRANSMIT DATA OUTPUT (PINS 3, 5, 7)

These are the EIA-232-D transmit signal output pins, which swing toward V_{DD} and V_{SS}. A logic one at a DI input causes the corrresponding Tx output to swing toward V_{SS}. A logic zero causes the output to swing toward V_{DD} (the output voltages will be slightly less than V_{DD} or V_{SS} depending upon the output load). Output slew rates are limited to a maximum of 30 volts per microsecond. When the MC145406 is off ($V_{DD} = V_{SS} = V_{CC} = GND$), the minimum output impedance is 300 ohms.

APPLICATIONS INFORMATION

The MC145406 has been designed to meet the electrical specifications of standards EIA-232-D and CCITT V.28. EIA-232-D defines the electrical and physical interface between Data Communication Equipment (DCE) and Data Terminal Equipment (DTE). A DCE is connected to a DTE using a cable that typically carries up to 25 leads. These leads, referred to as interchange circuits, allow the transfer of timing, data, control, and test signals. Electrically this transfer requires level shifting between the TTL/CMOS logic levels of the computer or modem and the high voltage levels of EIA-232-D, which can range from ±3 to ±25 volts. The MC145406, provides the necessary level shifting as well as meeting other aspects of the EIA-232-D specification.

3

DRIVERS

As defined by the specification, an EIA-232-D driver presents a voltage of between ±5 to ±15 volts into a load of between 3 to 7 kilohms. A logic one at the driver input results in a voltage of between −5 to −15 volts. A logic zero results in a voltage between +5 to +15 volts. When operating V_{DD} and V_{SS} at ±7 to ±12 volts, the MC145406 meets this requirement. When operating at ±5 volts, the MC145406 drivers produce less than ±5 volts at the output (when terminated), which does not meet EIA-232-D specification. However, the output voltages when using a ±5 volt power supply are high enough (around ±4 volts) to permit proper reception by an EIA-232-D receiver, and can be used in applications where strict compliance to EIA-232-D is not required.

Another requirement of the MC145406 drivers is that they withstand a short to another driver in the EIA-232-D cable. The worst-case condition that is permitted by EIA-232-D is a ±15 volt source that is current limited to 500 milliamperes. The MC145406 drivers can withstand this condition momentarily. In most short circuit conditions the source driver will have a series 300 ohm output impedance needed to satisfy the EIA-232-D driver requirements. This will reduce the short circuit current to under 40 mA which is an acceptable level for the MC145406 to withstand.

Unlike some other drivers, the MC145406 drivers feature an internally-limited output slew rate that does not exceed 30 volts per microsecond.

RECEIVERS

The job of an EIA-232-D receiver is to level-shift voltages in the range of −25 to +25 volts down to TTL/CMOS logic levels (0 to +5 volts). A voltage of between −3 and −25 volts on Rx1 is defined as a mark and produces a logic one at DO1. A voltage between +3 and +25 volts is a space and produces a logic zero. While receiving these signals, the Rx inputs must present a resistance between 3 and 7 kilohms. Nominally, the input resistance of the Rx1-3 inputs is 5.4 kilohms.

The input threshold of the Rx1-3 inputs is typically biased at 1.8 volts above ground (GND) with typically 800 millivolts of hysteresis included to improve noise immunity. The 1.8 volt bias forces the appropriate DO pin to a logic one when its Rx input is open or grounded as called for in the EIA-232-D specification. Notice that TTL logic levels can be applied to the Rx inputs in lieu of normal EIA-232-D signal levels. This might be helpful in situations where access to the modem or computer through the EIA-232-D connector is necessary with TTL devices. However, it is important not to connect the EIA-232-D outputs (Tx1-3) to TTL inputs since TTL operates off +5 volts only, and may be damaged by the high output voltage of the MC145406.

The DO outputs are to be connected to a TTL or CMOS input (such as an input to a modem chip). These outputs will swing from V_{CC} to ground, allowing the designer to operate the DO and DI pins from digital power supply. The Tx and Rx sections are independently powered by V_{DD} and V_{SS} so that one may run logic at +5 volts and the EIA-232-D signals at ±12 volts.

POWER SUPPLY CONSIDERATIONS

V_{CC} should not exceed V_{DD} by more than 0.5 volts. Due to an internal diode between V_{DD} and V_{CC}, the power-up or power-down power supply sequences may permit V_{CC} to be greater than V_{DD} for a short period of time. This condition could cause parts to fail for longer periods of time. A diode as shown in Figure 4 can be used to protect the device from this condition.

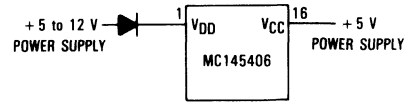
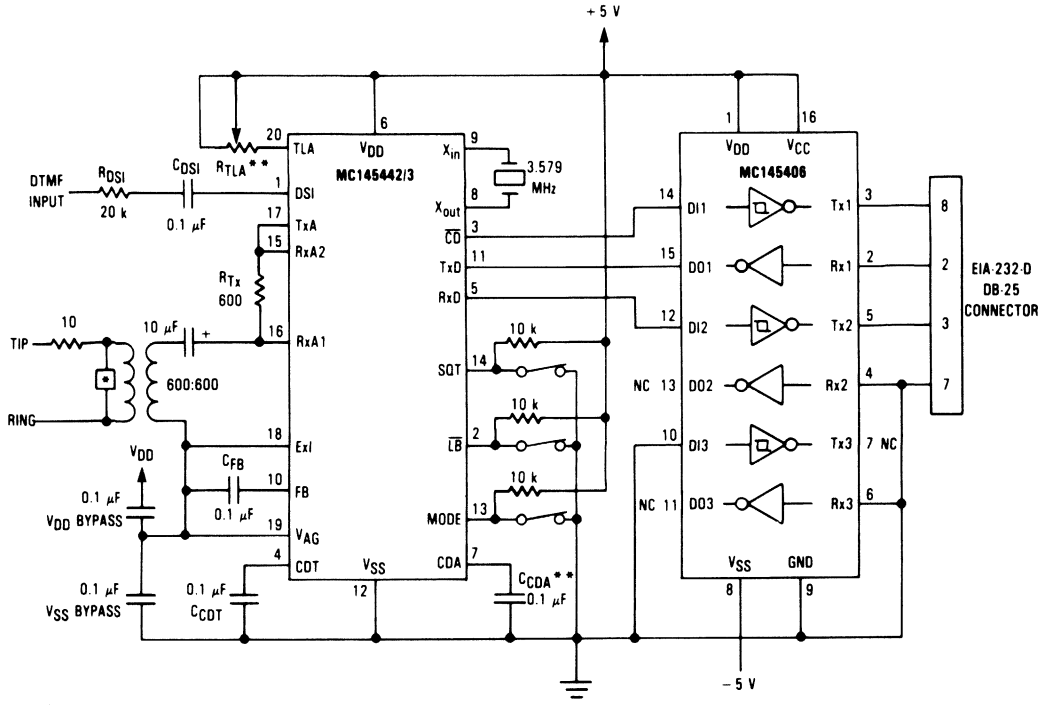


Figure 4. Protection Diode for $V_{CC} > V_{DD}$ Condition



*Line protection circuit
**Refer to the applications information for values of C_{CDA} and R_{TLA}

Figure 5. 5-Volt 300-Baud Modem with EIA-232-D Interface

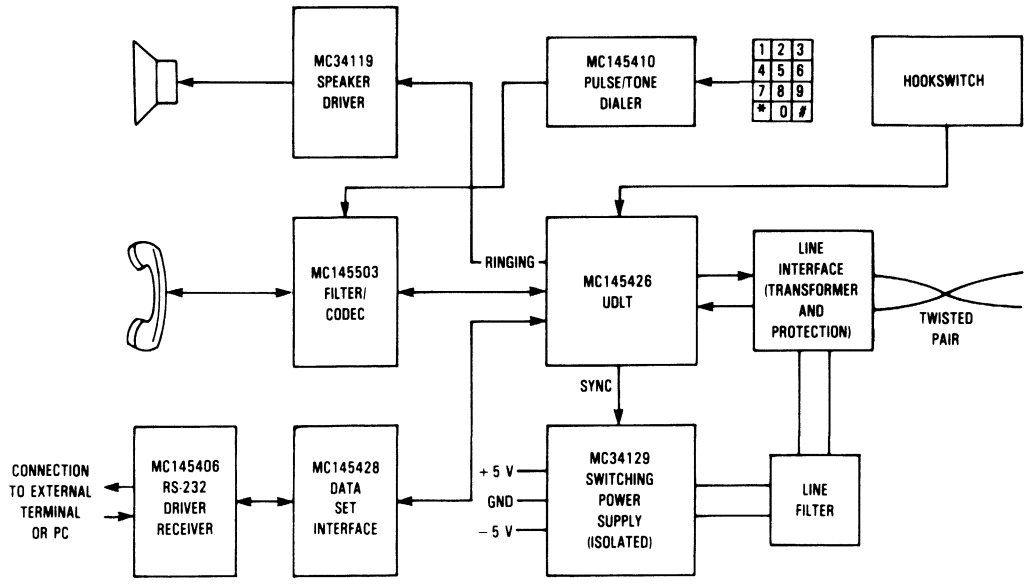


Figure 6. Line-Powered Voice/Data Telephone with Electrically Isolated EIA-232-D Interface

3

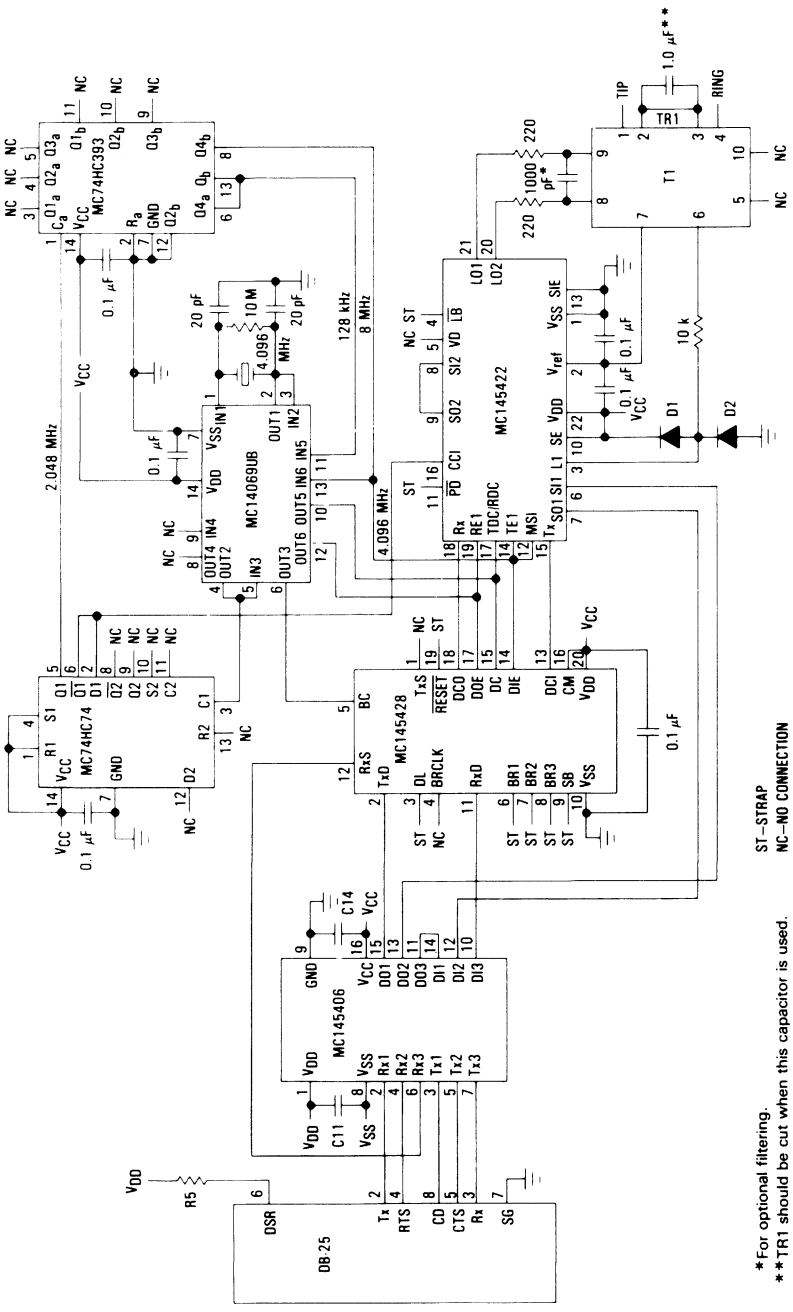


Figure 7. 80 kbps Limited Distance Modem with EIA-232-D Interface (Master)

MOTOROLA

MC145411

Advance Information

CMOS LSI
(LOW-POWER COMPLEMENTARY MOS)

BIT RATE GENERATOR

3

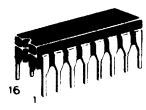
BIT RATE GENERATOR

The MC145411 bit rate generator is constructed with complementary MOS enhancement mode devices. It utilizes a frequency divider network to provide a wide range of output frequencies.

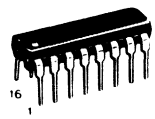
A crystal controlled oscillator is the clock source for the network. A two-bit address is provided to select one of four multiple output clock rates.

Applications include a selectable frequency source for equipment in the data communications market, such as teleprinters, printers, CRT terminals, and microprocessor systems.

- Single 5.0 V (±5%) Power Supply
- Internal Oscillator Crystal Controlled for Stability (to 4 MHz)
- Sixteen Different Output Clock Rates
- 50% Output Duty Cycle
- Programmable Time Bases for One of Four Multiple Output Rates
- Buffered Outputs Compatible with Low Power TTL
- Noise Immunity = 45% of V_{DD} Typical
- Diode Protection on All Inputs
- External Clock May be Applied to Pin 13
- Internal Pullup Resistor on Reset Input

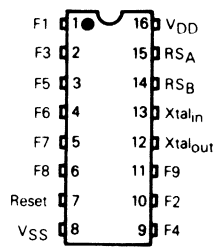


L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

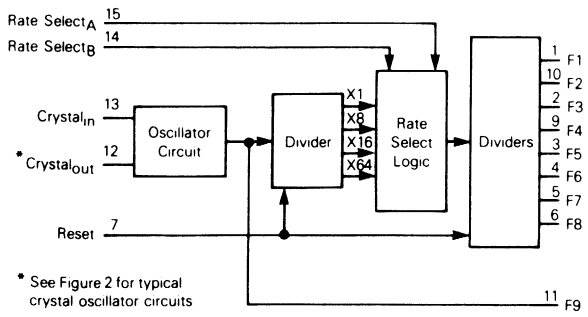
PIN ASSIGNMENT



MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

Rating	Symbol	Value	Unit
DC Supply Voltage Range	V_{DD}	5.25 to −0.5	V
Input Voltage, All Inputs	V_{in}	V_{DD} + 0.5 to V_{SS} − 0.5	V
DC Current Drain per Pin	I	10	mA
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

BLOCK DIAGRAM



* See Figure 2 for typical crystal oscillator circuits

** When Reset = 0, outputs F1 thru F8 = 0, output F9 = 1.

V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ADI1029

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} V	−40°C		25°C			+85°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Supply Voltage	V_{DD}	–	4.75	5.25	4.75	5.0	5.25	4.75	5.25	V
Output Voltage "0" Level	V_{out}	5.0	–	0.05	–	0	0.05	–	0.05	V
"1" Level		5.0	4.95	–	4.95	5.0	–	4.95	–	V
Input Voltage										V
(V_O = 4.5 or 0.5 V)	V_{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 0.5 or 4.5 Vdc)	V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	
Output Drive Current										mA
(V_{OH} = 2.5 V) Source	I_{OH}	5.0	−0.23	–	−0.20	−1.7	–	−0.16	–	
(V_{OL} = 0.4 V) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	
Input Current	I_{in}									μA
Pins 13, 14, 15		–	–	±0.1	–	±0.00001	±0.1	–	±1.0	
Pin 7		5.0	–	–	−1.5	–	−7.5	–	–	
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation	P_Q	5.0	–	2.5	–	0.015	2.5	–	15	mW
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	–	–	$P_D = (7.5\ mW/MHz)\ f + P_Q$					mW
Output Rise Time** $t_r = (3.0\ ns/pF)\ C_L + 25\ ns$	t_{TLH}	5.0	–	–	–	70	200	–	–	ns
Output Fall Time** $t_f = (1.5\ ns/pF)\ C_L + 47\ ns$	t_{THL}	5.0	–	–	–	70	200	–	–	ns
Input Clock Frequency	f_{CL}	5.0	–	4.0	–	–	4.0	–	4.0	MHz
Clock Pulse Width	$t_{W(C)}$	–	200	–	200	–	–	200	–	ns
Reset Pulse Width	$t_{W(R)}$	–	500	–	500	–	–	500	–	ns

†For dissipation at different external capacitance (C_L) refer to corresponding formula:
$P_T(C_L) = P_D + 2.6 \times 10^{-3}(C_L - 15\ pF)\ V_{DD}^2 f$
where: P_T, P_D in mW, C_L in pF, V_{DD} in V, and f in MHz.
**The formula given is for the typical characteristics only.

TABLE 1A — OUTPUT CLOCK RATES

Rate Select		Rate
B	A	
0	0	X1
0	1	X8
1	0	X16
1	1	X64

TABLE 1B — 1.843 MHz Crystal Output Rates

Output Number	Output Rates (Hz)			
	×64	×16	×08	×01
F1	614.4 k	153.6 k	76.8 k	9600
F2	230.4 k	57.6 k	28.8 k	3600
F3	153.6 k	38.4 k	19.2 k	2400
F4	115.2 k	28.8 k	14.4 k	1800
F5	76.8 k	19.2 k	9600	1200
F6	38.4 k	9600	4800	600
F7	19.2 k	4800	2400	300
F8	9600	2400	1200	150
F9*	1.843 M	1.843 M	1.843 M	1.843 M

*F9 is buffered oscillator output.

TABLE 1C — 3.6864 MHz Output Rates

Output Number	Output Rates (Hz)			
	×64	×16	×08	×01
F1	1.22 M	307.2 k	153.6 k	19.2 k
F2	460.8 k	115.2 k	57.6 k	7200
F3	307.2 k	76.8 k	38.4 k	4800
F4	230.4 k	57.6 k	28.8 k	3600
F5	153.6 k	38.4 k	19.2 k	2400
F6	76.8 k	19.2 k	9600	1200
F7	38.4 k	9600	4800	600
F8	19.2 k	4800	2400	300
F9*	3.6864 M	3.6864 M	3.6864 M	3.6864 M

*F9 is buffered oscillator output.

FIGURE 1 – DYNAMIC SIGNAL WAVEFORMS

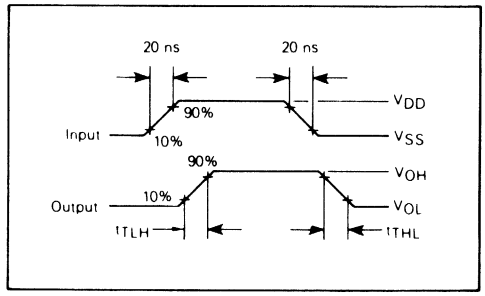
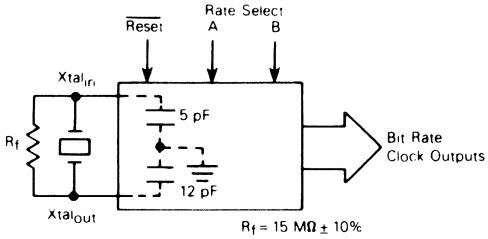


FIGURE 2 – TYPICAL CRYSTAL OSCILLATOR CIRCUIT



Crystal Specifications

Crystal Mode	Parallel
Frequency	1 8432 MHz or 3 6864 MHz ± 0.05% @ 13 pF
R_S	540 Ω max
C_0	7 0 pF max
Temperature Range	0 to 70°C
Test Level	1 mW
Test Set	TS – 330/TSM or Equivalent

MOTOROLA

MC 145412
MC 145413

PULSE/TONE REPERTORY DIALER

The MC145412 and MC145413 are silicon gate, monolithic CMOS integrated circuits which convert keyboard inputs into either pulse or DTMF outputs for telephone dialing. All of the features for implementing pulse or DTMF dialing are provided. Additionally, both parts provide last number redial and repertory memory.

Both parts work with either a 3 x 4 or 4 x 4 keyboard, and have a four second pause input. When used with a 4 x 4 keypad, the MC 145413 provides a keypad selectable pause/switch function which couples a four second pause with a switch in dialing modes (DTMF to pulse and vice versa). This dialing mode change is possible in all dialing sequences (normal, redial, and recall). The MC145412 requires manual switching of dialing modes.

The repertory memory can store nine, 18 digit numbers Manual and automatic dialing can be cascaded in any order. During repertory memory programming, dialing outputs are disabled.

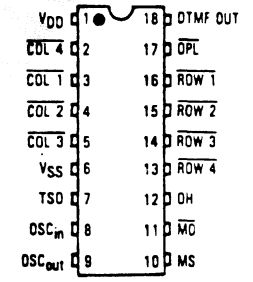
Both parts provide a 500 hertz tone signal output in the pulse dialing mode for user feedback. The mute output can be used to isolate the receiver from dialing outputs. The dialer can be controlled by an MCU.

- The MC145412 is Pin Compatible with LR 4803 (except Pin 7) and the MC145413 Adds Keypad Selectable Switching of Dialing Modes
- Single Pin Switchable Between DTMF, 10 pps and 20pps
- Memory Storage for 9, 18 Digit Numbers, Plus Last Number Redial
- Uses Standard 2-of-7 or 2-of-8 or Form A Type Keyboards
- Uses 3.579545 MHz Colorburst Crystal
- Telephone Line Powered
- Stand Alone DTMF Dialer/Stand Alone Pulse Dialer
- Silicon Gate CMOS Technology for 2.5 - 6.0V Low Power Operation

CMOS
(SILICON GATE)

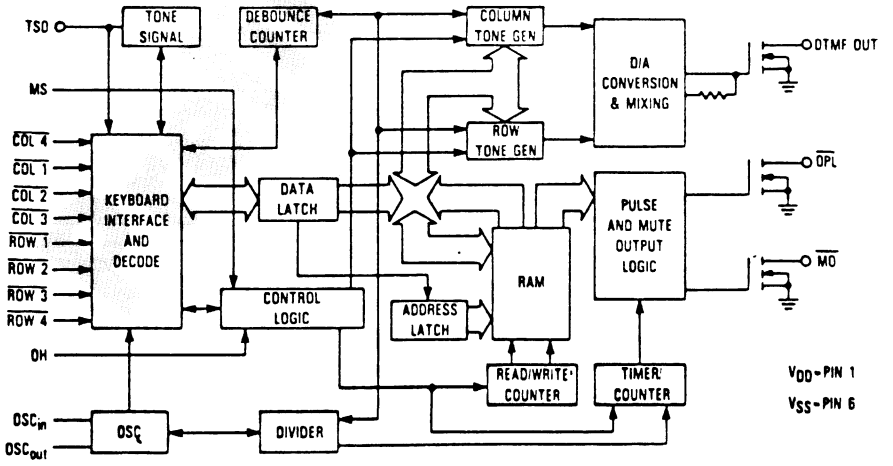
PULSE/TONE DIALER

PIN ASSIGNMENT



P SUFFIX
PLASTIC
CASE 707

BLOCK DIAGRAM



MOTOROLA

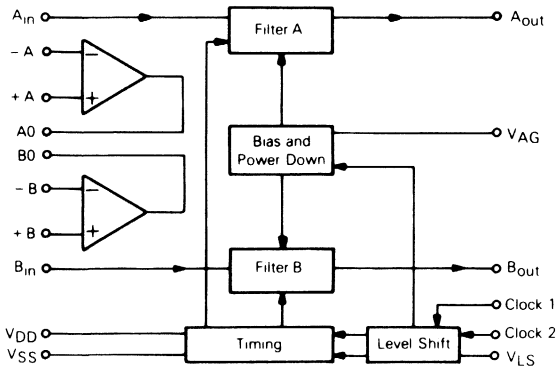
MC145414

DUAL TUNABLE LOW PASS SAMPLED DATA FILTERS

The MC145414 is sampled data, switched capacitor filter IC intended to provide band limiting and signal restoration filtering. It is capable of operating from either a single or split power supply and can be powered-down when not in use. Included on the IC are two totally uncommitted op amps for use elsewhere in the system as I to V converters, gain adjust buffers, etc.

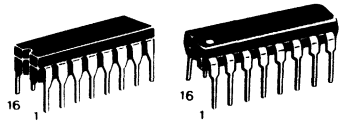
- Two General Purpose 5th Order Elliptic Low Pass Filters
- Low Operating Power Consumption – 30 mW (Typical)
- Power Down Capability – 1 mW (Maximum)
- ±5 to ±8 Volt Power Supply Ranges
- TTL or CMOS Compatible Inputs Using VLS Pin
- Two Operational Amplifiers Available to Reduce Component Count
- Useful in LPC or CVSD Speech Applications
- Passband Edges Tunable With Clock Frequency From 1.25 kHz to 10 kHz

BLOCK DIAGRAM



CMOS LSI
(LOW-POWER COMPLEMENTARY MOS)

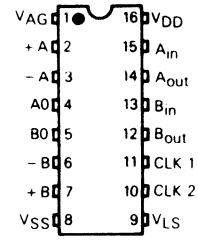
DUAL TUNABLE LOW PASS SAMPLED DATA FILTERS



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



ORDERING INFORMATION

MC14XXXX
- L Ceramic Package
- P Plastic Package

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

DS9557

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}-V_{SS}	−0.5 to 18	V
Input Voltage, All Pins	V_{in}	−0.5 to V_{DD} +0.5	V
DC Current Drain per Pin (Excluding V_{DD}, V_{SS})	I	10	mA
Operating Temperature Range	T_A	0 to 85	°C
Storage Temperature Range	T_{stg}	−65 to 150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}-V_{SS}	10	12	16	V
Clock 1, 2 Frequency	CLK 1, 2	50	128	400	kHz

3

DIGITAL ELECTRICAL CHARACTERISTICS (V_{SS} = 0 V)

Characteristic		Symbol	V_{DD} Vdc	25°C Min	25°C Typ	25°C Max	Unit
Operating Current		I_{DD}	12	–	2.0	4.0	mA
Power-Down Current (PDI = V_{SS})		I_{PD}	12	–	10	40	μA
Input Capacitance		C_{in}	12	–	5.0	–	pF
MODE CONTROL LOGIC LEVELS							
VLS Power-Down Mode		V_{IH}	12 15	11.5 14.5	11 13	– –	V
VLS TTL Mode		–	12 15	4.0 5.0	– –	8 9	V
VLS CMOS Mode		V_{IL}	12 15	– –	– –	0.8 0.8	V
VAG Power-Down Mode		V_{IH}	12 15	11.5 14.5	10.5 13.5	– –	V
VAG Analog-Ground Mode		V_{IL}	12 15	– –	– –	7.0 9.0	V
CMOS LOGIC LEVELS (V_{LS} = V_{SS})							
Input Current Clock 1, 2 (Internal Pulldown Resistors)	"1" Level "0" Level	I_{in}	12 12	– –	50 −0.00001	100 −0.3	μA
Input Voltage Clock 1, 2	"0" Level	V_{IL}	12 15	– –	5.25 6.75	3.0 3.5	V
	"1" Level	V_{IH}	12 15	9.0 11.5	6.75 8.25	–	V
TTL LOGIC LEVELS (VLS = 6 V, V_{SS} = 0 V)							
Input Current Clock 1, 2 (Internal Pulldown Resistor)	"1" Level "0" Level	I_{in}	12 12	– –	50 −0.00001	100 −0.3	μA
Input Voltage Clock 1, 2	"0" Level "1" Level	V_{IL} V_{IH}	12 12	– V_{LS} + 2.0	– –	VLS + 0.8 –	V

ANALOG ELECTRICAL CHARACTERISTICS (V_{DD} = 12 V)

Characteristic		Symbol	25°C Min	25°C Typ	25°C Max	Unit
Input Current	A_{in}, B_{in}	I_{in}	–	±0.00001	±1.0	μA
Input Current	VAG	I_{in}	–	±0.00001	±10	μA
AC Input Impedance (1 kHz)	A_{in}, B_{in}	Z_{in}	–	2	–	MΩ
Input Common Mode Voltage Range	A_{in}, B_{in}, +A, −A, +B, −B	V_{ICR}	2.0	–	10.0	V
Input Offset Current	+A to −A, +B to −B	I_{ID}	–	±10	–	nA
Input Bias Current	+A, −A, +B, −B	I_{IB}	–	±0.10	±1.0	nA
Input Offset Voltage	+A to −A, +B to −B	V_{ID}	–	±10	±70	mV
Output Voltage Range (R_L = 20 kΩ to VAG, R_B = ∞) (R_L = 600 Ω to VAG, R_B = 1.6 kΩ to V_{DD}) (R_L = 900 Ω to VAG, R_B = 1.8 kΩ to V_{DD})	A0, B0, A_{out}, B_{out}	V_{OR}	 1.5 3.0 2.5	 – – –	 10.5 8.3 9.0	V
Small Signal Output Impedance (1 kHz)	A_{out} B_{out}	Z_O	– –	50 50	– –	Ω
Output Current (V_O = 10.5 V) (V_O = 1.5 V)	 A_{out}, B_{out}, A0, B0 A_{out}, B_{out}, A0, B0	 I_{OH} I_{OL}	 −200 5	 −400 7.5	 – –	 μA mA
Unity Gain Output Noise	A0, B0	–	–	15	–	μVrms

FILTER A SPECIFICATIONS

(V_{DD} − V_{EE} = 12 V, Clock 1, 2 = 128 kHz, V_{in} = 0 dBm0, full scale = +3 dBm0, 7 V p-p)

Characteristic		25°C Min	25°C Typ	25°C Max	Unit
Gain (1020 Hz)		17.4	18	18.6	dB
Passband Ripple (50 Hz to 3000 Hz)		–	0.24	1.0	dB
Out of Band Response 3400 Hz 4000 Hz-4600 Hz 4600 Hz-64 kHz		 – −10 −25	 −0.8 −15.5 −33.0	 −1.5 – –	dB
Output Noise (A_{in} = VAG)	ref to 900 Ω	–	10	17	dBrnc0
Dynamic Range		76	83	–	dB
Differential Group Delay 1150 to 2300 kHz Delay 1000 to 2500 kHz Delay 800 to 2700 kHz Delay		 – – –	 – – –	 – – –	μs
Power Supply Rejection Ratio (V_{DD} = 12 V + 0.1 V_{RMS} @ 1 kHz)		–	36	–	dB
Crosstalk (A_{in} = VAG, B_{in} = 0 dBm0 Output at A_{out} at 3 kHz)		–	76	–	dB

FILTER B SPECIFICATIONS (V_{DD} − V_{EE} = 12 V, Clock 1, 2 = 128 kHz, V_{in} = 0 dBm0, full scale = +3 dBm0, 7 V p-p)

Characteristic	25°C Min	25°C Typ	25°C Max	Unit
Gain (1020 Hz)	−0.7	±0.15	+0.7	dB
Passband Ripple (300 Hz to 3000 Hz)	–	0.22	1.0	dB
Response 3400 Hz 4000 Hz-4600 Hz 4600 Hz-64 kHz	 – −10 −28	 −0.8 −15.5 −33.0	 −1.7 – –	dB
Output Noise (300 Hz-3400 Hz)	–	8	14	dBrnc0
Dynamic Range (7 V p-p Max)	79	87	–	dB
Differential Group Delay 1150 to 2300 kHz Delay 1000 to 2500 kHz Delay 800 to 2700 kHz Delay	 – – –	 – – –	 – – –	μs
Crosstalk (B_{in} = VAG, A_{in} = 0dBm0 @ 3 kHz Output at LPO @ 3 kHz)	–	76	–	dB
Power Supply Rejection Ratio	–	36	–	dB

3

SWITCHING CHARACTERISTICS ($V_{DD} - V_{SS} = 10$ V, $T_A = 25°C$)

Characteristics		Symbol	0 to 70°C			Units
			Min	Typ	Max	
Input Rise Time Input Fall Time	Clock 1, 2	t_{TLH} t_{THL}	–	–	4	μs
Pulse Width	Clock 1, 2	t_{WH}	200	–	–	ns
Clock Pulse Frequency	Clock 1, 2	f_{CL}	50	–	400	kHz
Clock 1, 2 Duty Cycle		–	40	–	60	%

FUNCTIONAL DESCRIPTION OF PINS

Pin 1 — V_{AG} (Analog Ground)
This pin should be held at approximately $(V_{DD}-V_{EE})/2$. All analog inputs and outputs are referenced to this pin. If this pin is brought to within approximately 1.0 V of V_{DD}, the chip will be powered down.

Pin 2 — +A
Non-inverting input of op-amp A.

Pin 3 — −A
Inverting input of op-amp A.

Pin 4 — A0
Output of uncommitted op-amp A.

Pin 5 — B0
Output of uncommitted op-amp B.

Pin 6 — −B
Inverting input of op-amp B.

Pin 7 — +B
Non-inverting input of op-amp B.

Pin 8 — V_{SS}
This is the most negative supply pin and digital ground for the package.

Pin 9 — V_{LS} (Logic Shift Voltage)
The voltage on this pin determines the logic compatibility for the Clock 1, 2 inputs. If V_{LS} is within 0.8 V of V_{SS}, the thresholds will be for CMOS operating between V_{DD} and V_{SS}. If VLS is within 1.0 V of V_{DD}, the chip will power down. If V_{LS} is between $V_{DD}-2$ V and $V_{SS}+2$ V, the thresholds for logic inputs at Clock 1, 2 will be between $V_{LS}+0.8$ V and $V_{LS}+2.0$ V for TTL compatibility.

Pin 10 — Clock 1
Always tie clock 1 and clock 2 together.

Pin 11 — Clock 2
Always tie clock 1 and clock 2 together.

Pin 12 — B_{out} (Lowpass Filter B)
This is the output of B lowpass filter.

Pin 13 — B_{in} (Lowpass Filter B)
This is the input to filter B.

Pin 14 — A_{out} (Low pass Filter A)
This pin is the output to filter A.

Pin 15 — A_{in} (Lowpass Filter A)
This is the input to filter A.

Pin 16 — V_{DD}
Nominally 12 volts.

NOTE: Both VAG and VLS are high-impedance inputs.

FILTER DESCRIPTION

FILTER A DESCRIPTION

Filter A of the MC145414 is a 5-pole elliptic tunable lowpass filter operating at a sampling rate determined by clock 1 and clock 2. This filter provides band limiting that is a direct function of clock 1 and clock 2. With a 128 kHz clock, the band limiting frequency is 3.6 kHz. By dividing the clock in half to 64 kHz, the band limiting frequency is cut in half to 1.8 kHz (as illustrated in Figure 1). Likewise by doubling the clock, the cutoff point will double (as illustrated in Figures 3 and 4). The clock frequency can be varied from 50 kHz to 400 kHz. Filter A, unlike filter B, has a gain of 18 db. Because the MC145414 is a switch capacitance filter, the sampled output signal will have switching noise present near multiples of the switching frequency; a single-pole RC filter may be required to reduce this.

To provide 50/60 Hz and 15 Hz rejection, a 3-pole Chebychev highpass filter can be externally realized with the MC145414 by using the uncommitted op-amps as an active filter. This is shown in Figure 5 and 6.

FILTER B DESCRIPTION

Filter B in the MC145414 consists of a 5-pole elliptic tunable lowpass filter operating at a sampled rate determined by clock 1 and clock 2. Filter B is functionally similar to filter A, except filter B has unity gain.

Clock 1 and 2

Logic levels of these signals can be either TTL or CMOS compatible. Choice of logic level can be user determined by applying the appropriate voltage to the level shift control pin, VLS. Clock 1, 2 pins should be tied together.

Power Down

The MC145414 may be powered down by bringing VAG to within 1.7 V of V_{CC} or by bringing VLS to within 1.7 V of V_{DD}

FIGURE 1 – FILTER A AND B LOWPASS CHARACTERISTICS WITH CLOCK 1 AND 2 AT 64 kHz

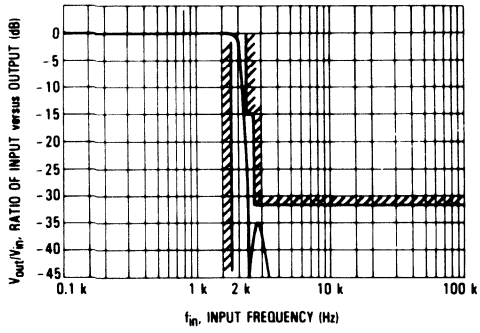
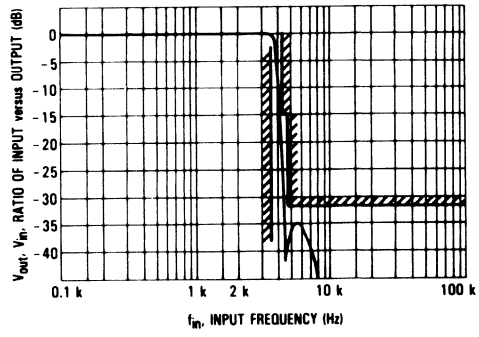


FIGURE 2 – FILTER A AND B LOWPASS CHARACTERISTICS WITH CLOCK 1 AND 2 AT 128 kHz



3

FIGURE 3 – FILTER A AND B LOWPASS CHARACTERISTICS WITH CLOCK 1 AND 2 AT 256 kHz

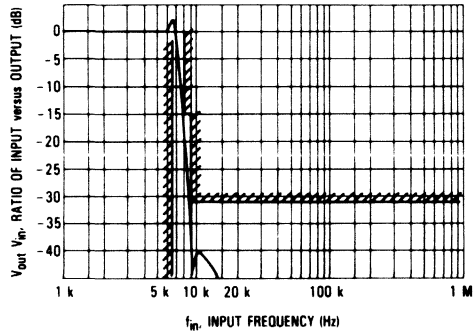


FIGURE 4 – FILTER A AND B LOWPASS CHARACTERISTICS WITH CLOCK 1 AND 2 AT 400 kHz

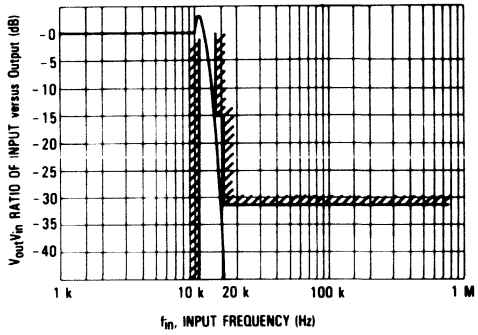
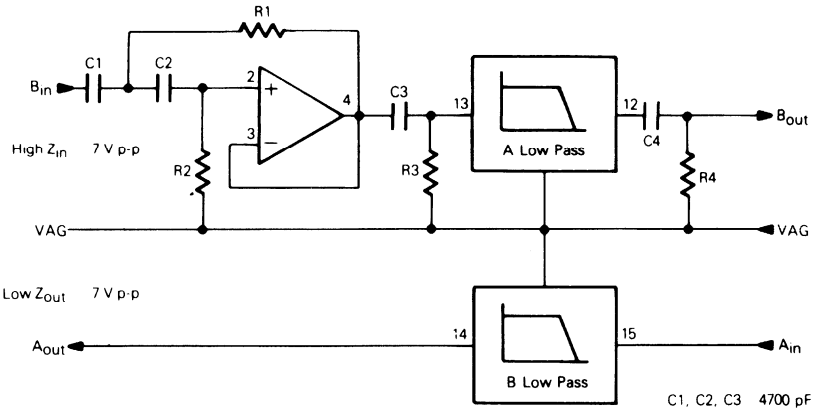


FIGURE 5 — FILTER SCHEMATIC FOR MC145414 WITH 60 Hz REJECT FILTER

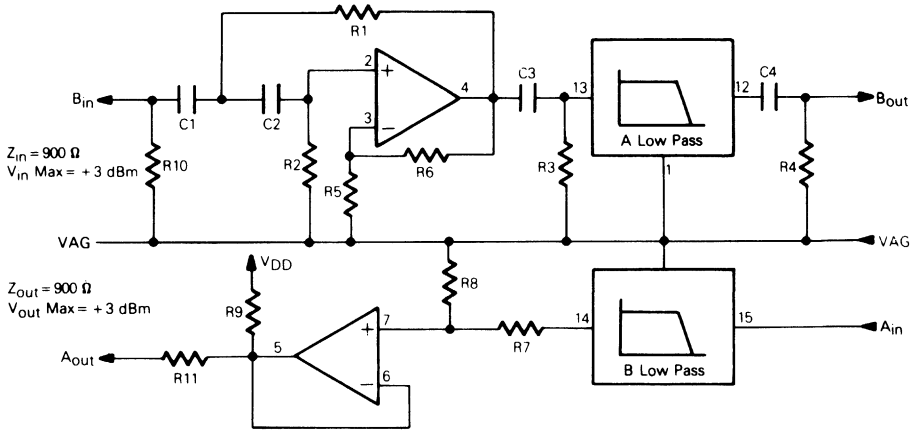


C1, C2, C3	4700 pF	± 1%
C4	0.2 μF	− 20% + 80%
R1	112 kΩ ¼ W	1%
R2	620 kΩ ¼ W	1%
R3	223 kΩ ¼ W	1%
R4	100 kΩ ¼ W	10%

NOTE: In noisy environment, R1-R4 should be 10 kΩ or less to minimize pickup.

AD0318

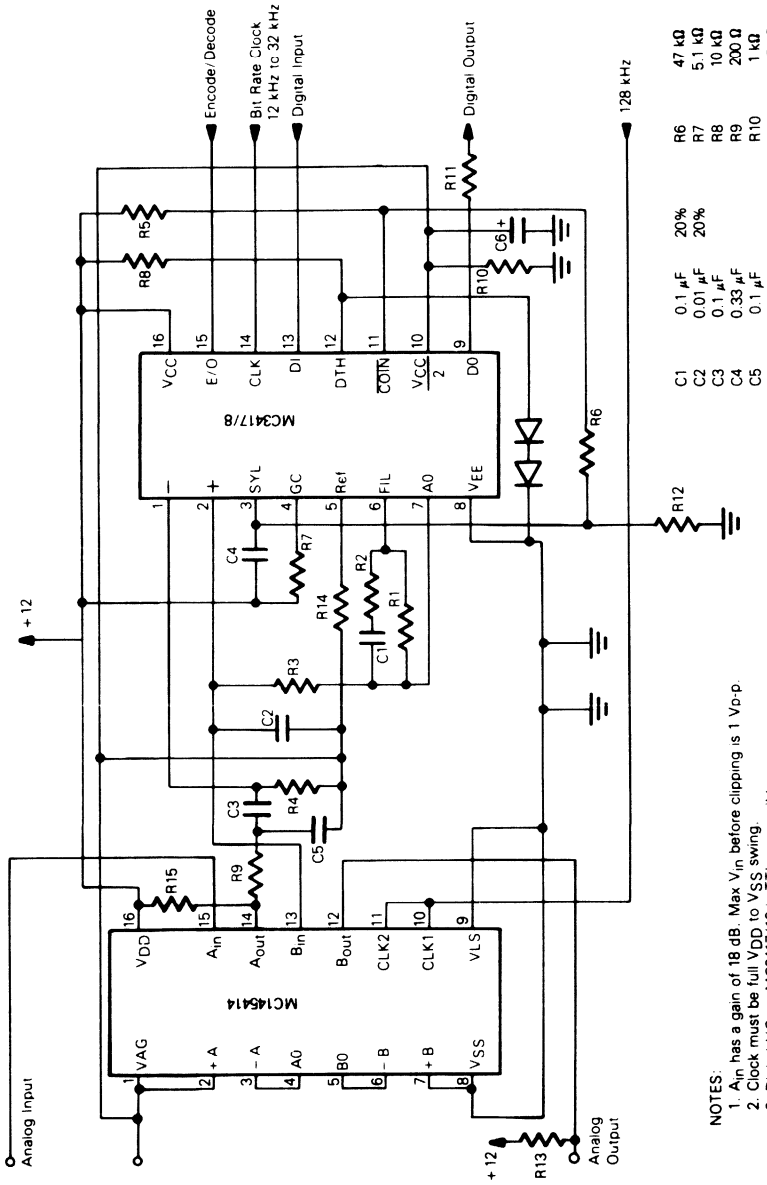
FIGURE 6 — FILTER SCHEMATIC FOR MC145414 WITH 60 Hz REJECTION AND 900 TERMINATION



C1, C2, C3	4700 pF	± 1%	R6	169 kΩ ¼ W	1%
C4	0.2 μF	− 20% + 80%	R7	24 kΩ ¼ W	1%
R1	236 kΩ ¼ W	1%	R8	33 kΩ ¼ W	1%
R2	294 kΩ ¼ W	1%	R9	1.8 kΩ ¼ W	10%
R3	223 kΩ ¼ W	1%	R10	900 Ω ¼ W	1%
R4	100 kΩ ¼ W	10%	R11	900 Ω ¼ W	1%
R5	200 kΩ ¼ W	1%			

AD0319

NOTE: In noisy environment, R1-R4 should be 10 kΩ or less to minimize pickup.



C1	0.1 μF	20%	R6	47 kΩ	5%
C2	0.01 μF	20%	R7	5.1 kΩ	5%
C3	0.1 μF		R8	10 kΩ	5%
C4	0.33 μF		R9	200 Ω	
C5	0.1 μF		R10	1 kΩ	
C6	10 μF		R11	4.7 kΩ	
R1	9.6 kΩ	5%	R12	22 M	
R2	400 kΩ	5%	R13	2 kΩ	
R3	7.5 kΩ	5%	R14	10 kΩ	
R4	15 kΩ	5%	R15	2 kΩ	
R5	8.2 kΩ	5%			

NOTES:
1. A_{in} has a gain of 18 dB. Max V_{in} before clipping is 1 Vp-p.
2. Clock must be full V_{DD} to V_{SS} swing.
3. Digital I/O on MC3417/18 is TTL compatible.

FIGURE 7 — DELTAMOD VOICE DIGITIZER USING MC3417 AND MC145414

3

MOTOROLA

MC145415

Advance Information

CMOS LSI
(LOW-POWER COMPLEMENTARY MOS)

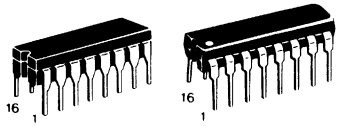
DUAL TUNABLE LINEAR PHASE LOW-PASS SAMPLED DATA FILTERS

3

DUAL TUNABLE LINEAR PHASE LOW-PASS SAMPLED DATA FILTERS

The MC145415 is sampled data, switched capacitor filter IC intended to provide band limiting and signal restoration filtering. It is capable of operating from either a single or split power supply and can be powered-down when not in use. Included on the IC are two uncommitted comparators for use elsewhere in the system.

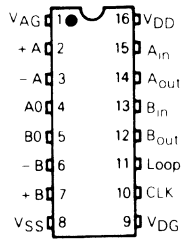
- Two Linear Phase 5th Order Low-Pass Filters
- Low Operating Power Consumption – 20 mW (Typical)
- ±2.5 to ±8 Volt Power Supply Ranges
- CMOS Compatible Inputs Using V_{DG} Pin
- Two Comparators Available to Reduce Component Count
- Useful in High Speed Data Modem Applications
- Pass-Band Edges Tunable With Clock Frequency from 1.25 kHz to 10 kHz



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

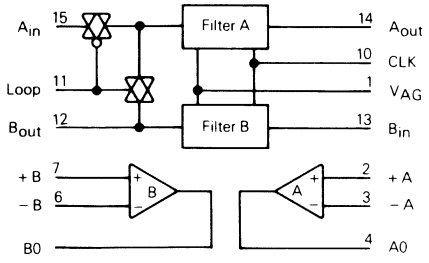
PIN ASSIGNMENT



ORDERING INFORMATION

MC14XXXX
- L Ceramic Package
- P Plastic Package

BLOCK DIAGRAM



V_{DG} = Pin 9
V_{DD} = Pin 16

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ADI983

ANALOG ELECTRICAL CHARACTERISTICS (V_{DD} = 12 V, V_{SS} = 0, V_{AG} = V_{DD}/2, T_A = −40 to 85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Current	A_{in}, B_{in}	I_{in}	–	±0.00001	±10	μA
Input Current	V_{AG}	I_{in}	–	±0.00001	±50	μA
AC Input Impedance (1 kHz)	A_{in}, B_{in}	Z_{in}	–	2	–	MΩ
Input Common Mode Voltage Range	A_{in}, B_{in}, +A, −A, +B, −B	V_{ICR}	2.0	–	10.0	V
Input Offset Current	+A to −A, +B to −B	I_{ID}	–	±10	–	nA
Input Bias Current	+A, −A, +B, −B	I_{IB}	–	±0.10	±1.0	nA
Input Offset Voltage	+A to −A, +B to −B	V_{ID}	–	±10	±70	mV
Output Voltage Range (R_L = 20 kΩ to V_{AG}, R_B = ∞) (R_L = 900 Ω to V_{AG}, R_B = 1.8 kΩ to V_{DD}) (R_L = 600 kΩ to V_{AG}, R_B = 1.6 kΩ to V_{DD})	A_{out}, B_{out}	V_{OR}	 1.5 2.5 3.0	 – – –	 10.5 9.0 8.3	V
Small Signal Output Impedance (1 kHz)	A_{out} B_{out}	Z_o	– –	50 50	– –	Ω
Output Current (V_O = 10.5 V) (V_O = 1.5 V)	 A_{out}, B_{out} A_{out}, B_{out}	 I_{OH} I_{OL}	 −200 5	 −400 7.5	 – –	 μA mA
Comparator Output Current (V_O = 9.5 V) (V_O = 0.5 V)	A0, B0	 I_{OH} I_{OL}	 −1.1 −3.0	 −2.25 −8.8	 – –	 mA

FILTER A SPECIFICATIONS (V_{DD} − V_{SS} = 12 V, Clock = 153.6 kHz, V_{in} = 0 dBm0, full scale = +3 dBm0, 0.875 V p-p, T_A = −40 to 85°C)

Characteristic	Min	Typ	Max	Unit
Gain (300 Hz)	17	18	19	dB
Responses (Ref. 300 Hz) 2400 Hz 4800 Hz	 −3.6 −16	 −3.0 −13.8	 −2.4 −12.8	dB
Idle Noise (A_{in} = V_{AG}, Ref. to 600 Ω)	–	13	24	dBrnc
Dynamic Range (Full Scale Output/Idle Noise)	76	87	–	dB
Deviation From Linear Phase dc to 2400 Hz	–	2.5	–	deg
Power Supply Rejection Ratio (V_{DD} = 12 V +0.1 V_{RMS} @ 1 kHz)	–	36	–	dB
Crosstalk (A_{in} = V_{AG}, B_{in} = 0 dBm0, Output at A_{out} at 3 kHz)	–	76	–	dB

FILTER B SPECIFICATIONS (V_{DD} − V_{SS} = 12 V, Clock = 153.6 kHz, V_{in} = 0 dBm0, full scale = +3 dBm0, 7 V p-p, T_A = −40 to 85°C)

Characteristic	Min	Typ	Max	Unit
Gain (300 Hz)	−0.7	±0.15	+0.7	dB
Response (Ref. 300 Hz) 2400 Hz 4800 Hz	 −3.6 −16	 −3.0 −14.1	 −2.4 −12.8	dB
Idle Noise (300 Hz, Ref to 600 Ω)	–	9	24	dBrnc
Dynamic Range (Full Scale Output/Idle Noise)	76	91	–	dB
Deviation From Linear Phase (dc to 2400 Hz)	–	2.5	–	deg
Power Supply Rejection Ratio (V_{DD} = 12 V +0.1 V_{RMS} @ 1 kHz)	–	36	–	dB
Crosstalk (B_{in} = V_{AG}, A_{in} = 0 dBm0 @ 2 kHz, Output at B_{out})	–	76	–	dB

3

MAXIMUM RATINGS (V_{SS} = 0)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}-V_{SS}	−0.5 to 18	V
Input Voltage, All Pins	V_{in}	−0.5 to V_{DD} +0.5	V
DC Current Drain per Pin (Excluding V_{DD}, V_{SS})	I	10	mA
Operating Temperature Range	T_A	−40 to 85	°C
Storage Temperature Range	T_{stg}	−65 to 150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}-V_{SS}	4.5	5	16	V
Clock Frequency*	CLK	50	128	400	kHz

*Filter frequency response may degrade slightly as clock frequency is increased above 200 kHz.

3

DIGITAL ELECTRICAL CHARACTERISTICS (V_{DD} = 10 V, V_{SS} = 0 V, V_{AG} = V_{DD}/2, T_A = −40 to 85°C)

Characteristic	Symbol	Min	Max	Unit
Operating Current	I_{DD}	–	4	mA
Input Capacitance	C_{in}	–	10	pF
Input Low Voltage (Pins 10, 11)	V_{IL}	–	V_{DG} + 0.3 (V_{DD} − V_{DG})	V
Input High Voltage (Pins 10, 11)	V_{IH}	0.7 × (V_{DD} − V_{DG}) + V_{DD}	–	V
Input Leakage Current (Pins 10, 11)	I_{IL}	V_{DD} − 0.3 (V_{DD} − V_{DG})	2.5	μA
V_{DG} Reference Voltage (Pin 9)	V_{DG}	V_{SS}	V_{DD} − 4.5	V

SWITCHING CHARACTERISTICS ($V_{DD} - V_{SS} = 12$ V, $T_A = -40$ to 85°C)

Characteristics	Symbol	Min	Typ	Max	Units
Input Rise Time (Pin 10)	t_{TLH}	–	–	4	μs
Input Fall Time (Pin 10)	t_{THL}	–	–	4	μs
Pulse Width (Pin 10)	t_{WH}	200	–	–	ns
Clock Pulse Frequency (Pin 10)	f_{CL}	50	–	400	kHz
Clock Duty Cycle (Pin 10)	–	40	–	60	%

FUNCTIONAL DESCRIPTION OF PINS

V_{DD} (PIN 16)
Positive supply pin.

V_{SS} (PIN 8)
This is the most negative supply pin.

V_{AG}, ANALOG GROUND (PIN 1)
This pin should be held at approximately $(V_{DD} - V_{SS})/2$. All analog inputs and outputs are referenced to this pin.

+A (PIN 2)
Non-inverting input of comparator A.

–A (PIN 3)
Inverting input of comparator A.

A0 (PIN 4)
Output of comparator A. This is a standard 'B' series CMOS output.

B0 (PIN 5)
Output of comparator B. This is a standard 'B' series CMOS output.

–B (PIN 6)
Inverting input of comparator B.

+B (PIN 7)
Non-inverting input of comparator B.

V_{DG}, DIGITAL GROUND (PIN 9)
This pin is logic ground reference for the CLK and LOOP pins.

CLK, CLOCK (PIN 10)
This is the clock input that determines the location of the cutoff frequency of the filters as given below:

$$-3 \text{ dB frequency} = f_{CLK} \div 64$$

LOOP (PIN 11)
When this pin is high, the input to filter A is disconnected from the pad and shorted to the filter B output pin. With this pin low, the loop back mode is disabled.

B_{out}, LOW-PASS FILTER B OUTPUT (PIN 12)
This is the output from Filter B.

B_{in}, LOW-PASS FILTER B INPUT (PIN 13)
This is the input to filter B.

A_{out}, LOW-PASS FILTER A OUTPUT (PIN 14)
This pin is the output from Filter A.

A_{in}, LOW-PASS FILTER A INPUT (PIN 15)
This is the input to Filter A.

NOTE: V_{AG} is a high-impedance input.

FILTER DESCRIPTION

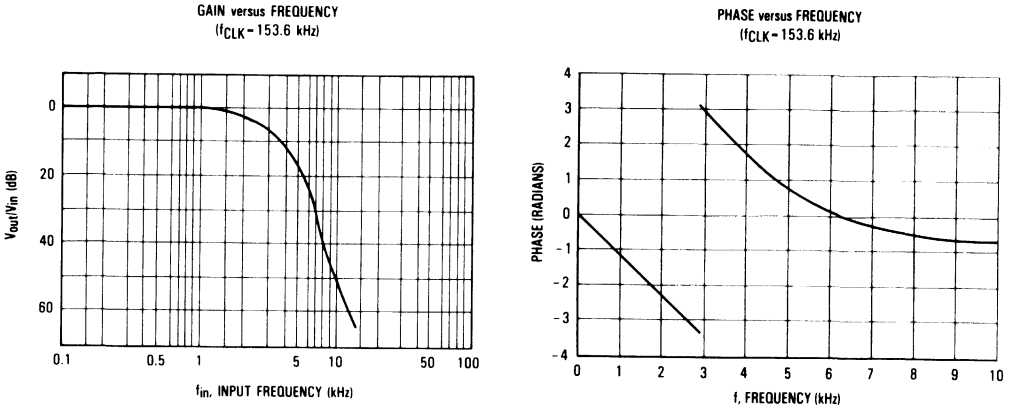
FILTER A DESCRIPTION

Filter A of the MC145415 is a 5-pole tunable linear phase low-pass filter operation at a sampling rate determined by the clock. The break frequency, which is a function of the clock, is calculated by dividing the input clock frequency by 64. With a 128 kHz clock, the band limiting frequency is 2 kHz. By dividing the clock in half to 64 kHz the band limiting frequency is cut in half to 1 kHz. Likewise, by doubling the clock, the cutoff point with double in frequency. The clock frequency can be varied from 50 kHz to 400 kHz. Filter A, unlike filter B, has a gain of 18 dB. Because the MC145415 is a switch capacitance filter, the sampled output signal will have switching components present near multiples of the switching frequency and inputs to these filters should be band-limited to under $\sim 3/4\ f_{CLK}$ to prevent aliasing.

FILTER B DESCRIPTION

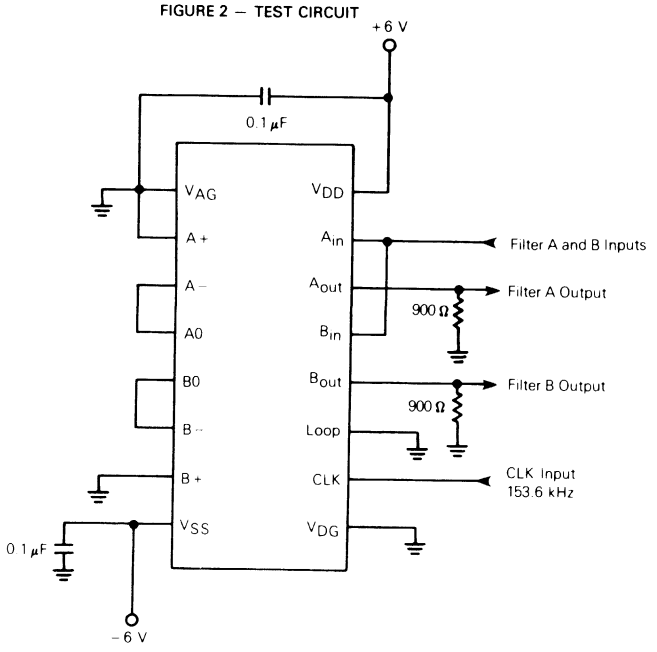
Filter B in the MC145415 consists of a 5-pole tunable linear phase low-pass filter operating at a sampled rate determined by the clock. Filter B is functionally similar to filter A, except filter B has unity gain.

FIGURE 1 — FILTER A AND B LOW-PASS CHARACTERISTICS



NOTES: 1. Break frequency is equal to the clock frequency ÷ 64.
2. Figure 1 illustrates Filter B performance.
Filter A would be 18 dB higher.

FIGURE 2 — TEST CIRCUIT

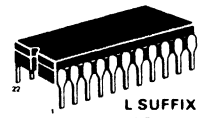


MC145418
MC145419

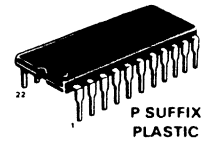
MOTOROLA

Advance Information

Digital Loop Transceivers (DLT)



L SUFFIX
CERAMIC
CASE 736



P SUFFIX
PLASTIC
CASE 708

3

The MC145418 and MC145419 DLTs are high-speed data transceivers that provide 80 kbps full duplex data communication. Intended primarily for use in digital subscriber voice/data telephone systems, these devices can also be used in any digital data transfer scheme (i.e., limited distance modems) where bidirectional data transfer is needed. These devices utilize a 256 kilobaud "squared" modified - DPSK burst modulation technique for transmission.

These devices are designed for compatibility with existing, as well as evolving, telephone switching hardware and software architectures.

The DLT chip set consists of the MC145418 master DLT for use at the telephone switch linecard and the MC145419 slave DLT for use at the remote digital telset and/or data terminal.

The devices employ CMOS technology in order to take advantage of its reliable low-power operation and proven capability for complex analog/digital LSI functions.

- Provides Full Duplex Synchronous 64 kbps Voice/Data Channel and Two 8 kbps Signalling/Data Channels
- Compatible with Existing and Evolving Telephone Switch Architectures and Call Signalling Schemes
- Full Duplex 80 Kilobits Transmission for an 8 kHz Frame Rate
- Protocol Independent
- Single 5 Volt Power Supply
- 22 Pin Package

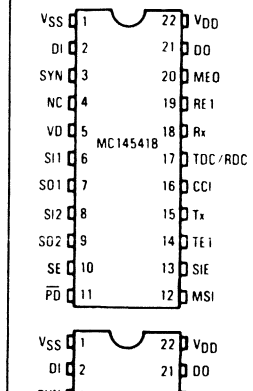
MC145418 Master DLT

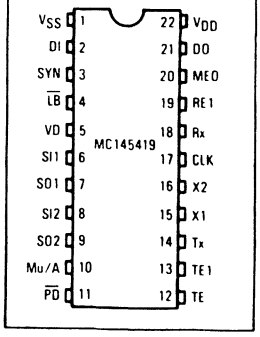
- Pin Controlled Power-Down Feature
- Signalling and Control I/O Capable of Sharing Common Bus Wiring with Other DLTs
- Variable Data Clock - 64 kHz to 2.56 MHz
- Pin Controlled Insertion/Extraction of 8 kbps Channel into LSB of 64 kbps Channel for Simultaneous Routing of Voice and Data Through PCM Voice Path of Telephone Switch

MC145419 Slave DLT

- Compatible with MC14400 Series PCM Mono-Circuits
- Pin Controlled Loop-Back Feature
- Automatic Power-Up/Down Feature
- On-Chip Data Clock Recovery and Generation
- Pin Controlled 500 Hz D3 or CCITT Format PCM Tone Generator for Audible Feedback Applications

PIN ASSIGNMENTS



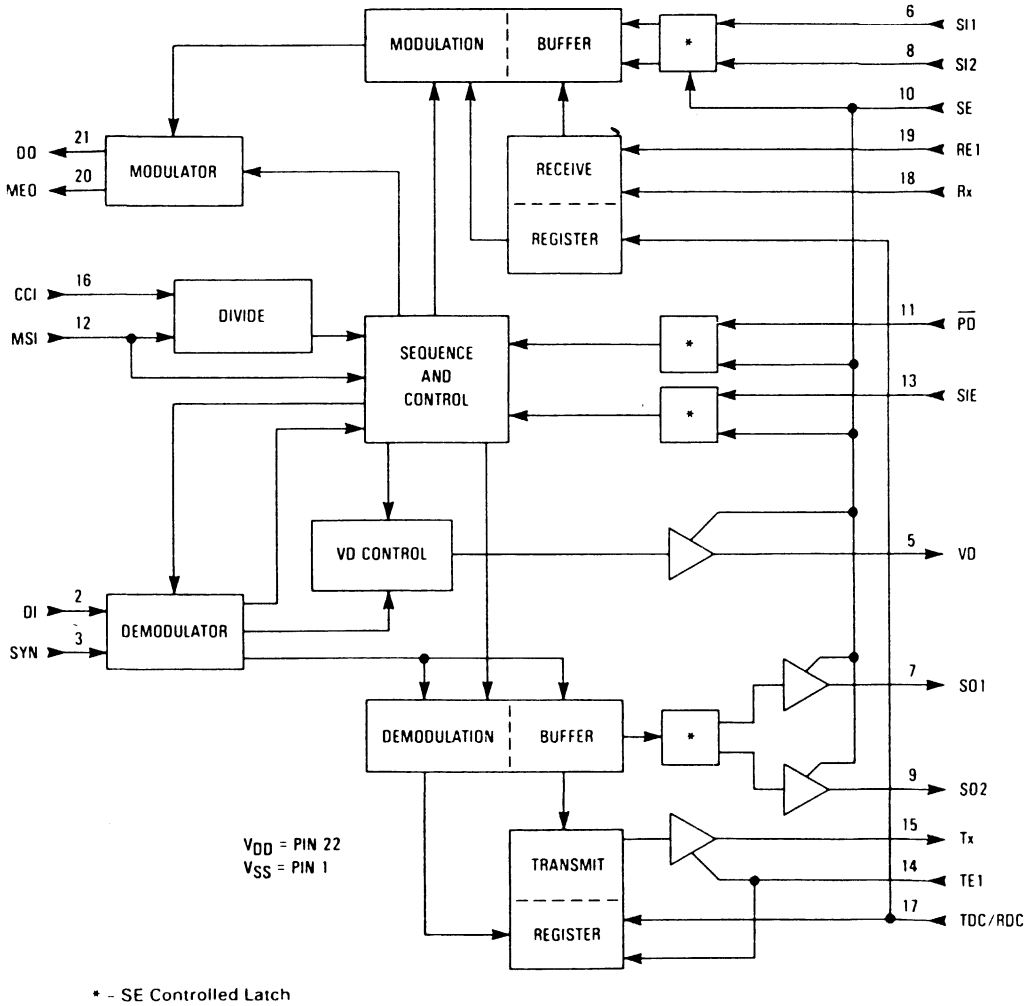


This document contains information on a new product. Specifications and information herein are subject to change without notice.

ADI1234

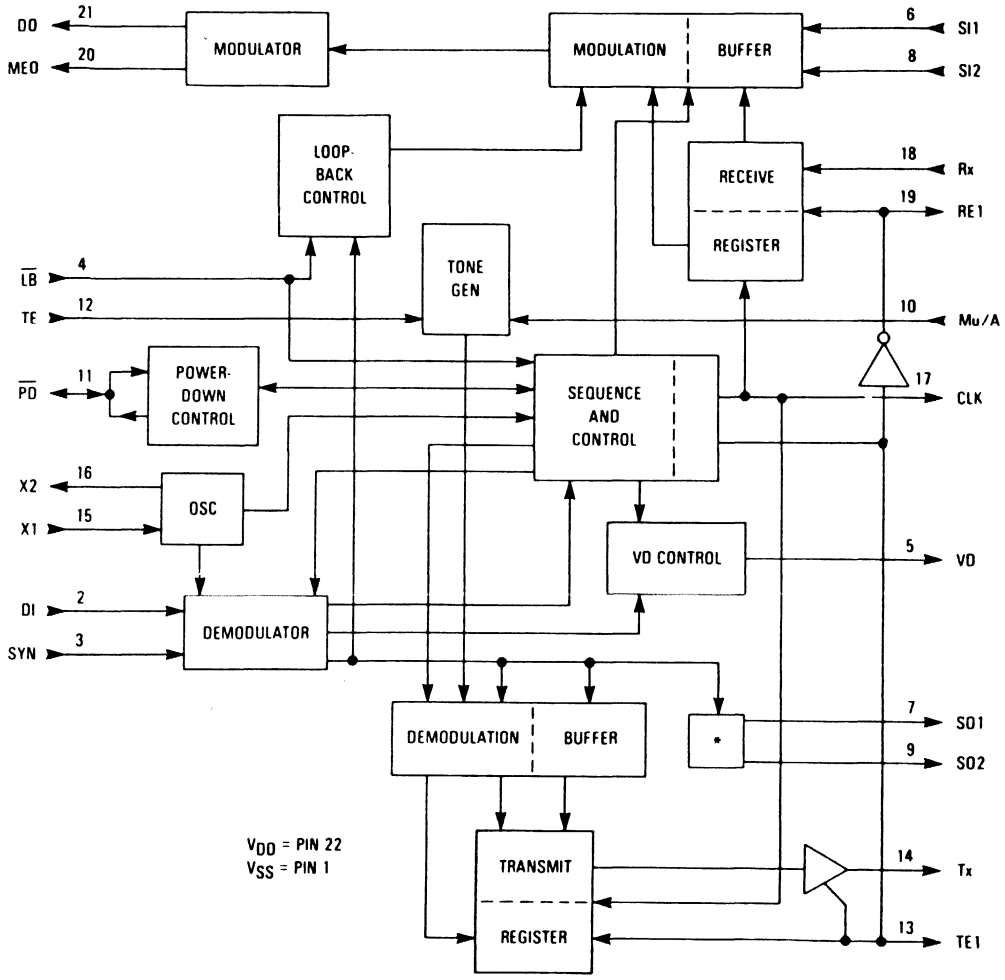
3

MC145418 MASTER DLT BLOCK DIAGRAM



* - SE Controlled Latch

MC145419 SLAVE DLT BLOCK DIAGRAM



* - Signal Bits Output Latch

ABSOLUTE MAXIMUM RATINGS (Voltage Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD} - V_{SS}	-0.5 to 9.0	V
Voltage, Any Pin to V_{SS}	V	-0.5 to V_{DD} +0.5	V
DC Current, Any Pin (Excluding V_{DD}, V_{SS})	I	±10	mA
Operating Temperature	T_A	-40 to +85	°C
Storage Temperature	T_{stg}	-85 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to 70°C)

Parameter	Pins	Min	Max	Unit
DC Supply Voltage	V_{DD}	4.5	5.5	V
Power Dissipation ($\overline{PD}$ = V_{DD}, V_{DD} = 5 V)	V_{DD}	—	15	mW
Power Dissipation ($\overline{PD}$ = V_{SS}, TE = V_{SS})	V_{DD}	—	10	mW
Frame Rate MC145418	MSI	7.9	8.1	kHz
MC145418 - MC145419 Frame Rate Slip (See Note 1)	—	—	0.25	%
CCI Clock Frequency (MSI = 8 kHz)	CCI	—	2.048	MHz
Data Clock Rate MC145418	TDC, RDC	64	2560	kHz
Modulation Baud Rate (See Note 2)	DO	—	256	kHz

NOTES
1. The MC145419 crystal frequency divided by 512 must equal the MC145418 MSI frequency ± 0.25% for optimum operation
2. Assumes crystal frequency of 4.096 MHz for the MC145419 and 2.048 MHz CCI for the MC145418

DIGITAL CHARACTERISTICS (V_{DD} = 5 V, T_A = 0 to 70°C)

Parameter		Min	Max	Unit
Input High Level		3.5	—	V
Input Low Level		—	1.5	V
Input Current		—	±1.0	μA
Input Capacitance		—	10	pF
Output High Current (Except Tx on MC145418 and Tx and $\overline{PD}$ on MC145419)	V_{OH} = 2.5 V V_{OH} = 4.6 V	-1.7 -0.36	— —	mA
Output Low Current (Except Tx on MC145418 and Tx and $\overline{PD}$ on MC145419)	V_{OL} = 0.4 V V_{OL} = 0.8 V	0.36 0.8	— —	mA
$\overline{PD}$ Output High Current (MC145419) (See Note 5)	V_{OH} = 2.5 V V_{OH} = 4.6 V	-90 -10	— —	μA
$\overline{PD}$ Output Low Current (MC145419) (See Note 5)	V_{OL} = 0.4 V V_{OL} = 0.8 V	60 100	— —	μA
Tx Output High Current	V_{OH} = 2.5 V V_{OH} = 4.6 V	-3.4 -0.7	— —	mA
Tx Output Low Current	V_{OL} = 0.4 V V_{OL} = 0.8 V	1.7 3.5	— —	mA
Tx Input Impedance (TE1 = V_{SS}, MC145418)		100	—	kΩ
Crystal Frequency (MC145419) (See Note 3)		4.0	4.4	MHz
PCM Tone (TE = V_{DD}, MC145419)		-22	-18	dBm0
Three-State Current (SO1, SO2, VD, Tx on MC145418, Tx on MC145419)		—	±1	μA
X2 - Oscillator Output High Drive Current (MC145419) (See Note 4)	V_{OH} = 4.6 V	-450	—	μA
X2 - Oscillator Output Low Drive Current (MC145419) (See Note 4)	V_{OL} = 0.4 V	450	—	μA

NOTES
3. The MC145419 crystal frequency divided by 512 must equal the MC145418 MSI frequency ±0.25% for optimum performance
4. Output drive when X1 is being driven from an external clock
5. To overdrive $\overline{PD}$ from a low level to 3.5 V or a high level to 1.5 V requires a minimum of ±800 μA drive capability

MC145418 SWITCHING CHARACTERISTICS (V_{DD} = 5 V, T_A = 25°C, C_L = 50 pF)

Parameter		Fig	Symbol	Min	Max	Unit
Input Rise Time	All Digital Inputs	1	t_r	—	4	μs
Input Fall Time	All Digital Inputs	1	t_f	—	4	μs
Pulse Width	TDC/RDC, RE1, MSI	1	$t_{w(H,L)}$	90	—	ns
CCI Duty Cycle		1	$t_{w(H,L)}$	45	55	%
Data Clock Frequency	TDC/RDC	—	t_{DC}	64	2560	kHz
Propagation Delay Time MSI to SO1, SO2, VD ($\overline{PD}$ = V_{DD}) TDC to Tx		 2 3	 t_{PLH}, t_{PHL}	 — —	 90 90	ns
MSI to TDC/RDC Setup Time		 4	t_{su3} t_{su4}	90 40	— —	ns
TE1/RE1 to TDC/RDC Setup Time		 4	t_{su3} t_{su4}	90 40	— —	ns
Rx to TDC, RDC Setup Time		5	t_{su5}	60	—	ns
Rx to TDC/RDC Hold Time		5	t_{h1}	60	—	ns
SI1, SI2 to MSI Setup Time		6	t_{su6}	60	—	ns
SI1, SI2 to MSI Hold Time		6	t_{h2}	60	—	ns
DO Valid to MEO Rising		10	t_{p7}	—	90	ns
DO Valid to MEO Falling		10	t_{p8}	—	90	ns
DI Valid to SYN Rising		11	t_{su7}	488	1200	ns
DI Valid to SYN Falling		11	t_{su8}	—	3900	ns

MC145419 SWITCHING CHARACTERISTICS (V_{DD} = 5 V, T_A = 25°C, C_L = 50 pF)

Parameter		Fig	Symbol	Min	Max	Unit
Input Rise Time	All Digital Inputs	1	t_r	—	4	μs
Input Fall Time	All Digital Inputs	1	t_f	—	4	μs
Clock Output Pulse Width	CLK	1	$t_{w(H,L)}$	3.8	4.0	μs
Crystal Frequency		—	f_{X1}	4.086	4.1	MHz
Propagation Delay Times TE1 Rising to CLK (TE = V_{DD}) TE1 Rising to CLK (TE = V_{SS}) CLK to TE1 Falling CLK to RE1 Rising RE1 Falling to CLK (TE = V_{DD}) RE1 Falling to CLK (TE = V_{SS}) CLK to Tx TE1 to SO1, SO2		 7 7 7 8 8 8 9 9	 t_{p1} t_{p1} t_{p2} t_{p3} t_{p4} t_{p4} t_{p5} t_{p6}	 -50 438 — — -50 438 — —	 50 538 40 40 50 538 90 90	ns
Rx to CLK Setup Time		5	t_{su5}	60	—	ns
Rx to CLK Hold Time		5	t_{h1}	60	—	ns
SI1, SI2 to TE1 Setup Time		6	t_{su6}	60	—	ns
SI1, SI2 to TE1 Hold Time		6	t_{h2}	60	—	ns

TIMING DIAGRAMS

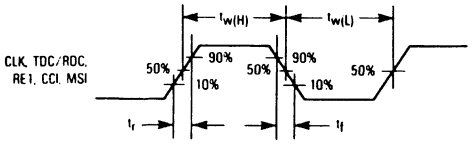


Figure 1

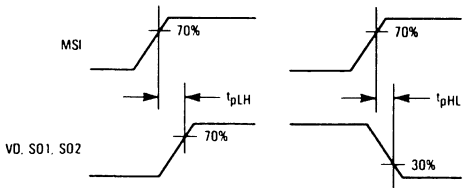


Figure 2

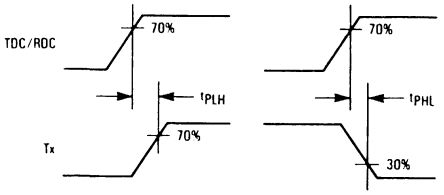


Figure 3

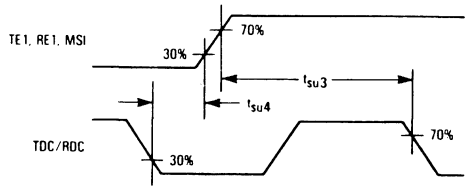


Figure 4

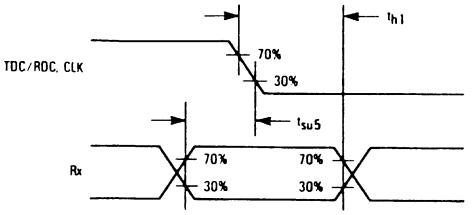


Figure 5

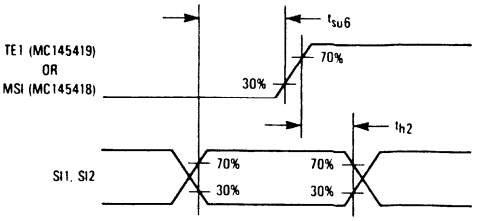


Figure 6

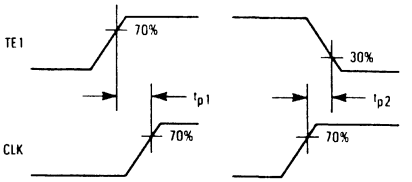


Figure 7

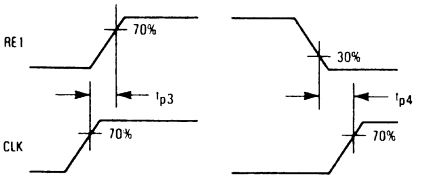


Figure 8

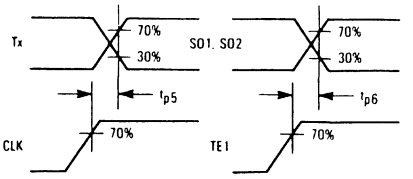


Figure 9

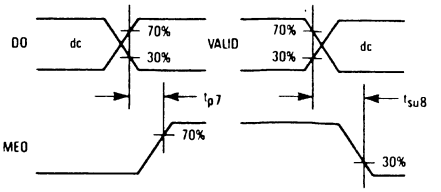


Figure 10

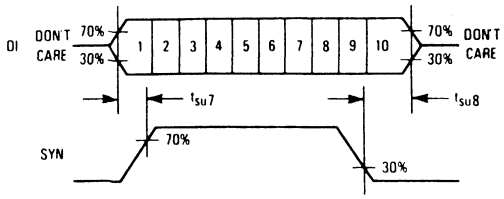


Figure 11

MC145418 MASTER DLT PIN DESCRIPTIONS

V_{DD} — POSITIVE SUPPLY

Normally 5 volts.

V_{SS} — NEGATIVE SUPPLY

This pin is the most negative supply pin, normally 0 volts.

DI — DATA INPUT

This input to the demodulator circuit should be a squared and limited version of the received line signal. (See Figure 15.)

SYN — SYNC INPUT

This input to the demodulator circuit should be a signal which is high when signal energy is detected on the line. (See Figure 14 for typical line interface circuit.)

This signal should be the output of a window comparator with a threshold of approximately 40% of the smallest received line signal. (See Figure 15.)

NC — NO CONNECTION

This pin is not available for use and should be left floating.

VD — VALID DATA OUTPUT

A high on this pin indicates that a valid line transmission has been demodulated. A valid transmission is determined by proper sync and the absence of detected bit errors. VD changes state on the leading edge of MSI when $\overline{PD}$ is high. When $\overline{PD}$ is low, VD changes state at the end of demodulation of a line transmission. VD is a standard B-series CMOS output and is high impedance when SE is held low.

SI1, SI2 — SIGNALING BIT INPUTS

Data on these pins is loaded on the rising edge of MSI for transmission to the slave. The state of these pins is internally latched if SE is held low.

SO1, SO2 — SIGNALING BIT OUTPUTS

These outputs are received signaling bits from the slave DLT and change state on the rising edge of MSI if $\overline{PD}$ is high, or at the completion of demodulation if $\overline{PD}$ is low. These outputs have standard B-series CMOS drive capability and are high impedance if the SE pin is held low.

SE — SIGNAL ENABLE INPUT

If held high, the $\overline{PD}$, SI1, SI2, and SIE inputs and the SO1, SO2, and VD outputs function normally. If held low, the states of these inputs are latched and held internally while the outputs are high impedance. This allows these pins to be bussed with those of other DLTs to a common controller.

$\overline{PD}$ — POWER-DOWN INPUT

If held low, the DLT ceases modulation. In power-down, the only active circuitry is that which is necessary to demodulate an incoming burst and output the signal and valid data bits. Internal data transfers to the transmit and receive registers cease. When brought high, the DLT powers up, and waits three positive MSI edges or until the end of an incoming transmission from the slave DLT and begins transmitting every MSI period to the slave DLT on the next rising edge of the MSI.

MSI — MASTER SYNC INPUT

This pin is the master 8 kHz input system sync and inititates modulation. MSI should be approximately leading-edge aligned with TDC/RDC.

SIE — SIGNAL INSERT ENABLE

This pin, when held high, inserts signal bit 2 received from the slave into the LSB of the outgoing PCM word at Tx and will ignore the SI2 pin and use in its place the LSB of the incoming PCM word at Rx for transmission to the slave. The PCM word to the slave will have its LSB forced low in this mode. In this manner, signal bit 2 to/from the slave DLT is inserted into the PCM words the master sends and receives from the backplane for routing through the PABX for simultaneous voice/data communication. The state of this pin is internally latched if the SE pin is brought and held low.

TE1 — TRANSMIT DATA ENABLE 1 INPUT

This pin controls the outputting of data on the Tx pin. While TE1 is high, the Tx data is presented on the eight rising edges of TDC/RDC. TE1 is also a high-impedance control of the Tx pin. If MSI occurs during this period, new data will be transferred to the Tx output register in the ninth high period of TDC/RDC after TE1 rises; otherwise, it will transfer on the rising edge of MSI. TE1 and TDC/RDC should be approximately leading-edge aligned.

Tx — TRANSMIT DATA OUTPUT

This three-state output pin presents new voice data on the rising edges of TDC/RDC when TE1 is high. (See TE1.)

CCI — CONVERT CLOCK INPUT

A 2.048 MHz clock signal should be applied to this pin. This signal is used for internal sequencing and control. This signal should be coherent with MSI for optimum performance but may be asynchronous if slightly worse error rate performance can be tolerated.

TDC/RDC — TRANSMIT/RECEIVE DATA CLOCK

This pin is the transmit and receive data clock and can be 64 kHz to 2.56 MHz. Data is output at the Tx pin while TE1 is high on the eight rising edges of TDC/RDC after the rising edge of TE1. Data on the Rx pin is loaded into the receive register of the DLT on the eight falling edges of TDC/RDC after a positive transition on RE1. This clock should be approximately leading-edge aligned with MSI.

Rx — RECEIVE DATA

Voice data is clocked into the DLT from this pin on the falling edges of TDC/RDC under the control of RE1.

RE1 — RECEIVE DATA ENABLE 1 INPUT

A rising edge on this pin will enable data on the Rx pin to be loaded into the receive data register on the next falling edges of the data clock, RDC. RE1 and RDC should be approximately leading-edge aligned.

DO — DATA OUTPUT

This B-series output is the square wave Modified - DPSK modulation waveform to be externally buffered and applied to the line. This output is valid only when the MEO output pin is high and is undefined while MEO is low. The external line driver should drive the line in a tri-level manner, controlled by DO and MEO as shown in Figure 15.

MEO — MODULATION ENABLE OUTPUT

This pin, when high, defines the valid data at the DO pin to be valid.

MC145419 SLAVE DLT PIN DESCRIPTIONS

V_{DD} — POSITIVE SUPPLY

Normally 5 volts.

V_{SS} — NEGATIVE SUPPLY

This pin is the most negative supply pin, normally 0 volts.

DI — DATA INPUT

This input to the demodulator circuit should be a squared and limited version of the received line signal. (See Figure 15.)

SYN — SYNC INPUT

This input to the demodulator circuit should be a signal which is high when signal energy is detected on the line. (See Figure 14 for typical line interface circuit.)

This signal should be the output of a window comparator with a threshold of approximately 40% of the smallest received line signal. (See Figure 15.)

$\overline{LB}$ — LOOP-BACK CONTROL

When this pin is held low and $\overline{PD}$ is high (the DLT is receiving transmissions from the master), the DLT will use the eight bits of demodulated PCM data in place of the eight bits of Rx data in the return burst to the master, thereby looping the part back on itself for system testing. SI1 and SI2 operate normally in this mode. CLK will be held low during loop-back operation.

VD — VALID DATA OUTPUT

A high on this pin indicates that a valid line transmission has been demodulated. A valid transmission is determined by proper sync and the absence of detected bit errors. VD changes state on the leading edge of TE1. If no transmissions from the master have been received in the last 250 μs (derived from the internal oscillator), VD will go low without TE1 rising since TE1 is not generated in the absence of received transmissions from the master. (See TE pin description for the one exception to this.)

SI1, SI2 — SIGNALING BIT INPUTS

Data on these pins is loaded on the rising edge of TE1 for transmission to the master. If no transmissions from the master are being received and $\overline{PD}$ is high, data on these pins will be loaded into the part on an internal signal. Therefore, data on these pins should be steady until synchronous communication with the master has been established, as indicated by the high on VD.

SO1, SO2 — SIGNALING BIT OUTPUTS

These outputs are received signaling bits from the master DLT and change state on the rising edge of TE1. These outputs have standard B-series CMOS output drive capability.

$\overline{PD}$ — POWER-DOWN INPUT/OUTPUT

This is a bidirectional pin with weak output drivers such that it can be overdriven externally. When held low, the DLT is powered down and the only active circuitry is: that which is necessary for demodulation, TE1/RE1/CLK generation upon demodulation: the outputting of data received from the master and updating of VD status. When held high, the DLT is powered up and transmits in response to received transmissions from the master. If no received bursts from the master have occured when powered up, for 250 μs (derived from the internal oscillator frequency), the DLT will generate a free running 125 μs internal clock from the internal oscillator and will burst a transmission to the master every other internal 125 μs clock using data on the SI1 and SI2 pins and the last data word loaded into the receive register. The weak output drivers will try to force $\overline{PD}$ high when a transmission from the master is demodulated and will try to force it low if 250 μs have passed without a transmission from the master. This allows the slave DLT to self power-up and down in demand powered-loop systems.

TE — TONE ENABLE

A high on this pin generates a 500 Hz square wave PCM tone and inserts it in place of the demodulated voice PCM word from the master for outputting to the Tx pin to the telset mono-circuit. A high on TE will generate TE1 and CLK from the internal oscillator when the slave is not receiving bursts from the master so that the PCM square wave can be loaded into the mono-circuit. This feature allows the user to provide audio feedback for the telset keyboard depressions except during loop-back. During loop-back of the slave DLT, CLK is defeated so a tone cannot be generated in this mode.

TE1 — TRANSMIT DATA ENABLE 1 OUTPUT

This is a standard B-series CMOS output which goes high after the completion of demodulation of an incoming transmission from the master. It remains high for eight CLK periods and then low until the next burst from the master is demodulated. While high, the voice data just demodulated is output on the first eight rising edges of CLK at the Tx pin. The signaling data just demodulated is output on SO1 and SO2 on TE1's rising edge, as is VD.

Tx — TRANSMIT DATA OUTPUT

This is a standard B-series CMOS output. Voice data is output on this pin on the rising edges of CLK while TE1 is high and is high-impedance when TE1 is low.

X1 — CRYSTAL INPUT

A 4.096 MHz crystal is tied between this pin and X2. A 10 MΩ resistor across X1 and X2 and 25 pF capacitors from X1 and X2 to V_{SS} are required for stability and to insure start-up. X1 may be driven by an external CMOS clock signal if X2 is left open.

X2 — CRYSTAL OUTPUT

This pin is capable of driving one external CMOS input and 15 pF of additional capacitance. (See X1.)

CLK — CLOCK OUTPUT

This is a standard B-series CMOS output which provides the data clock for the telset mono-circuit. It is generated by dividing the oscillator down to 128 kHz and starts upon the completion of demodulation of an incoming burst from the master. At this time, CLK begins and TE1 goes high. CLK will remain active for 16 periods, at the end of which it will remain low until another transmission from the master is demodulated. In this manner, sync from the master is established in the slave and any clock slip between the master and the slave is absorbed each frame. CLK is generated in response to an incoming burst from the master; however, if TE is brought high, then CLK and TE1/RE1 are generated from the internal oscillator until TE is brought low or an incoming burst from the master is received. CLK is disabled when $\overline{LB}$ is held low.

Rx — RECEIVE DATA INPUT

Voice data from the telset mono-circuit is input on this pin on the first eight falling edges of CLK after RE1 goes high.

Mu/A — TONE DIGITAL FORMAT INPUT

This pin determines if the PCM code of the 500 Hz square wave tone, generated when TE is high, is D3 (Mu/A = 1) or CCITT (Mu/A = 0) format.

RE1 — RECEIVE DATA ENABLE 1 OUTPUT

This is a standard B-series CMOS output which is the inverse of TE1 (see TE1). Data is clocked into Rx on the falling edges of CLK while RE1 is high.

DO — DATA OUTPUT

This B-series output is the square wave Modified-DPSK modulation waveform to be externally buffered and applied to the line. This output is valid only when the MEO output pin is high and is undefined while MEO is low. The external line driver should drive the line in a tri-level manner, controlled by DO and MEO as shown in Figure 15.

MEO — MODULATION ENABLE OUTPUT

This pin, when high, defines the valid data at the DO pin to be valid.

BACKGROUND

The MC145418 Master and MC145419 Slave DLT transceiver ICs main application is to bidirectionally transmit the digital signals present at a codec/filter-digital PABX backplane interface over transmission mediums such as telephone wire pairs or fiber optics. This allows the remoting of the mono-circuit in a digital telephone set and enables each set to have a high speed data access to the PABX switching facility. In effect, the DLT allows each PABX subscriber direct access to the inherent 64 kbps data routing capabilities of the PABX.

The DLT provides a means for transmitting and receiving 64 kbps of voice data and 16 kbps of signaling data. The DLT is a two chip set consisting of a Master and a Slave. The master DLT replaces the codec/filter and SLIC on the PABX linecard, and transmits and receives data over the intended transmission medium to the telset. The DLT appears to the linecard and backplane as if it were a PCM codec/filter and has almost the same digital interface features as the MC14400 series mono-circuits. The slave DLT is located in the telset and interfaces the mono-circuit to the transmission medium. By hooking two DLTs back-to-back, a repeater can also be formed. The master and slave DLTs operate in a frame synchronous manner, sync being established at the slave by the timing of the master's transmission. The master's sync is derived from the PABX frame sync.

The communication between master and slave DLTs require a single data link in the transmission medium. Eight bits of voice data and two bits of signaling data are transmitted and received each frame in a half duplex manner; i.e., the slave waits until the transmission from the master is completely received before transmitting back to the master. Transmission occurs at 256 kHz bit rate using a "squared" modified form of DPSK. This "ping-pong" mode will allow transmission of data at distances up to 2 km before turnaround delay becomes a problem. The DLT is so defined as to allow this data to be handled by the linecard, backplane, and PABX as if it were just another voice conversation. This allows existing PABX hardware and software to be unchanged and yet provides switched 64 kbps voice or data communications throughout its service area by simply replacing a subscriber's linecard and telset. A feature in the master allows one of the two signaling bits to be inserted and extracted from the backplane PCM word to allow simultaneous voice and data transmission through the PABX. The slave DLT has a loop-back feature by which the device can be tested in the user system.

The slave DLT has the additional feature of providing a 500 Hz Mu or A law coded square wave to the mono-circuit when the TE pin is brought high. This can be used to provide audio feedback in the telset during keyboard depressions.

Although the DLT was originally designed for a PABX environment, it can be used in any digital synchronous serial environment, such as, computer to computer communications or industrial control.

CIRCUIT DESCRIPTION

GENERAL

The DLT consists of a modulator, demodulator, two intermediate data buffers, sequencing and control logic, and transmit and receive data registers. The data registers inter-

face to the linecard or mono-circuit digital interface signals, the modulator and demodulator provide Modified - DPSK transmission and reception, while the intermediate data registers buffer data between these two sections. The DLT is intended to operate on a single 5 volt supply and can be driven by TTL or CMOS logic.

MASTER OPERATION

In the master, data is loaded into the receive register each frame from the Rx pin under the control of the TDC/RDC clock and the receive data enable, RE1. RE1 controls loading of eight serial bits, henceforth referred to as the voice data word. Each MSI, these words are transferred out of the receive register to the modulation buffer for subsequent modulation onto the line. The modulation buffer takes the received voice data word and the two signaling data input bits on SI1 and SI2 loaded on the MSI rising edge and formats the ten bits into a specific order. This data field is then transmitted in a 256 kHz "squared" Modified-DPSK burst to the remote slave DLT. An example of the modulated data field at DO is shown with the Modulation Enable Output (MEO) in Figure 15. V2-V1 is the differentially driven waveform onto the line in a twisted pair application.

The received signal coming into the demodulator should be a squared digital version of the line signal, shown as DI in Figure 15. The SYN signal which is the output of a window comparator is internally integrated and used by the demodulator's synchronization circuitry along with the first zero crossing of DI to establish the exact position (in time) of the incoming burst for demodulation purposes. The SYN pulse or pulses (output of the window comparator circuitry) must be present for the first eight baud periods of the incoming burst. They may persist longer but they must not occur within one full baud period before the arrival of the following burst. Upon demodulating the return burst from the slave, the decoded data is transferred to the demodulation buffer and the signaling bits are stripped ready to be output on SO1 and SO2 at the next MSI. The voice data word is loaded into the transmit register as described in the TE1 pin description for outputting via the Tx pin at the TDC/RDC data clock rate under the control of TE1. VD is output on the rising edge of MSI. Timing diagrams for the master are shown in Figure 12.

SLAVE OPERATION

In the slave, the synchronizing event is the detection of an incoming transmission from the master as indicated by the completion of demodulation. (The SYN signal and DI function the same as in the Master.) When an incoming burst from the master is demodulated, several events occur. As in the master, data is transferred from the demodulator to the demodulation buffer and the signaling bits are stripped for outputting at SO1 and SO2. Data in the receive register is transferred to the modulation buffer. TE1 goes high loading in data at SI1 and SI2, which will be used in the transmission burst to the master along with the data in the transmit data buffer. At the same time SO1, SO2, and VD are output. Modulation of the burst begins four 256 kHz periods after the completion of demodulation.

While TE1 is high, data is output at Tx on the rising edges of CLK. On the ninth rising edge of CLK, TE1 goes low, RE1 goes high, and data is input to the receive register from the Rx pin on the next eight falling edges of CLK.

The CLK pin is a 128 kHz output that is formed by dividing down the 4.096 MHz crystal frequency by 32. Slippage between the frame rate of the master (as represented by the completion of demodulation of an incoming transmission from the master) and the crystal frequency is absorbed by holding the 16th low period of CLK until the next completion of demodulation. This is shown in the slave DLT timing diagram of Figure 13.

POWER-DOWN OPERATION

In the master, when $\overline{PD}$ is low, the DLT stops modulating and only that circuitry necessary to demodulate the incoming bursts and output the signaling and VD data bits is active. In this mode, if the DLT receives a burst from the slave, the SO1, SO2, and VD pins will be updated upon completion of the demodulation instead of on the rising edge of MSI. The state of these pins will not change until either three rising MSI edges have occurred without the reception of a burst from the slave or until another burst is demodulated, whichever occurs first.

When $\overline{PD}$ is brought high, the master DLT will wait either three rising MSI edges or until the MSI rising edge following the demodulation of an incoming burst before transmitting to the slave. The data for the first transmission to the slave after power-up is loaded into the DLT during the RE1 period prior to the burst for Rx data, and on the present rising edge of MSI for signaling data.

In the slave, $\overline{PD}$ is a bidirectional pin with weak output drivers such that it can be overdriven externally. When held low, the DLT slave is powered down and only that circuitry necessary for demodulation, TE1/RE1/CLK generation upon demodulation, the outputting of Tx data, signaling bits, and VD is active. When held high, the DLT slave is powered up and transmits normally in response to received transmissions from the master. If no bursts have been received from the master within 250 μs after power-up (derived from the internal oscillator frequency), the DLT generates an internal 125 μs free-running clock from the internal oscillator. The slave DLT then bursts a transmission to the master DLT every other 125 μs clock period using data loaded into the Rx pin during the last RE1 period and SI1, SI2 data loaded in on the internal 125 μs clock edge. The weak output drivers will try to force $\overline{PD}$ high when a transmission from the master is demodulated and will try to force it low if 250 μs have passed without a transmission from the master. This allows the slave DLT to self power-up and down in demand powered loop systems.

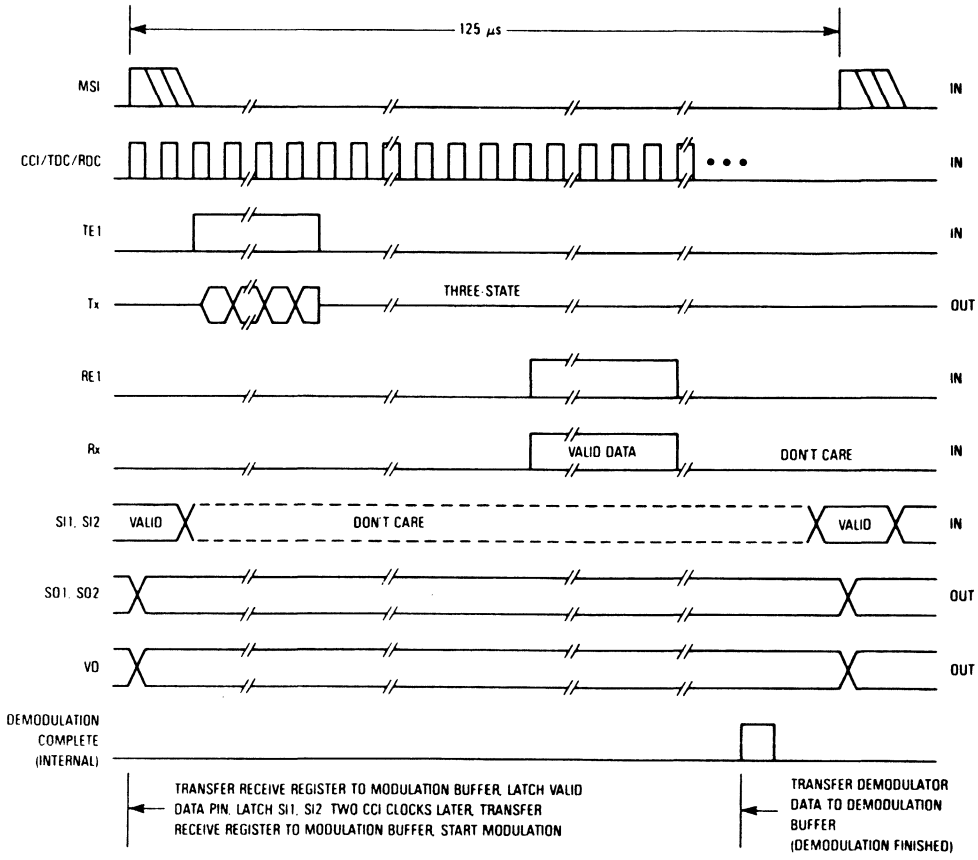


Figure 12. Master DLT Timing

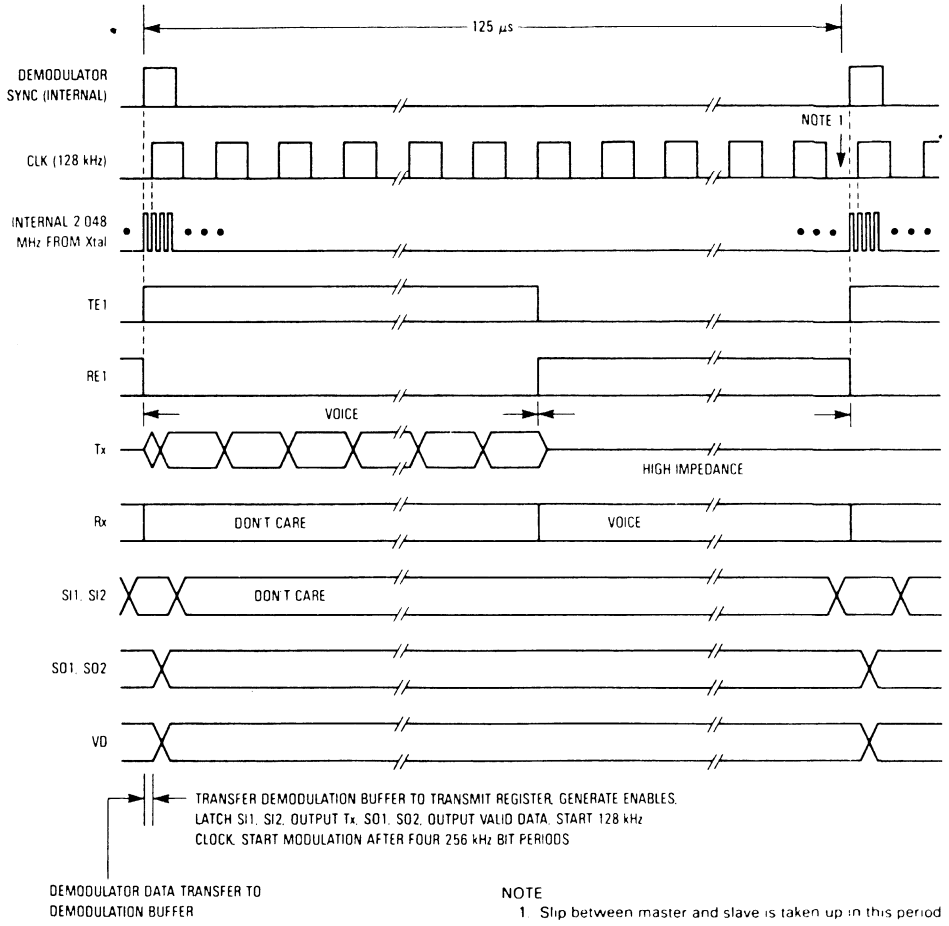


Figure 13. Slave DLT Timing

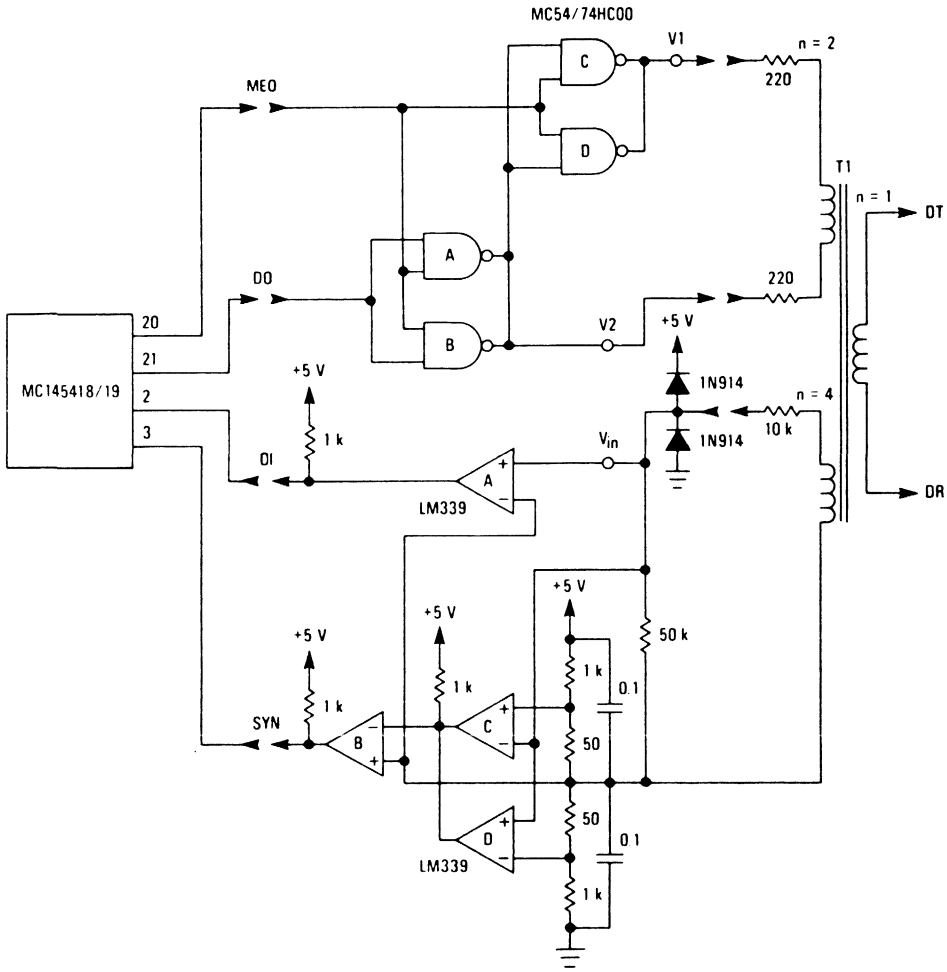
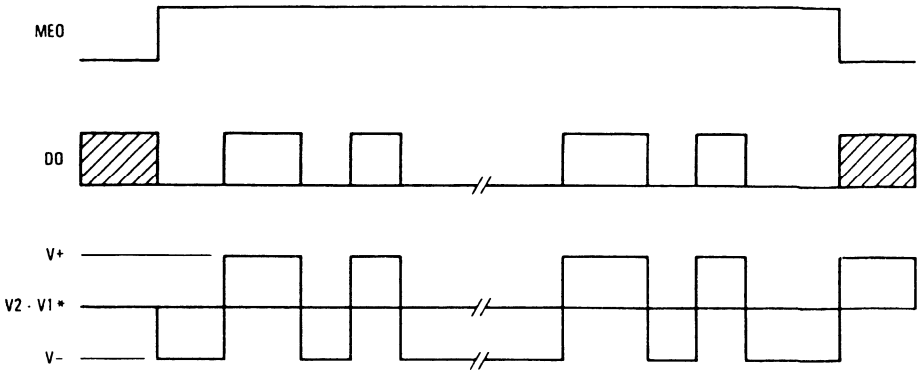
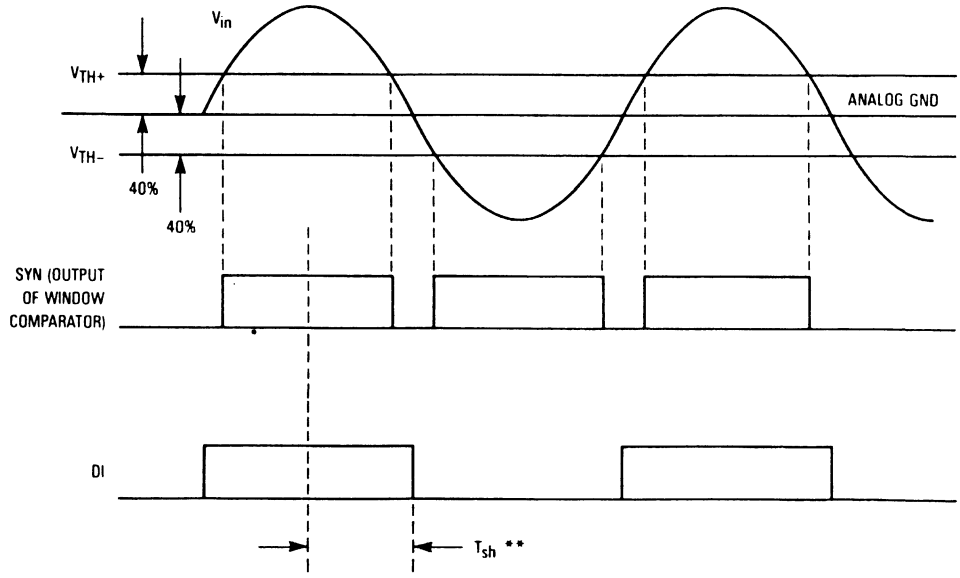


Figure 14. Typical DLT Line Interface



*See Figure 14 for voltages V2, V1. |V+| must equal |V-| within 5%. V2-V1, when MEO is low, must equal (V+ - V-)/2 within 5%



**T_{sh} - SYN should be high a minimum of three 4.096 MHz clock periods before the first zero crossing as indicated by DI state change.

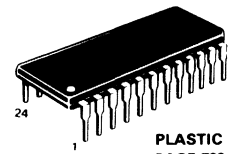
Figure 15. Line Driver Waveforms

MC145421
MC145425

MOTOROLA

Advance Information

ISDN Universal Digital Loop Transceivers II (UDLT II)



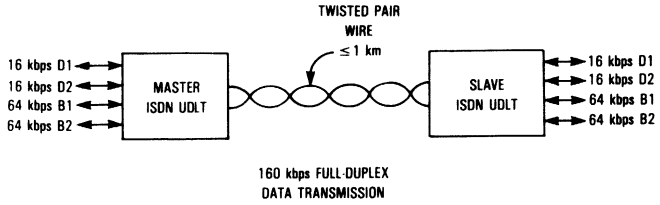
PLASTIC
CASE 709

The MC145421 and MC145425 UDLTs are high-speed data transceivers capable of providing 160 kbps full duplex data communication over 26 awg and larger twisted-pair cable up to 1 km in length. These devices are primarily used in digital subscriber voice and data telephone systems. In addition, the devices meet and exceed the CCITTs recommendations for data transfer rates of ISDNs on a single twisted pair. The devices utilize a 512 kilobaud MDPSK burst modulation technique to supply the 160 kbps full duplex data transfer rates. The 160 kbps rate is provided through four channels. There are two B channels, which are 64 kbps each. In addition, there are two D channels which are 16 kbps each.

The MC145421 and MC145425 UDLTs are designed for upward compatibility with the existing MC145422 and MC145426 80 kbps UDLTs, as well as compatibility with existing and evolving telephone switching hardware and software architectures.

The MC145421 (MASTER) UDLT is designed for use at the telephone switch line card while the MC145425 (SLAVE) UDLT is designed for use at the remote digital telset or data terminal.

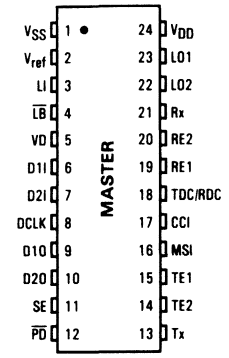
- Employs CMOS Technology, in Order to Take Advantage of Its Proven Capability for Complex Analog and Digital LSI Functions.
- Provides Synchronous Full Duplex 160 kbps Voice and Data Communication in a 2B + 2D Format For ISDN Compatibility.
- Provides the CCITT's Basic Access Data Transfer Rate (2B + D) for ISDNs on a Single Twisted Pair up to 1 km.
- Compatible with Existing and Evolving Telephone Switch Architectures and Call Signalling Schemes.
- Protocol Independent
- Single +5 V Power Supply



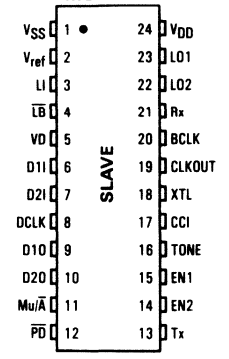
160 kbps FULL-DUPLEX
DATA TRANSMISSION

PIN ASSIGNMENTS

MC145421



MC145425

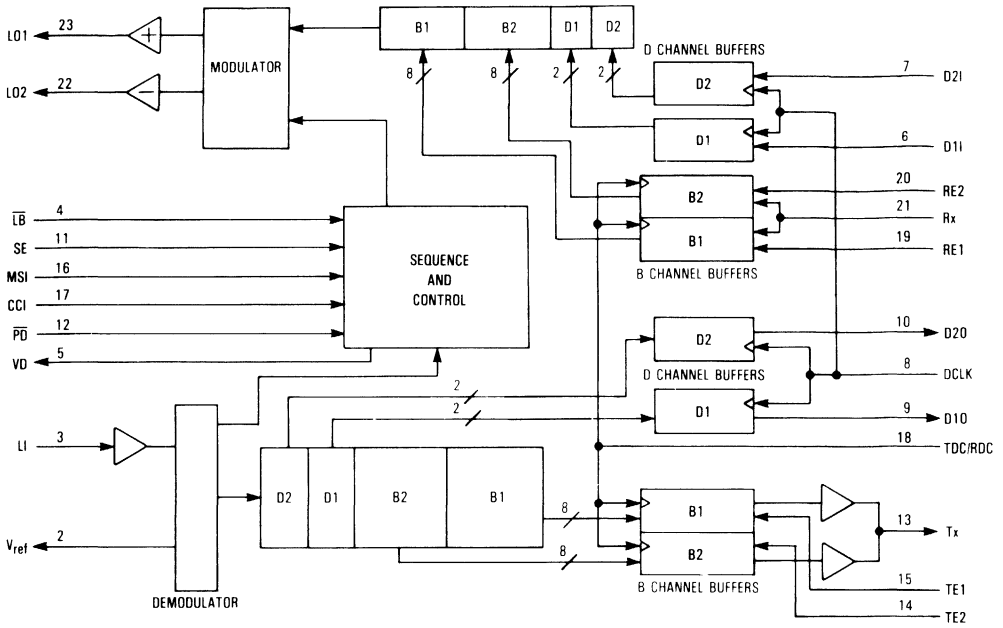


3

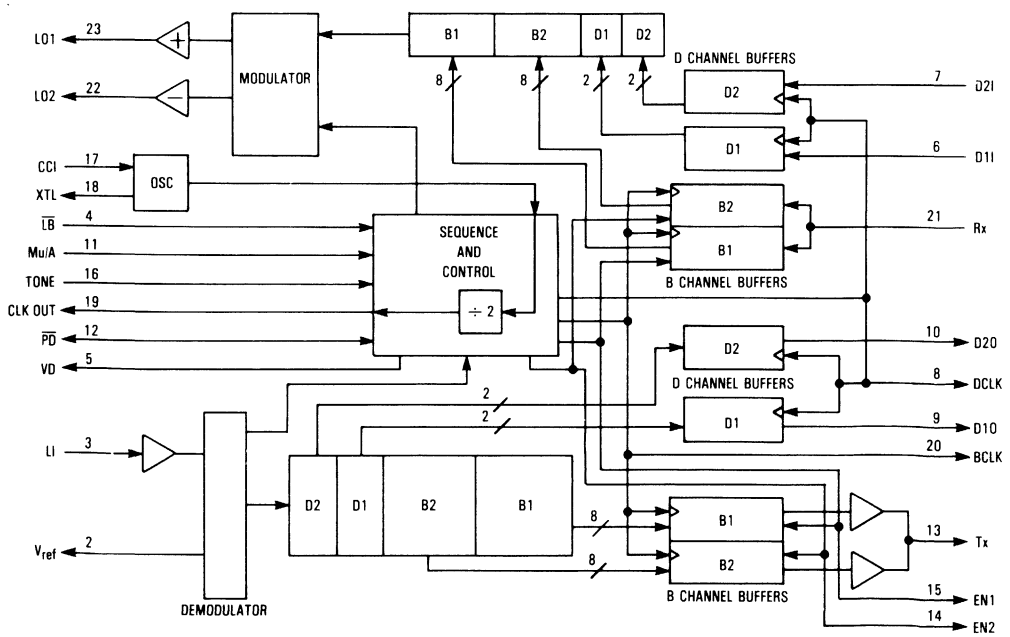
This document contains information on a new product. Specifications and information herein are subject to change without notice.

ADI1251

MC145421 MASTER ISDN BLOCK DIAGRAM



MC145425 SLAVE ISDN BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Voltage Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}-V_{SS}	−0.5 to 6.5	V
Voltage Any Pin to V_{SS}	V	−0.5 to V_{DD} + 0.5	V
DC Current, Any Pin (Excluding V_{DD}, V_{SS})	I	± 10	mA
Operating Temperature	T_A	−40 to +85	°C
Storage Temperature	T_{stg}	−85 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

RECOMMENDED OPERATING CONDITIONS (T_A = −40 to +85°C)

Parameter	Pins	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}	4.5	5.0	5.5	V
Frame Rate MC145421 (See Note 1)	MSI	—	8.0	—	kHz
MC145421/25 Frame Slip Rate (See Note 1)	—	—	—	0.25	%
CCI Clock Frequency	—	—	8.192	8.29	MHz
TDC/RDC Data Clocks (for Master)	—	0.128	—	4.1	MHz
DCLK	—	0.016	—	4.1	MHz
Modulation Baud Rate (CCI/16)	LO1, LO2	—	512	—	kHz

NOTE:

1. The slave's crystal frequency divided by 1024 must equal the master's MSI frequency ± 0.25% for optimum operation. Also, the 8.192 MHz input at the master divided by 1024 must be within 0.048% of the master's 8 kHz MSI clock frequency.

DIGITAL CHARACTERISTICS (V_{DD} = 5 V, T_A = −40 to +85°C)

Parameter		Min	Max	Unit
Input High Level		3.5	—	V
Input Low Level		—	1.5	V
Input Current, V_{DD}		—	15	mA
Input Current (Digital Pins)		—	5	μA
Input Capacitance		—	10	pF
Output High Current (Except Tx on Master and Slave, and $\overline{PD}$ on the Slave)	V_{OH} = 2.5 V_{OH} = 4.6	−1.7 −0.36	— —	mA
Tx Output High Current	V_{OH} = 2.5 V_{OH} = 4.6	−3.4 −0.7	— —	mA
$\overline{PD}$ (Slave Output High Current (See Note 2)	V_{OH} = 2.5	—	−90	μA
Output Low Current (Except Tx on Master and Slave, and $\overline{PD}$ on Slave)	V_{OL} = 0.4 V_{OL} = 0.8	0.36 0.8	— —	mA
Tx Output Low Current	V_{OL} = 0.4 V_{OL} = 0.8	1.7 3.5	— —	mA
$\overline{PD}$ (Slave) Output Low Current (See Note 2)	V_{OL} = 0.4	30	60	μA
Tx Three-State Impedance		100	—	kΩ
XTL Output High Current	V_{OH} = 4.6	—	−450	μA
XTL Output Low Current	V_{OH} = 0.4	450	—	μA

NOTE:

2. To overdrive $\overline{PD}$ from a low level to 3.5 V, or a high level to 1.5 V requires a minimum of ±800 μA drive capability.

ANALOG CHARACTERISTICS (V_{DD} = 5 V, T_A = 0 to 70°C)

Parameter	Min	Max	Unit
Modulation Differential Amplitude RL = 880 Ω (LO1-LO2)	4.6	—	Vpeak
Modulation Differential DC Offset	—	40	mV
V_{ref} Voltage (Typically 9/20•(V_{DD} − V_{SS}))	2.0	2.5	V
PCM Tone Level	−22	−18	dBm
Demodulator Input Amplitude	50	—	mVpeak
Demodulator Input Impedance (LI to V_{ref})	200	300	kΩ

MC145421 MASTER PIN DESCRIPTIONS

V_{DD}—POSITIVE SUPPLY (PIN 24)

The most positive power supply pin, normally +5 volts with respect to V_{SS}.

V_{SS}—NEGATIVE SUPPLY (PIN 1)

The most negative supply pin and logic ground, normally 0 volts.

V_{ref}—REFERENCE OUTPUT (ANALOG GROUND) (PIN 2)

This pin is the output of the internal reference supply and should be bypassed to V_{DD} and V_{SS} with 0.1 μF capacitors. This pin usually serves as an analog ground reference for transformer coupling of the device's incoming bursts from the line. No external dc load should be placed on this pin.

3

LI—LINE INPUT (PIN 3)

This pin is an input to the demodulator for the incoming bursts. The input has an internal 240 kΩ resistor tied to the V_{ref} pin, so an external capacitor or line transformer may be used to couple the input signal to the device with no dc offset.

LO1, LO2—LINE DRIVER OUTPUTS (PINS 23, 22)

These push-pull outputs drive the twisted pair transmission line with a 512 kHz modified DPSK (MDPSK) burst each 125 μs, in other words at an 8 kHz rate. When not modulating the line, these pins are driven to the active high state—being the same potential, they create an ac short. When used in conjunction with feed resistors, proper line termination is maintained.

SE—SIGNAL ENABLE INPUT (PIN 11)

At the time of a negative transition on this pin, an internal latch stores the states of $\overline{LB}$ and $\overline{PD}$ for as long as SE is held low. During this time, the VD, DO1, and DO2 outputs are driven to the high impedance state. When SE is high, all pins function normally.

$\overline{LB}$—LOOP BACK CONTROL (PIN 4)

A low level on this pin ties the internal modulator output to the internal demodulator input which loops the entire burst for testing purposes. During the loopback operation, the LI input is ignored and the LO1 and LO2 drivers are driven to the active high level. The state of this pin is internally latched if the SE pin is held low. This feature is only active when the $\overline{PD}$ input is high.

$\overline{PD}$—POWER DOWN INPUT (PIN 12)

When held low the ISDN UDLT powers down, except the circuitry that is necessary to demodulate an incoming burst and to output VD, B channel and D channel data bits. When $\overline{PD}$ is brought high, the ISDN UDLT powers up. Then, it begins transmitting every MSI period to the slave device, shortly after the rising edge of MSI. The state of this pin is latched if the SE pin is held low.

VD—VALID DATA OUTPUT (PIN 5)

A high level on this pin indicates that a valid line transmission has been demodulated. A valid transmission burst is determined by proper synchronization and the absence of detected bit errors. VD changes state on the rising edge of MSI when $\overline{PD}$ is high. When $\overline{PD}$ is low, VD changes state at the end of demodulation of a transmission burst and does not change again until three MSI rising edges have occurred, at which time it goes low, or until the next demodulation of a burst. VD is a standard B-series CMOS output and is high-impedance when SE is low.

MSI—MASTER SYNC INPUT (PIN 16)

This pin is the master, 8 kHz, frame reference input. The rising edge of MSI loads B and D channel data which had been input during the previous frame into the modulator section of the device and initiates the out-bound burst onto the twisted-pair cable. The rising edge of MSI also initiates the buffering of the B and D channel data demodulated during the previous frame. MSI should be approximately leading edge aligned with the TDC/RDC data clock input pin.

CCI—HIGH-SPEED CLOCK INPUT (PIN 17)

An 8.192 MHz clock should be supplied to this input. The 8.192 MHz input should be 50% duty cycle, however it may free-run with respect to all other clocks without performance degradation.

D1I, D2I—D CHANNEL SIGNALING BIT INPUTS (PINS 6, 7)

These inputs are 16 kbps serial data inputs. Two bits should be clocked into each of these inputs between the rising edges of the MSI frame reference clock. The first bit of each D channel is clocked into an intermediate buffer on the first falling edge of the DCLK following the rising edge of MSI. The second bit of each D channel is clocked in on the next negative transition of the DCLK. If further DCLK negative edges occur, new information is serially clocked into the buffer replacing the previous data one bit at a time. Buffered D channel data bits are burst to the slave device on the next rising edge of the MSI frame reference clock.

D1O, D2O—D CHANNEL SIGNAL OUTPUTS (PINS 9, 10)

These serial outputs provide the 16 kbps D channel signaling information from the incoming burst. Two data bits should be clocked out of each of these outputs between the rising edges of the MSI frame reference clock. The rising edge of MSI produces the first bit of each D channel on its respective pin. Circuitry then searches for a negative D clock edge. This tells the D channel data shift register to produce the second D channel bit on the next rising edge of the DCLK. Further positive edges of the DCLK recirculate the D channel output buffer information.

DCLK—D CHANNEL CLOCK INPUT (PIN 8)

This input is the transmit and receive data clock for both D channels. D channel input and output operation is described in the D1O, D2O pin description.

Tx—TRANSMIT DATA OUTPUT (PIN 13)

This pin is high impedance when both TE1 and TE2 are low. This pin serves as an output for B channel information received from the slave device. The B channel data is under the control of TE1, TE2, and TDC/RDC. (See TE1, TE2 description.)

Rx—RECEIVE DATA INPUT (PIN 21)

B channel data is input on this pin and is controlled by the RE1, RE2, and TDC/RDC pins. (See RE1, RE2 description.)

TE1, TE2—TRANSMIT DATA ENABLE INPUT (PIN 15)

These two pins control the output of data for their respective B channel on the Tx output pin. When both TE1 and TE2 are low, the Tx pin is high impedance. The rising edge of the respective enable produces the first bit of the selected B channel data on the Tx pin. Internal circuitry then scans for the next negative transition of the TDC/RDC clock. Following this event the next seven bits of the selected B channel data are output on the next seven rising edges of the TDC/RDC data clock. When TE1 and TE2 are high simultaneously, data on the Tx pin is undefined. TE1 and TE2 should be approximately leading-edge aligned with the TDC/RDC data clock signal. In order to keep the Tx pin out of the high-impedance state, these enable lines should be high while the respective B channel data is being output.

RE1, RE2—RECEIVE DATA ENABLE INPUTS (PINS 19, 20)

These inputs control the input of B channel data on the Rx pin of the device. The rising edge of the respective enable signal causes the device to load the selected receive data buffer with data from the Rx pin on the next eight falling edges of the TDC/RDC clock input. The RE1 and RE2 enables should be roughly leading-edge aligned with the TDC/RDC data clock input. These enables are rising edge sensitive and need not be high for the entire B-channel input period.

TDC/RDC—TRANSMIT/RECEIVE DATA CLOCK INPUT (PIN 18)

This input is the transmit and receive data clock for the B channel data. As described in the TE1/TE2 and the RE1/RE2 sections, output data changes state on the rising edge of this signal, and input data is read on the falling edges of this signal. TDC/RDC should be roughly leading-edge aligned with the TE1, TE2, RE1, and RE2 enables, as well as the MSI frame reference signal.

MC145425 SLAVE PIN DESCRIPTIONS

V_{DD}—POSITIVE SUPPLY (PIN 24)

The most positive power supply pin, normally +5 volts with respect to V_{SS}.

V_{SS}—NEGATIVE SUPPLY (PIN 1)

The most negative supply pin and logic ground, normally 0 volts.

V_{ref}—REFERENCE OUTPUT (ANALOG GROUND) (PIN 2)

This pin is the output of the internal reference supply and should be bypassed to V_{DD} and V_{SS} with 0.1 μF capacitors. This pin usually serves as an analog ground reference for transformer coupling of the device's incoming bursts from the line. No external dc load should be placed on this pin.

LI—LINE INPUT (PIN 3)

This pin is an input to the demodulator for the incoming bursts. The input has an internal 240 kΩ resistor tied to the V_{ref} pin, so an external capacitor or line transformer may be used to couple the input signal to the device with no dc offset.

LO1, LO2—LINE DRIVER OUTPUTS (PINS 23, 22)

These push-pull outputs drive the twisted pair transmission line with a 512 kHz modified DPSK (MDPSK) burst each 125 μs; in other words at an 8 kHz frame rate. When not modulating the line, these pins are driven to the active high state—being the same potential, they create an ac short. So when used in conjunction with feed resistors, proper line termination is maintained.

CLK OUT—CLOCK OUTPUT (PIN 19)

This pin serves as a buffered output of the crystal frequency divided by two. This clock is provided for systems using the MC145428 Data Set Interface asynchronous/synchronous terminal adaptor device.

$\overline{LB}$—LOOPBACK CONTROL INPUT (PIN 4)

When this pin is low, the incoming B channels from the master are burst back to the master—instead of the Rx B channel input data. The B channel data from the master continues to be output at the slave's Tx pin during loopback. If the TONE and the loopback function are active simultaneously, the loopback function overrides the TONE function. D channel data is not affected by $\overline{LB}$.

VD—VALID DATA OUTPUT (PIN 5)

A high on this pin indicates that a valid transmission burst has been demodulated. A valid burst is determined by proper synchronization and the absence of detected bit errors. If no transmissions from the master have been received in the last 250 μs, as determined by an internal oscillator, VD will go low.

Mu/$\overline{A}$—TONE FORMAT INPUT (PIN 11)

This pin determines the PCM code for the 500 Hz square wave tone generated when the TONE input is high—Mu law (Mu/$\overline{A}$ = 1) or CCITT A law (Mu/$\overline{A}$ = 0) format.

TONE—TONE ENABLE INPUT (PIN 16)

A high on this pin causes a 500 Hz square wave PCM tone to be inserted in place of the demodulated B channel data on B channel 1. This feature allows the designer to provide audio feedback for telset keyboard operations.

$\overline{PD}$—POWER DOWN INPUT/OUTPUT (PIN 12)

This is a bidirectional pin with a weak output driver so that it can be externally overdriven. When held low, the ISDN UDLT is powered down, and the only active circuitry is that which is necessary for demodulation, generation of EN1, EN2, BCLK, and DCLK, and outputting of the data bits and VD. When held high, the ISDN UDLT is powered up and transmits normally in response to received bursts from the master. If the ISDN UDLT is powered up for 250 μs—which is derived from an internal oscillator and no bursts from the master have occurred, the ISDN slave UDLT generates a free-running set of

EN1, EN2, BCLK, and DCLK signals and sends a burst to the master device every other 125 μs frame. This is a wake-up signal to the master.

When $\overline{PD}$ is floating and a burst from the master is demodulated, the weak output drivers will try to force $\overline{PD}$ high. It will try to force $\overline{PD}$ low if 250 μs have elapsed without a burst from the master being successfully demodulated. This allows the slave device to self power up and down in demand-powered loop systems.

CCI—CRYSTAL INPUT (PIN 17)

Normally, an 8.192 MHz crystal is tied between this pin and the XTL pin. A 10 MΩ resistor between CCI and XTL and 25 pF capacitors from CCI and XTL to V_{SS} are required to ensure stability and start-up. CCI may also be driven with an external 8.192 MHz signal if a crystal is not desired.

3

XTL—CRYSTAL OUTPUT (PIN 18)

This pin is capable of driving one external CMOS input and 15 pF of additional load capacitance.

D1I, D2I—D CHANNEL INPUTS (PINS 6, 7)

These two pins are inputs for the 16 kbps D data channels. The D channel data bits are clocked in serially on the negative edge of the 16 kbps DCLK output pin.

D1O, D2O—D CHANNEL OUTPUTS (PINS 9, 10)

These two pins are outputs for the 16 kbps D data channels. These pins are updated on the rising edges of the slave DCLK output pin.

Tx—TRANSMIT DATA OUTPUT (PIN 13)

This line is an output for the B channel data received from the master. B channel 1 data is output on the first eight cycles of the BCLK output when EN1 is high. B channel 2 data is output on the next eight cycles of the BCLK, when EN2 is high. B channel data bits are clocked out on the rising edge of the BCLK output pin.

DCLK—D CHANNEL CLOCK OUTPUT (PIN 8)

This output is the transmit and receive data clock for both D channels. It starts upon demodulation of a burst from the master device. This signal is rising edge aligned with the EN1 and BCLK signals. After the demodulation of a burst, the DCLK line completes two cycles and then remains low until another burst from the master is demodulated. In this manner synchronization with the master is established and any clock slip between master and slave is absorbed each frame.

Rx—RECEIVE DATA INPUT (PIN 21)

This pin is an input for the B channel data. B channel 1 data is clocked in on the first eight falling edges of the BCLK output following the rising edge of the EN1 output. B channel 2 data is clocked in on the next eight falling edges of the BCLK following the rising edge of the EN2 output.

EN1—B CHANNEL 1 ENABLE OUTPUT (PIN 15)

This line is an 8 kHz enable signal for the input and output of the B channel 1 data. While EN1 is high, B channel 1 data is clocked out on the Tx pin on the first eight rising edges of the BCLK. During this same time B channel 1 input data is clocked in on the Rx pin on the first eight falling edges of the BCLK. The VD pin is also updated on the rising edge of the EN1 signal. EN1 serves as the slave device's 8 kHz frame reference signal.

EN2—B CHANNEL 2 ENABLE OUTPUT (PIN 14)

This pin is the logical inverse of the EN1 output and is used to signal the time slot for the input and output of data for the B channel 2 data.

BCLK—B CHANNEL DATA CLOCK OUTPUT (PIN 20)

This is a standard B series output which provides the data clock for the B channel data. This clock signal is 128 kHz and begins operating upon the successful demodulation of a burst from the master. At this time, EN1 goes high and BCLK starts toggling. BCLK remains active for 16 periods, at the end of which time it remains low until another burst is received from the master. In this manner synchronization between the master and slave is established and any clock slippage is absorbed each frame.

BACKGROUND

The MC145421 and the MC145425 ISDN UDLTs provide an economical means of sending and receiving two B channels (64 kbps each) of voice/data and two D channels (16 kbps each) of signal data in a two wire configuration at distances up to one kilometer. There are two ISDN UDLTs, master and slave. The master UDLT is compatible with existing and evolving PABX architectures. This device transmits 2B + 2D channels of data to the remote slave. At the remote end, the slave device presents a replica of the PBX backplane to the terminal devices.

These devices permit existing digital PBX architectures to remain unchanged and provide enhanced voice/data communication services throughout the PBX service area by simply replacing a subscriber's line card and telset.

All operations occur within the boundaries of an 8 kHz frame (125 μs). In the master, the frame sequence begins on the rising edge of MSI. In the slave, the frame begins after the demodulation of a burst from the master. The slave initializes its timing controls at this point to stay synchronized with the master.

During one 125 μs frame four main activities are performed:

1. Previously buffered 2B + 2D channel data is burst to the other end.
2. New 2B + 2D channel data is accepted for the next frame's transmission.
3. An incoming burst is demodulated and stored.
4. 2B + 2D channel data from the previous demodulated frame is output.

The bursts are 20 bits long, composed of two 8-bit B channels and two 2-bit D channels. Bursts are encoded using a modified DPSK method at 512 kHz. Since a single wire pair is used, half duplex operation is used. A 512 kHz burst is sent from end to end in a ping-pong fashion. This method provides apparent full duplex 160 kbps transmission of data at distances up to one kilometer.

GENERAL

The ISDN UDLT consists of a modulator, a demodulator, intermediate data registers, receive and transmit data registers, and sequencing and control logic. The Rx and Tx buffers interface digitally to the line card backplane signals, while the modulator and demodulator interface to the twisted pair transmission media. Intermediate data registers buffer data between these main components. The ISDN UDLT is intended to operate with a 5 volt power supply and can be driven by CMOS or TTL logic.

MASTER OPERATION

In the master, the rising edge of MSI initiates the 125 μs frame. B channel data is clocked into the Rx registers under control of TDC/RDC, RE1, and RE2. This data is combined with the D channel data clocked in on pins D1I and D2I by the DCLK. The resulting 20 bit packet is stored for the next frame transmission to the slave UDLT.

The burst output to the slave consists of the 2B + 2D data loaded during the previous frame. The burst received from the slave is demodulated and stored for outputting in the following frame.

B channel bits demodulated in the previous frame are output on the Tx pin under control of TDC/RDC, TE1, and TE2. Demodulated D channel bits are output on the D1O and D2O output pins. The indication of a valid burst demodulation is the VD output, which is updated at the start of every frame.

SLAVE OPERATION

In normal slave operation, the main synchronizing event is completion of demodulating a burst from the master UDLT. This action initializes the 125 μs frame boundary of the slave. During the slave frame, B channel data is loaded and stored under control of the BCLK, EN1, and EN2 outputs. D channel data is loaded at D1I and D2I under control of the DCLK output.

The demodulated burst from the master is separated into its D channel and B channel components and output on the D1O, D2O, and Tx pins. The return burst to the master consisting of previously loaded 2B + 2D data is transmitted eight bauds after the completion of demodulation of the master's burst. This provides a period for line transients to diminish.

The start of the slave frame initiates two cycles of the 16 kHz DCLK, and one cycle each of the 8 kHz EN1 and EN2 enables. After completing their cycles, these outputs remain low until another demodulation signals the start of a new slave frame. In this manner, clock slip between the master and slave UDLTs is absorbed each frame.

POWER-DOWN OPERATION

When $\overline{PD}$ is low in the master, the ISDN UDLT is powered down and only that circuitry necessary to demodulate incoming bursts is active. No transmissions to the slave occur during power down. If the master is receiving bursts from the slave, the VD pin will change state upon completion of the demodulation.

When the $\overline{PD}$ input pin is driven high, the master ISDN UDLT is powered up. In this mode, the master bursts to the slave every frame. B and D channel data can be loaded and unloaded and VD is updated on the MSI rising edge.

If no bursts are received by the master, whether powered up or not, the B channel data is unknown and the D channel bits will remain at their last known values.

The $\overline{PD}$ pin on the slave UDLT is bidirectional with a weak output driver that can be overdriven externally. When low—either externally or internally derived, the slave is powered down. No bursts to the master can be transmitted. EN1, EN2, BCLK, and DCLK outputs are inactive during power down except when TONE is high or a burst has been received from the master. B and D channel data can be loaded and unloaded, and VD is updated upon completion of demodulation of an incoming burst from the master. Input B and D channel data is not transmitted until the slave is powered up, in which case the first burst contains the most recently loaded data.

When the $\overline{PD}$ pin is high, the slave is powered up and transmits every frame. The data enables and clocks are output and data can be loaded and unloaded.

TIMEOUT OPERATION

Timeout is an operating state in both the UDLT master and slave devices. This state indicates that no incoming bursts have been demodulated, forcing the VD pin low. An internal counter is incremented for each frame that does not contain an incoming burst. The counter is reset upon demodulating a burst from the far end. Timeout can occur whether the device is powered up or down.

In the master, timeout begins on the rising edge of the third MSI following the last received burst. This is equivalent to two MSI frames. The VD output is forced low during timeout. The B channel output data will be unknown, but the D channel bits will remain at their last values. Successful demodulation of a burst from the slave will result in leaving the timeout state on the next rising MSI edge.

Timeout in the slave begins during the third frame without an incoming burst. The VD pin is forced low and the last D channel bits are saved. Normally, the slave timing is synchronized to the incoming master bursts, but in timeout, the slave operates from a free-running internal frame clock accompanied by BCLK, EN1, and EN2. These clocks are not generated during the two frames prior to entering timeout. If powered up during timeout, the slave will burst to the master on every other frame. This mode allows the terminal equipment to transmit its status to the master even though it is not receiving data. Demodulation of a burst from the master will cause the slave to exit the timeout mode.

When the $\overline{PD}$ pin is used as an output on the slave UDLT, timeout controls the pin. Timeout forces the $\overline{PD}$ output low to indicate that the device has powered itself down. In this case, the slave will not transmit to the master. However, when a valid burst is received, timeout ends and the $\overline{PD}$ pin is driven high to indicate power up. This feature allows the slave UDLT to self-power-up and down in demand-powered loop systems.

NOTE

The slave uses a free running clock during timeout. After a long period without a burst from the master, the timing between master and slave could be such that more than one burst will be needed to resync the two devices.

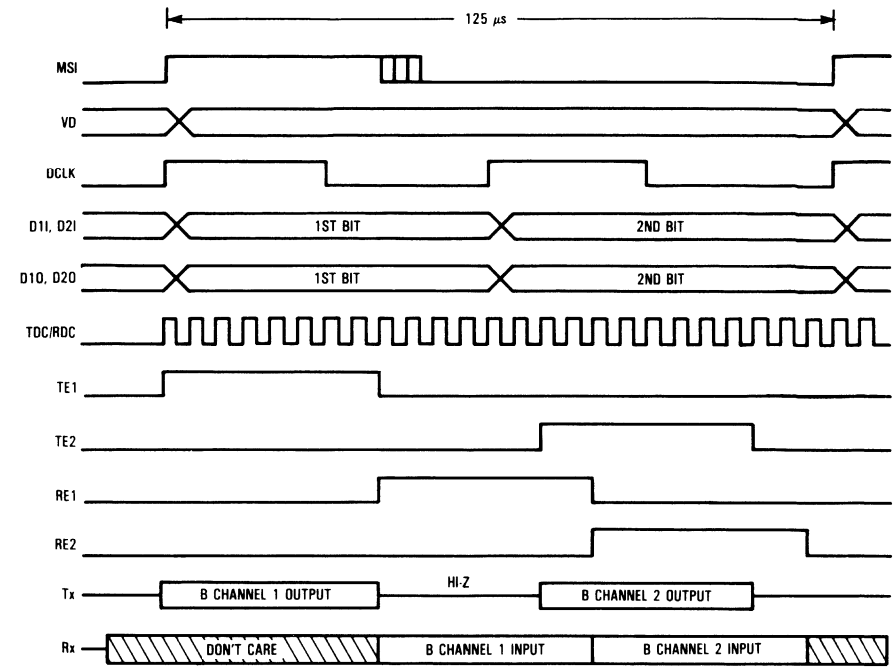


Figure 1. Typical MC145421 Master ISDN UDLT Timing

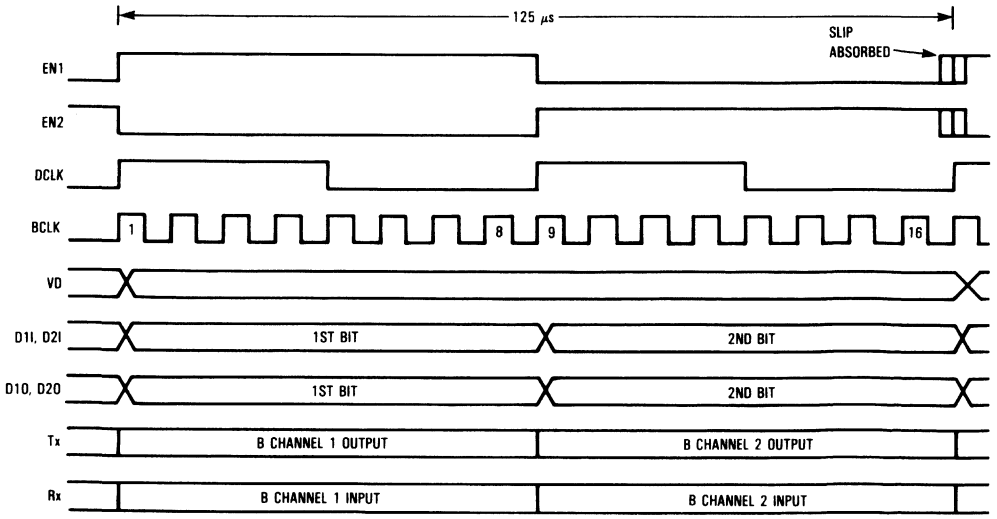
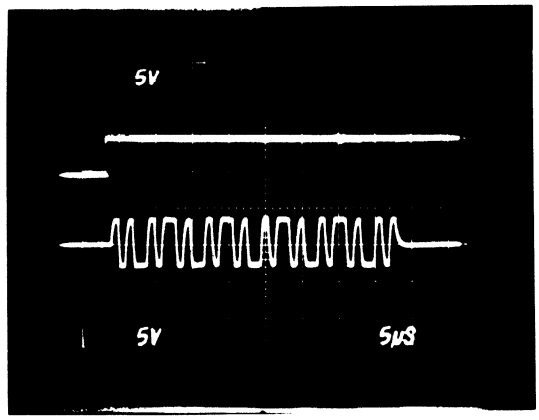
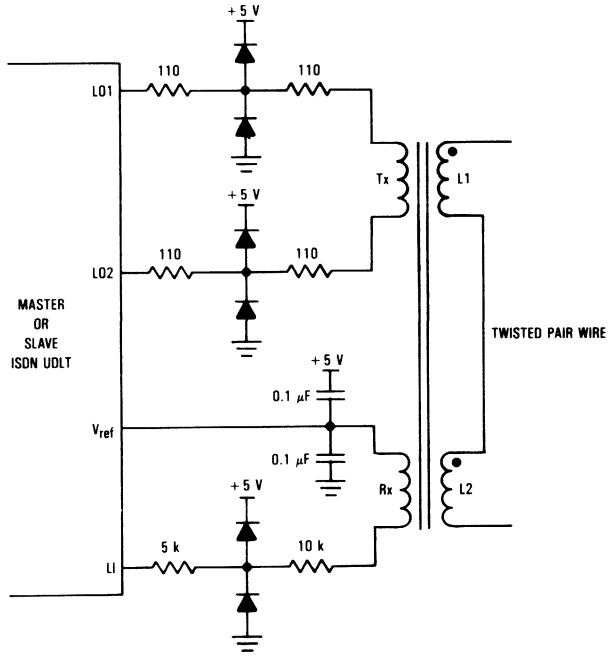


Figure 2. MC145425 Slave ISDN UDLT Timing



Top Trace: MSI
Bottom Trace: Outgoing burst measured at LI (with respect to V_{ref})

Figure 3. Master Burst



TRANSFORMER PARAMETERS

INDUCTANCE OF Tx WINDING: 1.75 mH
TURNS RATIO: Tx: L1 + L2 2:1
TURNS RATIO: Rx: L1 + L2 4:1

DIODES: 1N4148 OR EQUIVALENT

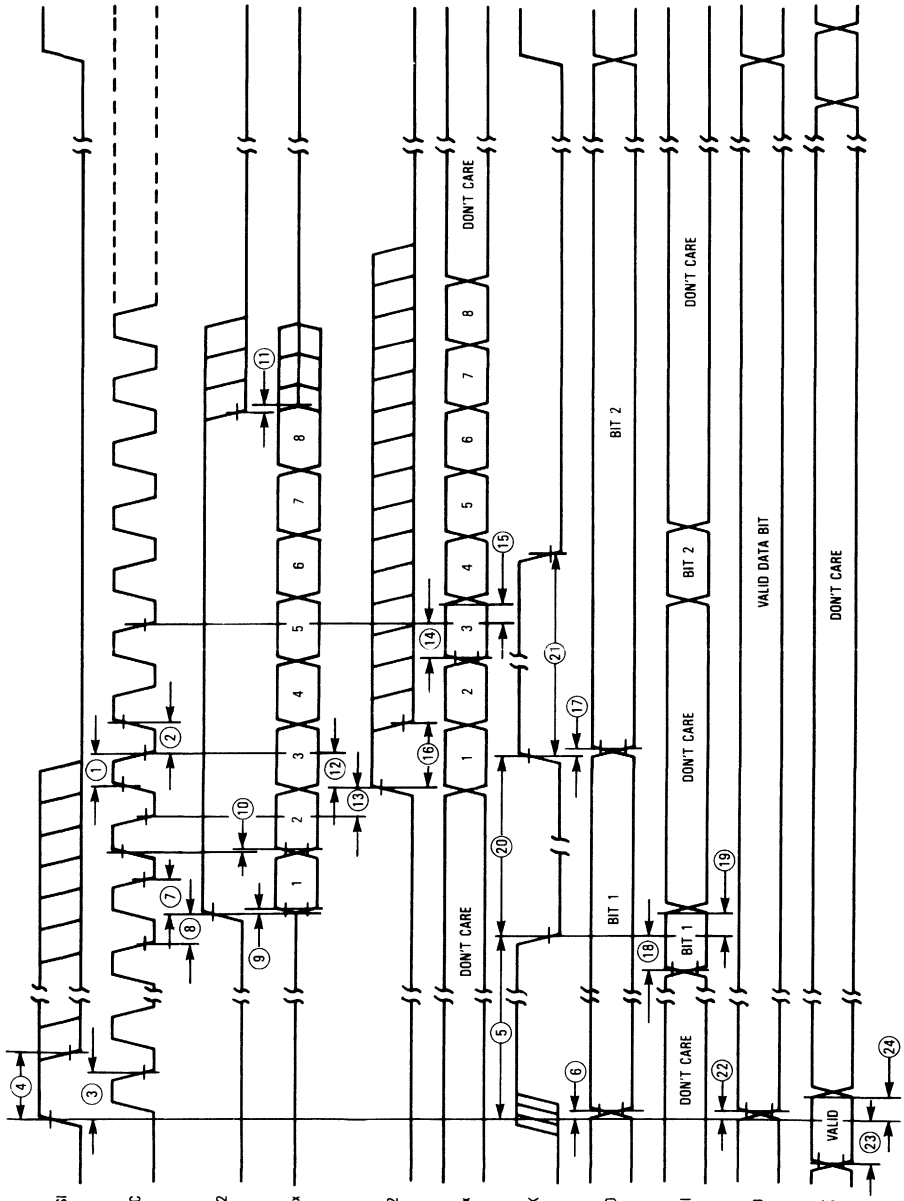
Figure 4. Interface to Twisted Pair Wire

SWITCHING CHARACTERISTICS (V_{DD} = 5 V, T_A = 0 to 70°C)

No.*	Parameter	Min	Max	Unit
Master Timing				
1	TDC/RDC Pulse Width High	110		ns
2	TDC/RDC Pulse Width Low	110		ns
3	MSI Rising Edge to TDC/RDC Falling Edge	90		ns
4	MSI Pulse Width	200		ns
5	MSI Rising Edge to First DCLK Falling Edge	90		ns
6	MSI Rising Edge to First D1O, D2O Bit Valid		–	ns
7	TE1, TE2 Rising Edge to TDC/RDC Falling Edge	110		ns
8	TDC/RDC Falling Edge to TE1, TE2 Rising Edge	20		ns
9	TE1, TE2 Rising Edge to First Tx Data Bit Valid		50	ns
10	TDC/RDC Rising Edge to Tx Data Bits 2 Through 8 Valid		50	ns
11	TE1, TE2 Falling Edge to Tx High-Impedance		70	ns
12	RE1, RE2 Rising Edge to TDC/RDC Falling Edge	110		ns
13	TDC/RDC Falling Edge to RE1, RE2 Rising Edge	20		ns
14	Rx Data Setup (Data Valid Before TDC/RDC Falling Edge)	50		ns
15	Rx Data Hold (Data Valid After TDC/RDC Falling Edge)	20		ns
16	RE1, RE2 Pulse Width	220		ns
17	DCLK Rising Edge to D1O, D2O Bit Valid		–	ns
18	D1I,D2I Data Setup (Data Valid Before DCLK Falling Edge)	50		ns
19	D1I, D2I Data Hold (Data Valid After DCLK Falling Edge)	20		ns
20	DCLK Pulse Width Low	110		ns
21	DCLK Pulse Width High	110		ns
22	MSI Rising Edge to VD Valid		–	ns
23	$\overline{PD}$, $\overline{LB}$ Setup ($\overline{PD}$, $\overline{LB}$ Valid Before MSI Rising Edge)	50		ns
24	$\overline{PD}$, $\overline{LB}$ Hold ($\overline{PD}$, $\overline{LB}$ Valid After MSI Rising Edge)	20		ns
Slave Timing				
25	BCLK Pulse Width High (CCI = 8.192 MHz)	3.66	4.15	µs
26	BCLK Pulse Width Low (CCI = 8.192 MHz)	3.66	4.15	µs
27	EN1 or EN2 Rising Edge to BCLK Rising Edge		±50	ns
28	EN1 or EN2 Rising Edge to DCLK Rising Edge		±50	ns
29	EN1 or EN2 Rising Edge to First Tx Data Bit Valid		50	ns
30	BCLK Rising Edge to Tx Data Bits 2 Through 8 Valid		50	ns
31	DCLK Pulse Width High (CCI = 8.192 MHz)	31.0	31.5	µs
32	DCLK Pulse Width Low (CCI = 8.192 MHz)	31.0	31.5	µs
33	DCLK Rising Edge to D1O, D2O Bits Valid		50	ns
34	Rx Setup (Rx Data Valid Before BCLK Falling Edge)	50		ns
35	Rx Hold (Rx Data Valid After BCLK Falling Edge)	20		ns
36	D1I, D2I Setup (D1I, D2I Valid Before DCLK Falling Edge)	50		ns
37	D1I, D2I Hold (D1I, D2I Valid After DCLK Falling Edge)	20		ns
38	EN1 Rising Edge to VD Valid		50	ns
SE Pin Timing				
39	$\overline{LB}$, $\overline{PD}$ Hold ($\overline{LB}$, $\overline{PD}$ Valid After SE Falling Edge)	20		ns
40	D1O, D2O, VD High-Impedance After SE Falling Edge		70	ns
41	D1O, D2O, VD Valid After SE Rising Edge)	60		ns
42	$\overline{LB}$, $\overline{PD}$ Setup ($\overline{LB}$, $\overline{PD}$ Valid Before SE Rising Edge)	50		ns

*See Switching Characteristics waveforms

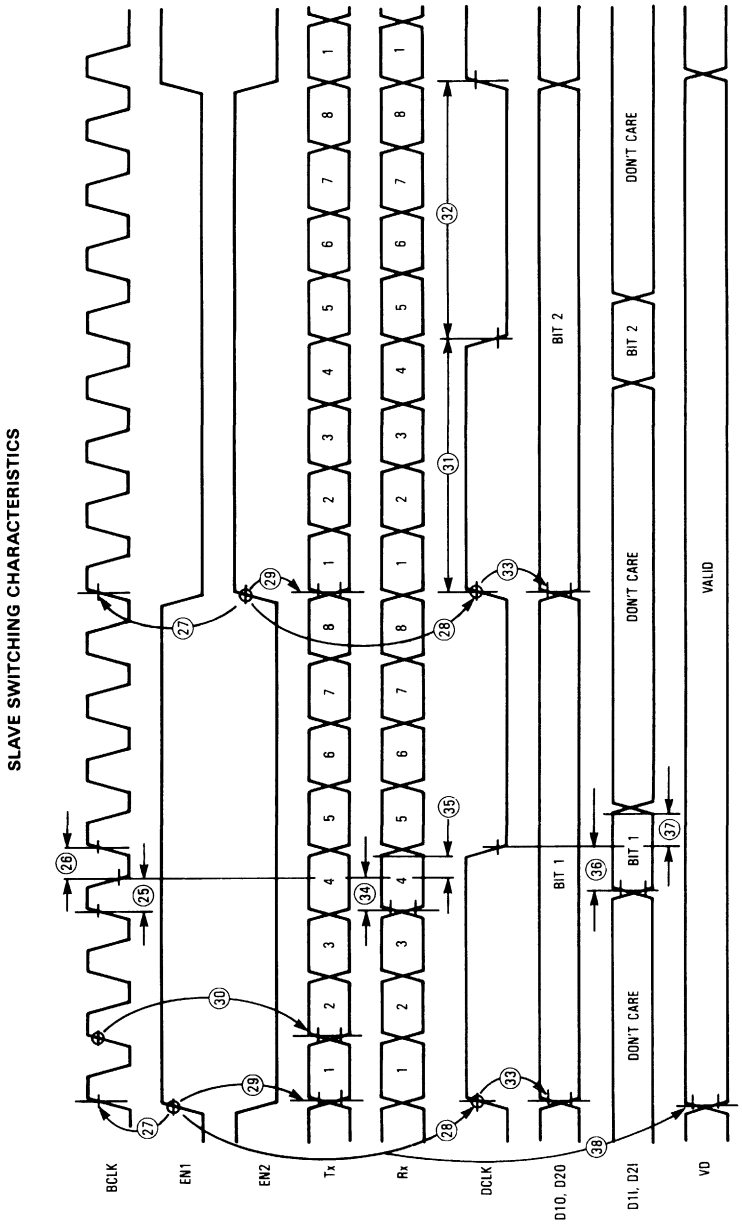
MASTER SWITCHING CHARACTERISTICS



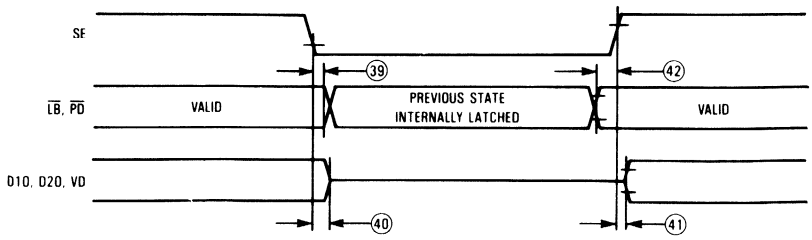
NOTE: All measurement thresholds are 30% or 70% of V_{DD}.

3

SLAVE SWITCHING CHARACTERISTICS



MASTER SE PIN TIMING



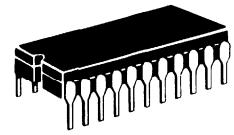
NOTE: All measurement thresholds are 30% or 70% of V_{DD}.

MOTOROLA

MC145422
MC145426

Advance Information

Universal Digital-Loop Transceivers (UDLT)



L SUFFIX
CERAMIC
CASE 736

3

The MC145422 and MC145426 UDLTs are high-speed data transceivers that provide 80 kilobits per second full duplex data communication over 26 AWG and larger twisted pair cable up to two kilometers in distance. Intended primarily for use in digital subscriber voice/data telephone systems, these devices can also be used in remote data acquisition and control systems. These devices utilize a 256 kilobaud modified differential phase shift keying burst modulation technique for transmission to minimize RFI/EMI and crosstalk. Simultaneous power distribution and duplex data communication can be obtained using a single twisted pair wire.

These devices are designed for compatibility with existing, as well as evolving, telephone switching hardware and software architectures.

The UDLT chip-set consists of the MC145422 master UDLT for use at the telephone switch linecard and the MC145426 slave UDLT for use at the remote digital telset and/or data terminal.

The devices employ CMOS technology in order to take advantage of its reliable low-power operation and proven capability for complex analog/digital LSI functions.

- Provides Full Duplex Synchronous 64 Kilobits-Per-Second Voice/Data Channel and Two Eight Kilobits-Per-Second Signaling Data Channels Over One 26 AWG Wire Pair Up to Two Kilometers
- Compatible with Existing and Evolving Telephone Switch Architectures and Call Signaling Schemes
- Automatic Detection Threshold Adjustment for Optimum Performance Over Varying Signal Attenuations
- Protocol Independent
- Single Five Volt Power Supply
- 22 Pin Package

MC145422 Master UDLT

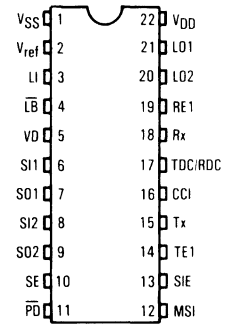
- Pin Controlled Power-Down and Loop-Back Features
- Signaling and Control I/O Capable of Sharing Common Bus Wiring with Other UDLTs
- Variable Data Clock—64 kHz to 2.56 MHz
- Pin Controlled Insertion/Extraction of Eight Kilobits/Second Channel into LSB of 64 Kilobits/Second Channel for Simultaneous Routing of Voice and Data Through PCM Voice Path of Telephone Switch

MC145426 Slave UDLT

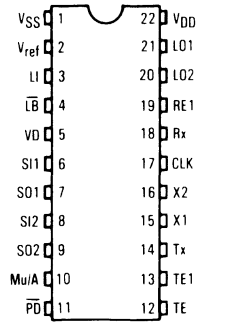
- Compatible with MC14400 Series PCM Mono-Circuits
- Pin Controlled Loop-Back Feature
- Automatic Power-Up/Down Feature
- On-Chip Data Clock Recovery and Generation
- Pin Controlled 500 Hz D3 or CCITT Format PCM Tone Generator for Audible Feedback Applications

PIN ASSIGNMENTS

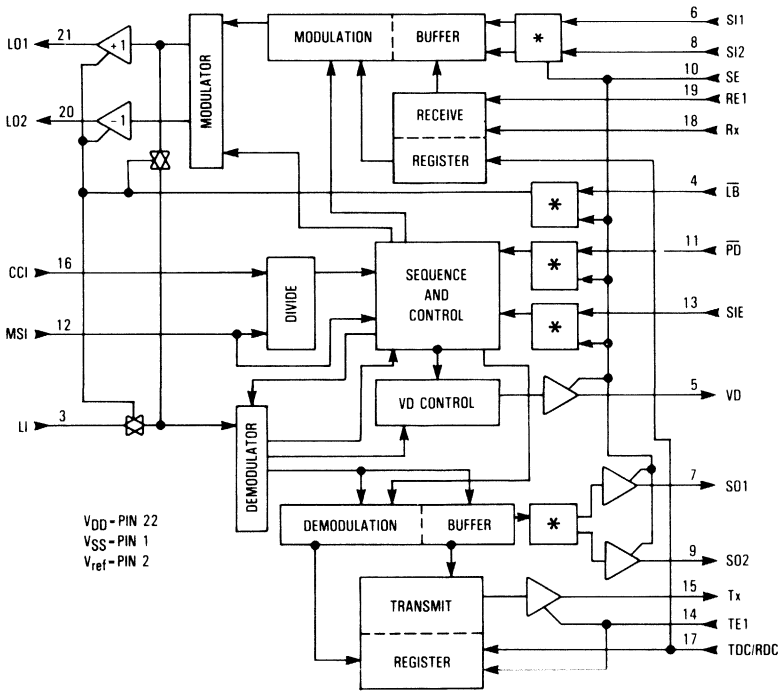
MC145422



MC145426

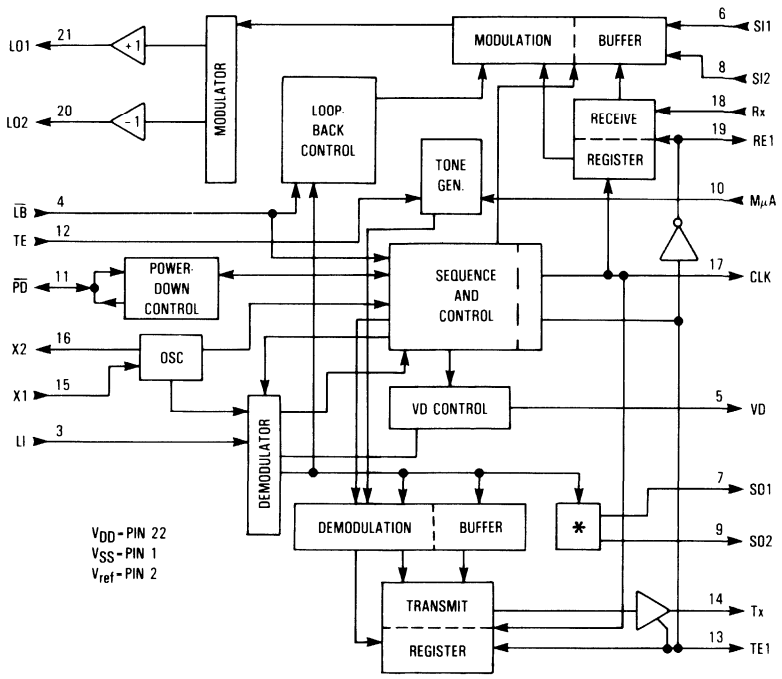


MC145422 MASTER UDLT BLOCK DIAGRAM



* – SE controlled latch

MC145426 SLAVE UDLT BLOCK DIAGRAM



* – Signal Bits Output Latch

ABSOLUTE MAXIMUM RATINGS (Voltage Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}-V_{SS}	−0.5 to 9.0	V
Voltage, Any Pin to V_{SS}	V	−0.5 to V_{DD} + 0.5	V
DC Current, Any Pin (Excluding V_{DD}, V_{SS})	I	±10	mA
Operating Temperature	T_A	−40 to +85	°C
Storage Temperature	T_{stg}	−85 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to 70°C)

Parameter	Pins	Min	Max	Unit
DC Supply Voltage	V_{DD}	4.5	5.5	V
Power Dissipation (PD = V_{DD}, V_{DD} = 5 V)	V_{DD}	–	80	mW
Power Dissipation (PD = V_{SS}, TE = V_{SS})	V_{DD}	–	75	mW
Frame Rate MC145422	MSI	7.9	8.1	kHz
MC145422-MC145426 Frame Rate Slip (See Note 1)	–	–	0.25	%
CCI Clock Frequency (MSI = 8 kHz)	CCI	–	2.048	MHz
Data Clock Rate MC145422	TDC, RDC	64	2560	kHz
Modulation Baud Rate (See Note 2)	LO1, LO2	–	256	kHz

NOTES: 1. The MC145426 crystal frequency divided by 512 must equal the MC145422 MSI frequency ±0.25% for optimum operation.
2. Assumes crystal frequency of 4.096 MHz for the MC145426 and 2.048 MHz CCI for the MC145422.

DIGITAL CHARACTERISTICS (V_{DD} = 5 V, T_A = 0 to 70°C)

Parameter		Min	Max	Unit
Input High Level		3.5	–	V
Input Low Level		–	1.5	V
Input Current	Except LI	−1.0	1.0	μA
	LI	−100	100	
Input Capacitance		–	7.5	pF
Output High Current (Except Tx on MC145422	V_{OH} = 2.5 V	−1.7	–	mA
and Tx and $\overline{PD}$ on MC145426)	V_{OH} = 4.6 V	−0.36	–	
Output Low Current (Except Tx on MC145422	V_{OL} = 0.4 V	0.36	–	mA
and Tx and $\overline{PD}$ on MC145426)	V_{OL} = 0.8 V	0.8	–	
$\overline{PD}$ Output High Current (MC145426)	V_{OH} = 2.5 V	−90	–	μA
(See Note 7)	V_{OH} = 4.6 V	−10	–	
$\overline{PD}$ Output Low Current (MC145426)	V_{OL} = 0.4 V	60	–	μA
(See Note 7)	V_{OL} = 0.8 V	100	–	
Tx Output High Current	V_{OH} = 2.5 V	−3.4	–	mA
	V_{OH} = 4.6 V	−0.7	–	
Tx Output Low Current	V_{OL} = 0.4 V	1.7	–	mA
	V_{OL} = 0.8 V	3.5	–	
Tx Input Impedance (TE1 = V_{SS}, MC145422)		100	–	kΩ
Crystal Frequency (MC145426, Note 3)		4.0	4.4	MHz
PCM Tone (TE = V_{DD}, MC145426)		−22	−18	dBm0
Three-State Current (SO1, SO2, VD, Tx on MC145422, Tx on MC145426)		–	±1	μA
V_{ref} Voltage (See Note 6)		2	3	V
X2 – Oscillator Output High Drive Current (MC145426) (See Note 5)	V_{OH} = 4.6 V	−450	–	μA
X2 – Oscillator Output Low Drive Current (MC145426) (See Note 5)	V_{OL} = 0.4 V	450	–	μA

ANALOG CHARACTERISTICS (V_{DD} = 5 V, T_A = 0 to 70°C)

Parameter		Min	Max	Unit
Modulation Differential Amplitude (R_L = 440 Ω)	LO1 to LO2	4.5	6.0	V_{p-p}
Modulation Differential DC Offset		0	300	mV
Demodulator Input Amplitude (See Note 4)		0.050	2.5	V peak
Demodulator Input Impedance		50	150	kΩ

NOTES:
3. The MC145426 crystal frequency divided by 512 must equal the MC145422 MSI frequency ±0.25% for optimum performance.
4. The input level into the demodulator to reliably demodulate incoming bursts. Input referenced to V_{ref}.
5. Output drive when X1 is being driven from an external clock.
6. V_{ref} typically (9/20 V_{DD}-V_{SS})
7. To overdrive $\overline{PD}$ from a low level to 3.5 V or a high level to 1.5 V requires a minimum of ±800 μA drive capability.

3

MC145422 SWITCHING CHARACTERISTICS (V_{DD} = 5 V, T_A = 25°C, C_L = 50 pF)

Parameter		Fig	Symbol	Min	Max	Unit
Input Rise Time	All Digital Inputs	1	t_r	–	4	μs
Input Fall Time	All Digital Inputs	1	t_f	–	4	μs
Pulse Width	TDC/RDC, RE1, MSI	1	$t_{w(H,L)}$	90	–	ns
CCI Duty Cycle		1	$t_{w(H,L)}$	45	55	%
Data Clock Frequency	TDC/RDC	–	t_{DC}	64	2560	kHz
Propagation Delay Time						ns
MSI to SO1, SO2, VD ($\overline{PD}$ = V_{DD})		2	t_{PLH}, t_{PHL}	–	90	
TDC to Tx		3		–	90	
MSI to TDC/RDC Setup Time			t_{su3}	90	–	ns
		4	t_{su4}	40	–	
TE1/RE1 to TDC/RDC Setup Time			t_{su3}	90	–	ns
		4	t_{su4}	40	–	
Rx to TDC/RDC Setup Time		5	t_{su5}	60	–	ns
Rx to TDC/RDC Hold Time		5	t_{h1}	60	–	ns
SI1, SI2 to MSI Setup Time		6	t_{su6}	60	–	ns
SI1, SI2 to MSI Hold Time		6	t_{h2}	60	–	ns

MC145426 SWITCHING CHARACTERISTICS (V_{DD} = 5 V, T_A = 25°C, C_L = 50 pF)

Parameter		Fig	Symbol	Min	Max	Unit
Input Rise Time	All Digital Inputs	1	t_r	–	4	μs
Input Fall Time	All Digital Inputs	1	t_f	–	4	μs
Clock Output Pulse Width	CLK	1	$t_{w(H,L)}$	3.8	4.0	μs
Crystal Frequency		–	f_{X1}	4.086	4.1	MHz
Propagation Delay Times						ns
TE1 Rising to CLK (TE = V_{DD})		7	t_{P1}	50	50	
TE1 Rising to CLK (TE = V_{SS})		7	t_{P1}	438	538	
CLK to TE1 Falling		7	t_{P2}	–	40	
CLK to RE1 Rising		8	t_{P3}	–	40	
RE1 Falling to CLK (TE = V_{DD})		8	t_{P4}	−50	50	
RE1 Falling to CLK (TE = V_{SS})		8	t_{P4}	438	538	
CLK to Tx		9	t_{P5}	–	90	
TE1 to SO1, SO2		9	t_{P6}	–	90	
Rx to CLK Setup Time		5	t_{su5}	60	–	ns
Rx to CLK Hold Time		5	t_{h1}	60	–	ns
SI1, SI2 to TE1 Setup Time		6	t_{su6}	60	–	ns
SI1, SI2 to TE1 Hold Time		6	t_{h2}	60	–	ns

SWITCHING WAVEFORMS

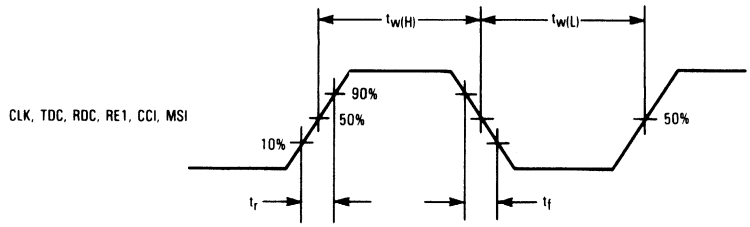


Figure 1

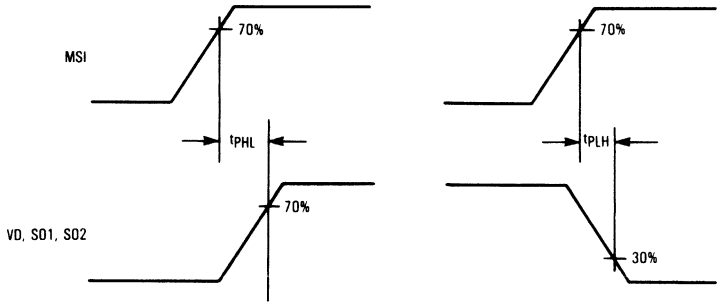


Figure 2

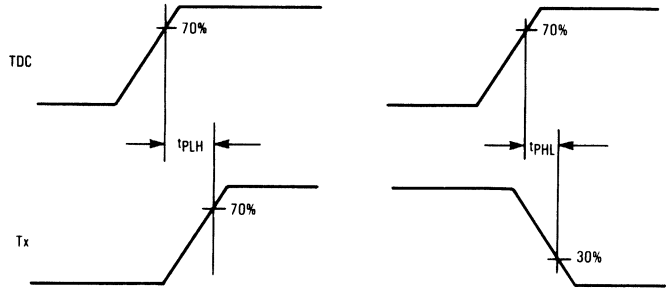


Figure 3

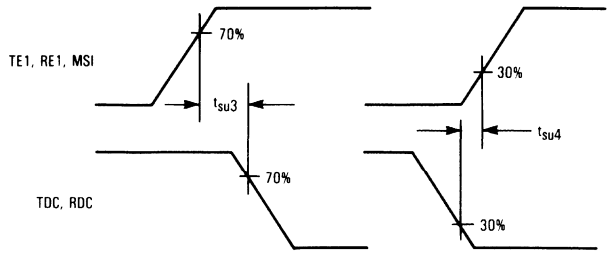


Figure 4

3

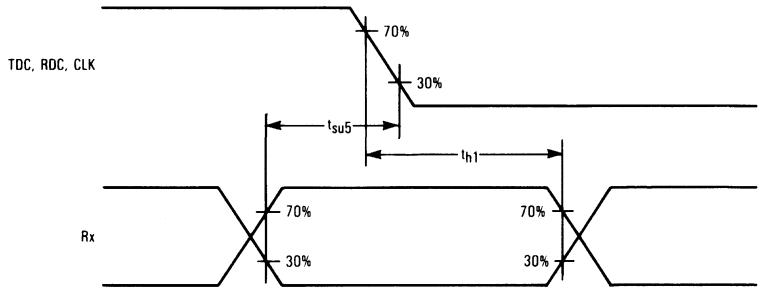


Figure 5

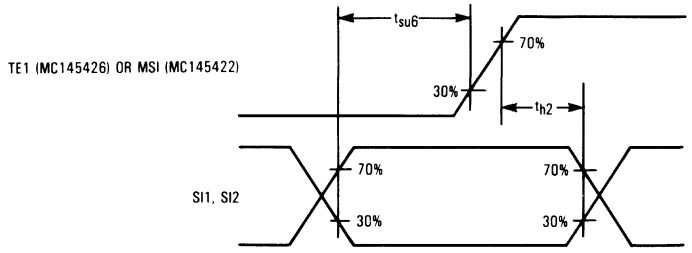


Figure 6

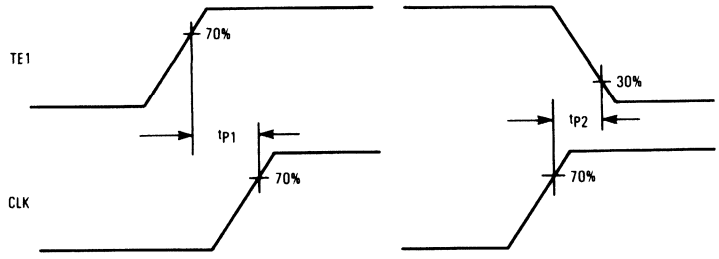


Figure 7

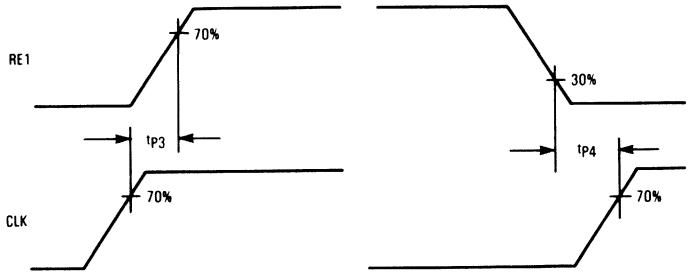


Figure 8

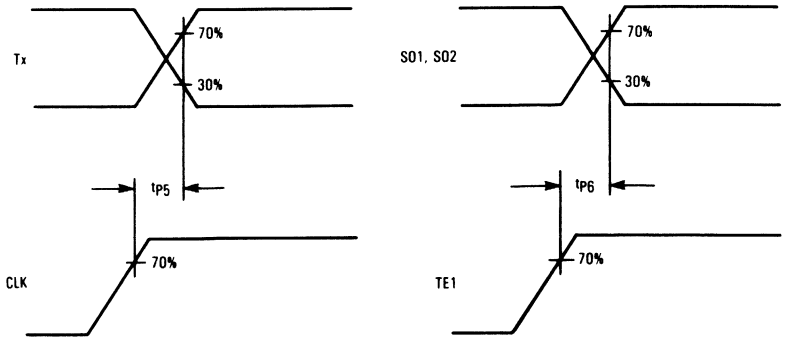


Figure 9

MC145422 MASTER UDLT PIN DESCRIPTIONS

V_{DD} – POSITIVE SUPPLY

Normally 5 volts.

V_{SS} – NEGATIVE SUPPLY

This pin is the most negative supply pin, normally 0 volts.

V_{ref} – REFERENCE OUTPUT

This pin is the output of the internal reference supply and should be bypassed to V_{DD} and V_{SS} by 0.1 μF capacitors. No external dc load should be placed on this pin.

3

LI – LINE INPUT

This input to the demodulator circuit has an internal 100 k resistor tied to the internal reference node so that an external capacitor and/or line transformer may be used to couple the input signal to the part with no dc offset.

$\overline{LB}$ – LOOP-BACK CONTROL

A low on this pin disconnects the LI pin from internal circuitry, drives LO1, LO2 to V_{ref} and internally ties the modulator output to the demodulator input which loops the part on itself for testing in the system. The state of this pin is internally latched if the SE pin is brought and held low. Loop-Back is active only when $\overline{PD}$ is high.

VD – VALID DATA OUTPUT

A high on this pin indicates that a valid line transmission has been demodulated. A valid transmission is determined by proper sync and the absence of detected bit errors. VD changes state on the leading edge of MSI when $\overline{PD}$ is high. When $\overline{PD}$ is low, VD changes state at the end of demodulation of a line transmission. VD is a standard B-series CMOS output and is high impedance when SE is held low.

SI1, SI2 – SIGNALING BIT INPUTS

Data on these pins is loaded on the rising edge of MSI for transmission to the slave. The state of these pins is internally latched if SE is held low.

SO1, SO2 – SIGNALING BIT OUTPUTS

These outputs are received signaling bits from the slave UDLT and change state on the rising edge of MSI if $\overline{PD}$ is high, or at the completion of demodulation if $\overline{PD}$ is low. These outputs have standard B-series CMOS drive capability and are high impedance if the SE pin is held low.

SE – SIGNAL ENABLE INPUT

If held high, the $\overline{PD}$, $\overline{LB}$, SI1, SI2, and SIE inputs and the SO1, SO2, and VD outputs function normally. If held low, the state of these inputs are latched and held internally while the outputs are high impedance. This allows these pins to be bussed with those of other UDLTs to a common controller.

$\overline{PD}$ – POWER-DOWN INPUT

If held low, the UDLT ceases modulation. In power-down, the only active circuitry is that which is necessary to demodulate an incoming burst and output the signal and valid data bits. Internal data transfers to the transmit and receive registers cease. When brought high, the UDLT powers-up, and waits three positive MSI edges or until the end of an incoming transmission from the slave UDLT and begins transmitting every MSI period to the slave UDLT on the next rising edge of the MSI.

MSI – MASTER SYNC INPUT

This pin is the system sync and initiates the modulation on the twisted pair. MSI should be approximately leading-edge aligned with TDC/RDC.

SIE – SIGNAL INSERT ENABLE

This pin, when held high, inserts signal bit 2 received from the slave into the LSB of the outgoing PCM word at Tx and will ignore the SI2 pin and use in place the LSB of the incoming PCM word at Rx for transmission to the slave. The PCM word to the slave will have LSB forced low in this mode. In this manner, signal bit 2 to/from the slave UDLT is inserted into the PCM words the master sends and receives from the backplane for routing through the PABX for simultaneous voice/data communication. The state of this pin is internally latched if the SE pin is brought and held low.

TE1 – TRANSMIT DATA ENABLE 1 INPUT

This pin controls the outputting of data on the Tx pin. While TE1 is high, the Tx data is presented on the eight rising edges of TDC/RDC. TE1 is also a high-impedance control of the Tx pin. If MSI occurs during this period, new data will be transferred to the Tx output register in the ninth high period of TDC/RDC after TE1 rises; otherwise, it will transfer on the rising edge of MSI. TE1 and TDC/RDC should be approximately leading-edge aligned.

Tx – TRANSMIT DATA OUTPUT

This three-state output pin presents new voice data during the high periods of TDC/RDC when TE1 is high (see TE1).

CCI – CONVERT CLOCK INPUT

A 2.048 MHz clock signal should be applied to this pin. The signal is used for internal sequencing and control. This signal should be coherent with MSI for optimum performance but may be asynchronous if slightly worse error rate performance can be tolerated.

TDC/RDC – TRANSMIT/RECEIVE DATA CLOCK

This pin is the transmit and receive data clock and can be 64 kHz to 2.56 MHz. Data is output at the Tx pin while TE1 is high on the eight rising edges of TDC/RDC after the rising edge of TE1. Data on the Rx pin is loaded into the receive register of the UDLT on the eight falling edges of TDC/RDC after a positive transition on RE1. This clock should be approximately leading-edge aligned with MSI.

Rx—RECEIVE DATA

Voice data is clocked into the UDLT from this pin on the falling edges of TDC/RDC under the control of RE1.

RE1—RECEIVE DATA ENABLE 1 INPUT

A rising edge on this pin will enable data on the Rx pin to be loaded into the receive data register on the next eight falling edges of the data clock, TDC/RDC. RE1 and TDC/RDC should be approximately leading-edge aligned.

LO1, LO2—LINE DRIVER OUTPUTS

These outputs drive the twisted pair line with 256 kHz modified DPSK bursts each frame and are push-pull. These pins are driven to V_{ref} when not modulating the line.

MC145426 SLAVE UDLT PIN DESCRIPTIONS

V_{DD}—POSITIVE SUPPLY

Normally 5 volts.

V_{SS}—NEGATIVE SUPPLY

This pin is the most negative supply pin, normally 0 volts.

V_{ref}—REFERENCE OUTPUT

This pin is the output of the internal reference supply and should be bypassed to V_{DD} and V_{SS} by 0.1 μF capacitors. No external dc load should be placed on this pin.

LI—LINE INPUT

This input to the demodulator circuit has an internal 100 kilohm resistor tied to the internal reference node (V_{ref}) so that an external capacitor and/or line transformer may be used to couple the signal to this part with no dc offset.

$\overline{LB}$—LOOP-BACK CONTROL

When this pin is held low and $\overline{PD}$ is high (the UDLT is receiving transmissions from the master), the UDLT will use the eight bits of demodulated PCM data in place of the eight bits of Rx data in the return burst to the master, thereby looping the part back on itself for system testing. SI1 and SI2 operate normally in this mode. CLK will be held low during loop-back operation.

VD—VALID DATA OUTPUT

A high on this pin indicates that a valid line transmission has been demodulated. A valid transmission is determined by proper sync and the absence of detected bit errors. VD changes state on the leading edge of TE1. If no transmissions from the master have been received in the last 250 μs (derived from the internal oscillator), VD will go low without TE1 rising since TE1 is not generated in the absence of received transmissions from the master (see TE pin description for the one exception to this).

SI1, SI2—SIGNALING BIT INPUTS

Data on these pins is loaded on the rising edge of TE1 for transmission to the master. If no transmissions from the master are being received and $\overline{PD}$ is high, data on these pins will be loaded into the part on an internal signal. Therefore, data on these pins should be steady until synchronous communication with the master has been established, as indicated by the high on VD.

SO1, SO2—SIGNALING BIT OUTPUTS

These outputs are received signaling bits from the master UDLT and change state on the rising edge of TE1. These outputs have standard B-series CMOS output drive capability.

$\overline{PD}$—POWER-DOWN INPUT/OUTPUT

This is a bidirectional pin with weak output drivers such that it can be overdriven externally. When held low, the UDLT is powered down and the only active circuitry is: that which is necessary for demodulation, TE1/RE1/CLK generation upon demodulation the outputting of data received from the master and updating of VD status. When held high, the UDLT is powered-up and transmits in response to received transmissions from the master. If no received bursts from the master have occurred when powered-up, for 250 μs (derived from the internal oscillator frequency), the UDLT will generate a free running 125 μs internal clock from the internal oscillator and will burst a transmission to the master every other internal 125 μs clock using data on the SI1 and SI2 pins and the last data word loaded into the receive register. The weak output drivers will try to force $\overline{PD}$ high when a transmission from the master is demodulated and will try to force it low if 250 μs have passed without a transmission from the master. This allows the slave UDLT to self power-up and down in demand powered loop systems.

TE—TONE ENABLE

A high on this pin generates a 500 Hz square wave PCM tone and inserts it in place of the demodulated voice PCM word from the master for outputting to the Tx pin to the telset mono-circuit. A high on TE will generate TE1 and CLK from the internal oscillator when the slave is not receiving bursts from the master so that the PCM square wave can be loaded into the mono-circuit. This feature allows the user to provide audio feedback for the telset keyboard depressions except during Loop-Back. During Loop-Back of the slave UDLT, CLK is defeated so a tone cannot be generated in this mode.

TE1—TRANSMIT DATA ENABLE 1 OUTPUT

This is a standard B-series CMOS output which goes high after the completion of demodulation of an incoming transmission from the master. It remains high for eight CLK periods and then low until the next burst from the master is demodulated. While high, the voice data just demodulated is output on the first eight rising edges of CLK at the Tx pin. The signaling data just demodulated is output on SO1 and SO2 on TE1's rising edge, as is VD.

Tx—TRANSMIT DATA OUTPUT

This is a standard B-series CMOS output. Voice data is output on this pin on the rising edges of CLK while TE1 is high and is high impedance when TE1 is low.

X1—CRYSTAL INPUT

A 4.096 MHz crystal is tied between this pin and X2. A 10 megohm resistor across X1 and X2 and 25 pF capacitors from X1 and X2 to V_{SS} are required for stability and to insure start-up. X1 may be driven by an external CMOS clock signal if X2 is left open.

X2-CRYSTAL OUPUT

This pin is capable of driving one external CMOS input and 15 pF of additional capacitance. (SEE X1)

CLK—CLOCK OUTPUT

This is a standard B-series CMOS output which provides the data clock for the telset mono-circuit. It is generated by dividing the oscillator down to 128 kHz and starts upon the completion of demodulation of an incoming burst from the master. At this time, CLK begins and TE1 goes high. CLK will remain active for 16 periods, at the end of which it will remain low until another transmission from the master is demodulated. In this manner, sync from the master is established in the slave and any clock slip between the master and the slave is absorbed each frame. CLK is generated in response to an incoming burst from the master; however, if TE is brought high, then CLK and TE1/RE1 are generated from the internal oscillator until TE is brought low or an incoming burst from the master is received. CLK is disabled when $\overline{LB}$ is held low.

Rx—RECEIVE DATA INPUT

Voice data from the telset mono-circuit is input on this pin on the first eight falling edges of CLK after RE1 goes high.

Mu/A—TONE DIGITAL FORMAT INPUT

This pin determines if the PCM code of the 500 Hz square wave tone, generated when TE is high, is D3 (Mu/A = 1) or CCITT (Mu/A = 0) format.

RE1-RECEIVE DATA ENABLE 1 OUTPUT

This is a standard B-series CMOS output which is the inverse of TE1 (see TE1).

LO1, LO2—LINE DRIVER OUTPUTS

These outputs drive the twisted pair line with 256 kHz modified DPSK bursts each frame and are push-pull. These pins are driven to V_{ref} when the device is not modulating.

BACKGROUND

The MC145422 master and MC145426 slave UDLT transceiver ICs main application is to bidirectionally transmit the digital signals present at a codec/filter-digital PABX backplane interface over normal telephone wire pairs. This allows the remoting of the mono-circuit in a digital telephone set and enables each set to have a high speed data access to the PABX switching facility. In effect, the UDLT allows each PABX subscriber direct access to the inherent sixty-four kilobits per second data routing capabilities of the PABX.

The UDLT provides a means for transmitting and receiving sixty-four kilobits of voice data and sixteen kilobits-per-second of signaling data in two wire format over normal telephone pairs. The UDLT is a two chip set consisting of a master and a slave. The master UDLT replaces the codec/filter and SLIC on the PABX line card, and transmits and receives data over the wire pair to the telset. The UDLT appears to the linecard and backplane as if it were a PCM codec/filter and has almost the same digital interface features as the MC14400 series mono-circuits. The slave UDLT is located in the telset and interfaces the mono-circuit to the wire pair. By hooking two UDLTs back-to-back, a repeater can also be formed. The master and slave UDLTs operate in a frame synchronous manner, sync being established at the slave by the timing of the master's transmission. The master's sync is derived from the PABX frame sync.

The UDLT operates using one twisted pair. Eight bits of voice data and two bits of signaling data are transmitted and received each frame in a half duplex manner; i.e., the slave waits until the transmission from the master is completely received before transmitting back to the master. Transmission occurs at 256 kilohertz bit rate using a modified form of DPSK. This "ping-pong" mode will allow transmission of data at distances up to two kilometers before turnaround delay becomes a problem. The UDLT is so defined as to allow this data to be handled by the linecard, backplane, and PABX as if it were just another voice conversation. This allows existing PABX hardware and software to be unchanged and yet provides switched sixty-four kilobits per second voice or data communications throughout its service area by simply replacing a subscriber's linecard and telset. A feature in the master allows one of the two signaling bits to be inserted and extracted from the backplane PCM word to allow simultaneous voice and data transmission through the PABX. Both UDLTs have a loop-back feature by which the device can be tested in the user system.

The slave UDLT has the additional feature of providing a 500 hertz Mu or A-law coded square wave to the mono-circuit when the TE pin is brought high. This can be used to provide audio feedback in the telset during keyboard depressions.

CIRCUIT DESCRIPTION

GENERAL

The UDLT consists of a modulator, demodulator, two intermediate data buffers, sequencing and control logic, and transmit and receive data registers. The data registers interface to the linecard or mono-circuit digital interface signals, the modulator and demodulator interface the twisted pair transmission medium, while the intermediate data registers buffer data between these two sections. The UDLT is intended to operate on a single five volt supply and can be driven by TTL or CMOS logic.

MASTER OPERATION

In the master, data from the linecard is loaded into the receive register each frame from the Rx pin under the control of the TDC/RDC clock and the receive data enable, RE1. RE1 controls loading of eight serial bits, henceforth referred to as the voice data word. Each MSI, these words are transferred out of the receive register to the modulation buffer for subsequent modulation onto the line. The modulation buffer takes the received voice data word and the two signaling data input bits on SI1 and SI2 loaded on the MSI transition and formats the ten bits into a specific order. This data field is then transmitted in a 256 kilohertz modified DPSK burst onto the line to the remote slave UDLT.

Upon demodulating the return burst from the slave, the decoded data is transferred to the demodulation buffer and the signaling bits are stripped ready to be output on SO1 and SO2 at the next MSI. The voice data word is loaded into the transmit register as described in the TE1 pin description for outputting via the Tx pin at the TDC/RDC data clock rate under the control of TE1. VD is output on the rising edge of MSI. Timing diagrams for the master are shown in Figure 10.

SLAVE OPERATION

In the slave, the synchronizing event is the detection of an incoming line transmission from the master as indicated by the completion of demodulation. When an incoming burst from the master is demodulated, several events occur. As in the master, data is transferred from the demodulator to the demodulation buffer and the signaling bits are stripped for outputting at SO1 and SO2. Data in the receive register is transferred to the modulation buffer. TE1 goes high loading in data at SI1 and SI2, which will be used in the transmission burst to the master along with the data in the transmit data buffer, and outputting SO1, SO2, and VD. Modulation of the burst begins four 256 kilohertz periods after the completion of demodulation.

While TE1 is high, voice data is output on Tx to the telset mono-circuit on the rising edges of the data clock output on the CLK pin. On the ninth rising edge of CLK, TE1 goes low, RE1 goes high, and voice data from the mono-circuit is input to the receive register from the Rx pin on the next eight falling edges of CLK. RE1 is TE1 inverted and is provided to facilitate interface to the mono-circuit.

The CLK pin 128 kilohertz output is formed by dividing down the 4.096 megahertz crystal frequency by thirty-two. Slippage between the frame rate of the master (as represented by the completion of demodulation of an incoming transmission from the master) and the crystal frequency is absorbed by holding the sixteenth low period of CLK until the next completion of demodulation. This is shown in the slave UDLT timing diagram of Figure 11.

POWER-DOWN OPERATION

In the master, when $\overline{PD}$ is low, the UDLT stops modulating and only that circuitry necessary to demodulate the incoming bursts and output the signaling and VD data bits is active. In this mode, if the UDLT receives a burst from the slave, the SO1, SO2, and VD pins will change state upon completion of the demodulation instead of the rising edge of MSI. The state of these pins will not change until either three rising MSI edges have occurred without the reception of a burst from the slave or until another burst is demodulated, whichever occurs first.

When $\overline{PD}$ is brought high, the master UDLT will wait either three rising MSI edges or until the MSI rising edge following the demodulation of an incoming burst before transmitting to the slave. The data for the first transmission to the slave after power−up is loaded into the UDLT during the RE1 period prior to the burst in the case of voice, and on the present rising edge of MSI for signaling data.

In the slave, $\overline{PD}$ is a bidirectional pin with weak output drivers such that it can be overdriven externally. When held low, the UDLT slave is powered−down and only that circuitry necessary for demodulation, TE1/RE1/CLK generation upon demodulation, and the outputting of voice and signaling bits is active. When held high, the UDLT slave is powered-up and transmits normally in response to received transmissions from the master. If no bursts have been received from the master within 250 μs after power-up (derived from the internal oscillator frequency), the UDLT generates an internal 125 μs free-running clock from the internal oscillator. The slave UDLT then bursts a transmission to the master UDLT every other 125 μs clock period using data loaded into the Rx pin during the last RE1 period and SI1, SI2 data loaded in on the internal 125 μs clock edge. The weak output drivers will try to force $\overline{PD}$ high when a transmission from the master is demodulated and will try to force it low if 250 μs have passed without a transmission from the master. This allows the slave UDLT to self power-up and down in demand powered-loop systems.

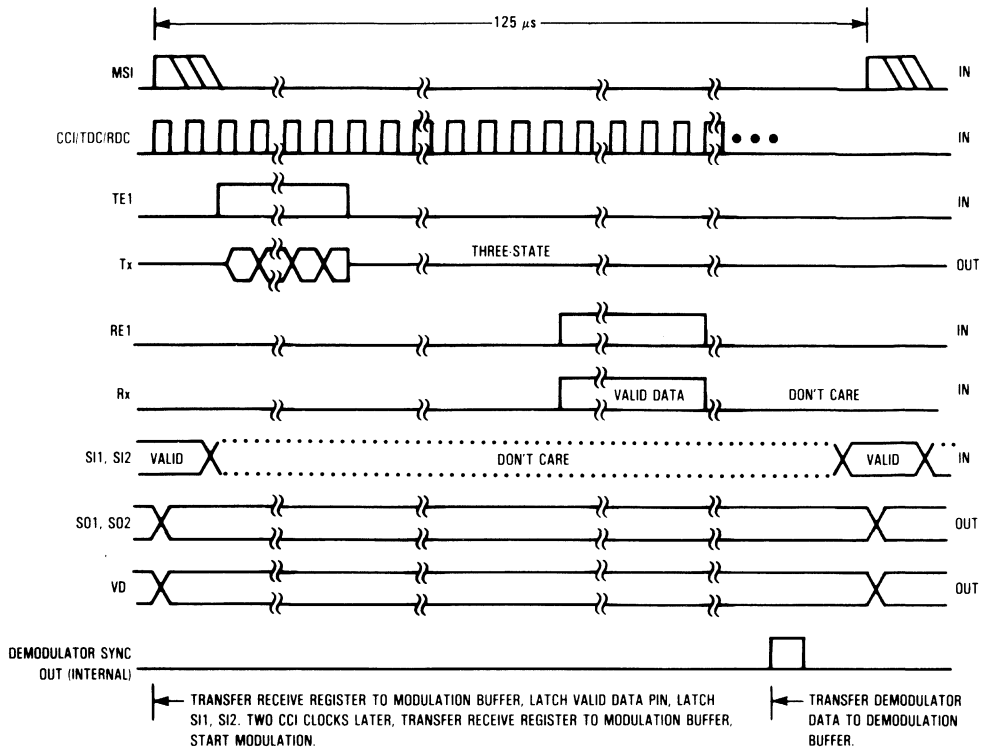
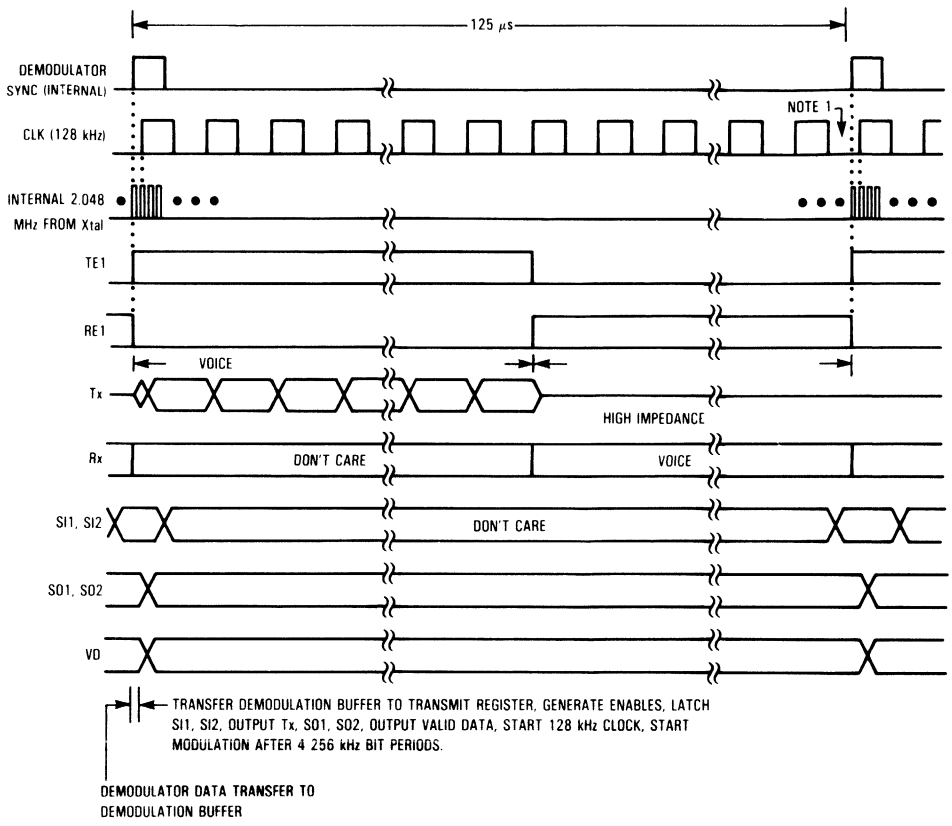


Figure 10. Master UDLT Timing



NOTE:
1. Slip between master and slave is taken up in this period.

Figure 11. Slave UDLT Timing

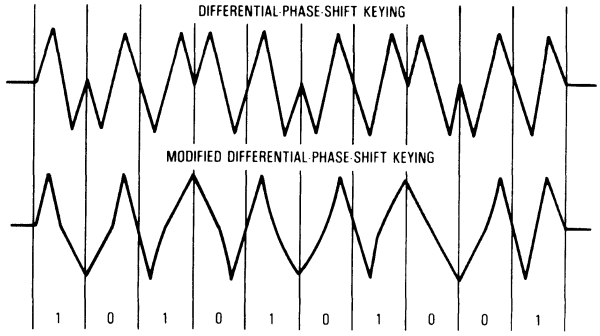
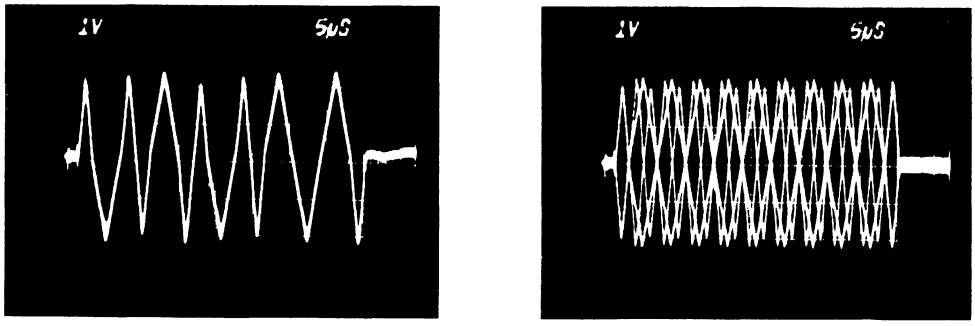


Figure 12. Modified Differential Phase Shift Keying

3

Both the Differential-Phase Shift Keying and the Modified Differential-Phase-Shift Keying waveforms are shown above. The DPSK encodes data as phase reversals of a 256 kHz carrier. A "0" is indicated by a 180 degree phase shift between bit boundaries, while the signal continues in phase to indicate a "1". This method needs no additional bits to indicate the start of the burst.

The Modified DPSK waveform actually used in the transceivers is a slightly modified form of DPSK, as shown in the figure. The phase-reversal cusps of the DPSK waveform have been replaced by a 128 kHz half cycle to lower the spectral content of the waveform, which, save for some key differences, appears quite similar to frequency-shift keying. The burst always begins and ends with a half cycle of 256 kHz, which helps locate bit boundaries.



13a–BIT PATTERN–1010101000

13b–BIT PATTERN–RANDOM

The bit pattern shown above in Figure 13a shows a stable waveform due to the even number of phase changes or zeros. The waveform shown in Figure 13b shows random data patterns being modulated.

Figure 13. Typical Modulated Waveforms

"Ping pong" signals on 3000 feet of 26 AWG twisted pair wire as viewed at LI (Line Input) of the master ULDT and the slave UDLT.

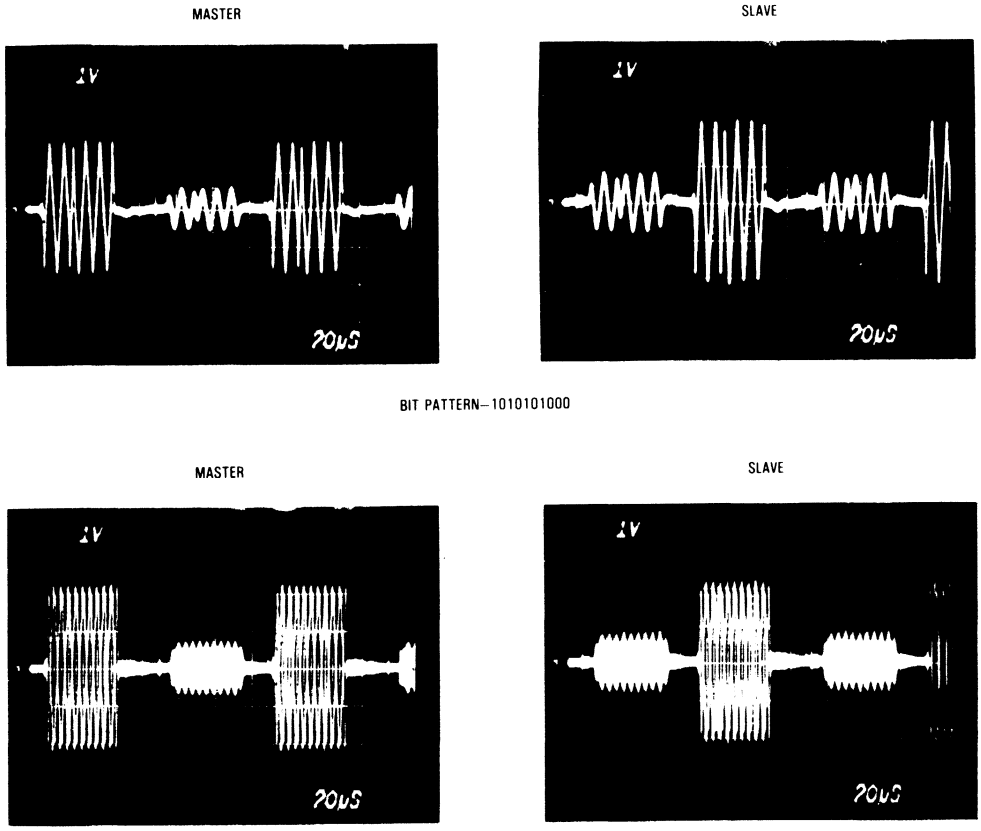


Figure 14. Typical Signal Waveforms at Demodulator

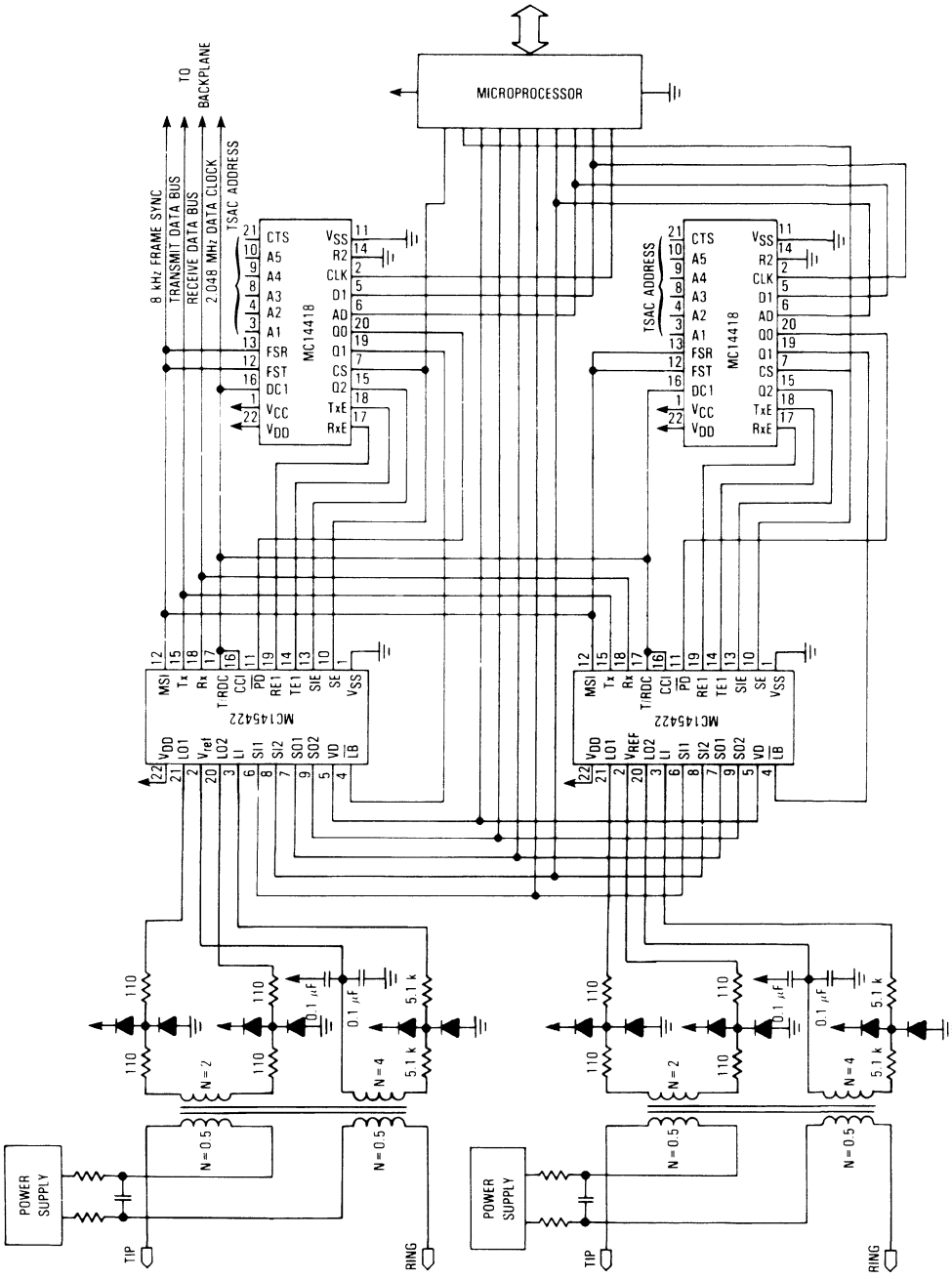


Figure 15. Typical Multichannel Digital Line Card

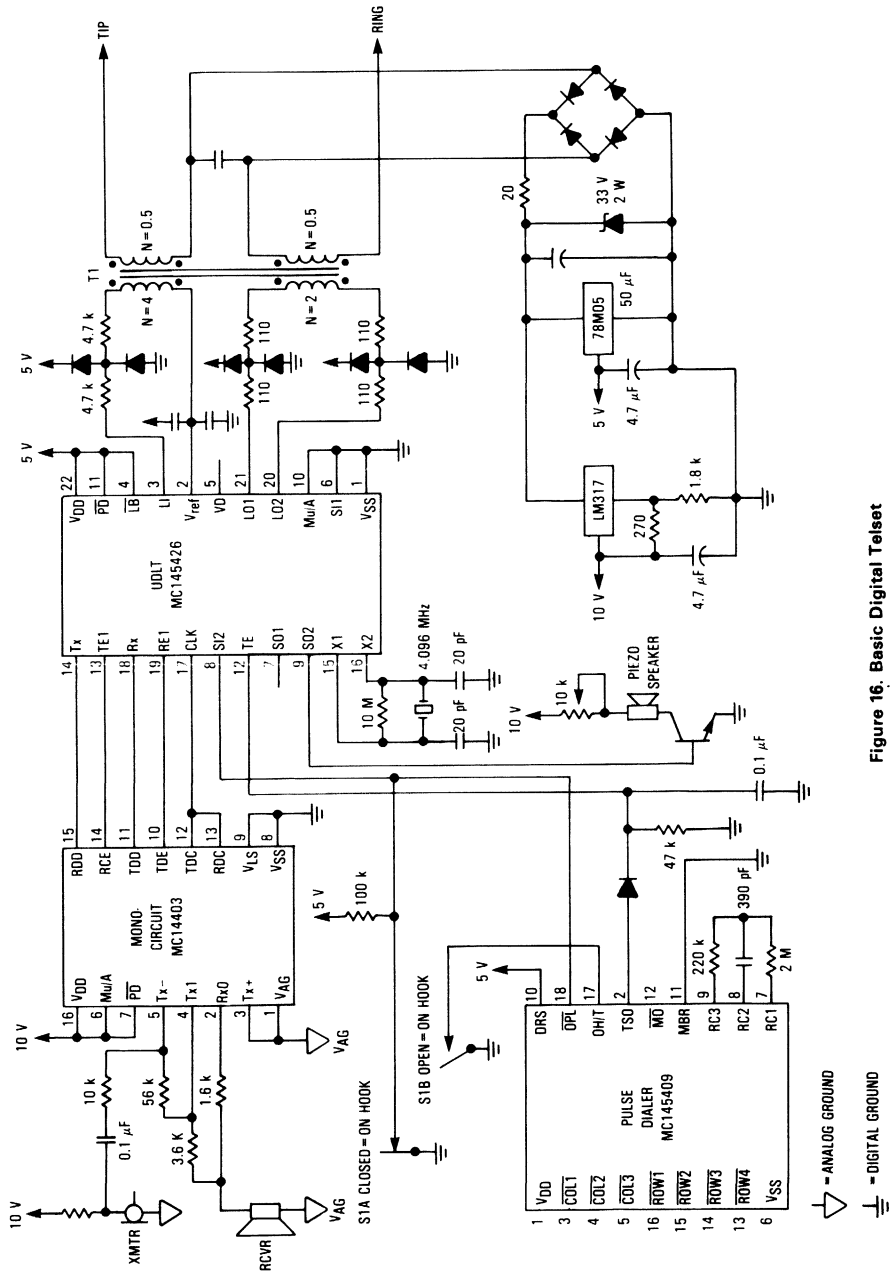


Figure 16. Basic Digital Telset

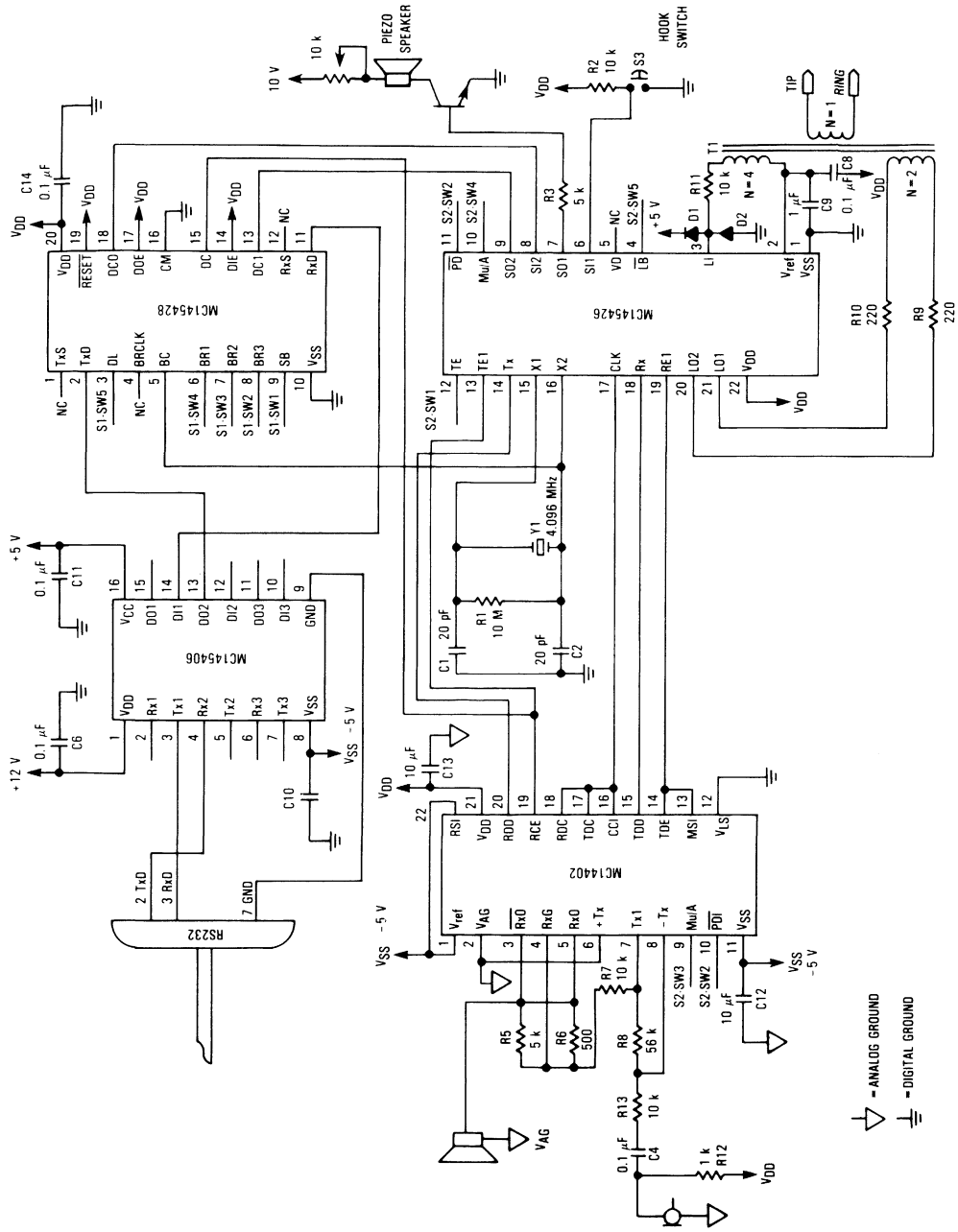


Figure 17. Full Featured Digital Telset

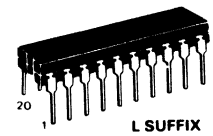
MC145428

MOTOROLA

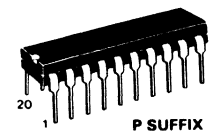
Advance Information

Data Set Interface

Asynchronous-To-Synchronous Synchronous-To-Asynchronous Converter



L SUFFIX
CERAMIC
CASE 732



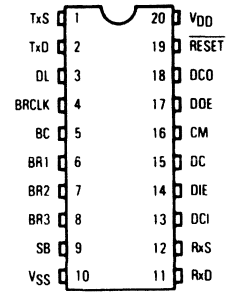
P SUFFIX
PLASTIC
CASE 738

3

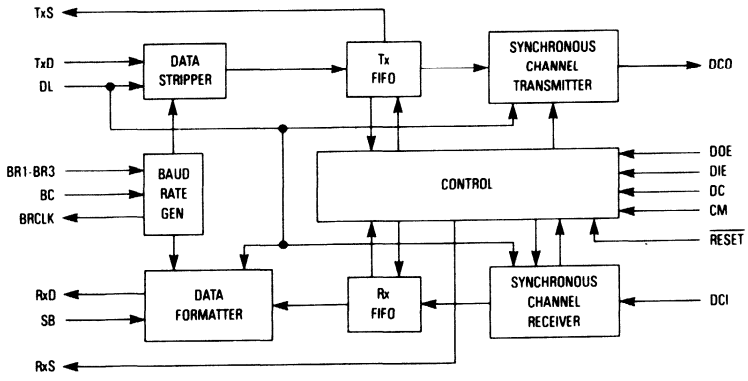
The MC145428 Data Set Interface provides asynchronous to synchronous and synchronous to asynchronous data conversion. It is ideally suited for voice/data digital telsets supplying an RS-232 compatible data port into a synchronous transmission link. Other applications include, data multiplexers, concentrators, data-only switching and PBX-based local area networks. This low power CMOS device directly interfaces with either the 64 kbps or 8 kbps channel of Motorola's MC145422 and MC145426 Universal Digital Loop Transceivers (UDLTs), as well as the MC145418 and MC145419 Digital Loop Transceivers (DLTs).

- Provides the Interface Between Asynchronous Data Ports and Synchronous Transmission Links
- Up to 128 kbps Asynchronous Data Rate Operation
- Up to 2.1 Mbps Synchronous Data Rate Operation
- On-board Bit Rate Clock Generator with Pin Selectable Bit Rates of 300, 1200, 2400, 4800, 9600, 19200 and 38400 bps or an Externally Supplied 16 Times Bit Rate Clock
- Accepts Asynchronous Data Words of Eight or Nine Bits in Length
- False Start Detection Provided
- Automatic Sync Insertion and Checking
- Single 5 Volt Power Supply
- Low Power Consumption of 5 mW Typical
- Applications Notes AN943 and AN946

PIN ASSIGNMENT



BLOCK DIAGRAM



ADI1019R1

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD} - V_{SS}	-0.5 to 6.0	V
Voltage, Any Pin to V_{SS}	V	-0.5 to V_{DD} +0.5	V
DC Current, Any Pin (Excluding V_{DD}, V_{SS})	I	+10	mA
Operating Temperature	T_A	-40 to +85	°C
Storage Temperature	T_{stg}	-85 to +150	°C

DIGITAL CHARACTERISTICS (V_{DD} = 4.5 to 5.5 V, T_A = 0 to 70°C)

Parameter	Symbol	V_{DD}	Min	Max	Unit
Input High Level	V_{IH}	5	3.5	—	V
Input Low Level	V_{IL}	5	—	1.5	V
Input Current	I_{in}	—	—	+1.0	μA
Input Capacitance	C_{in}	—	—	7.5	pF
Output High Current (Source) V_{OH} = 2.5 V V_{OH} = 4.6 V	I_{OH}	 5 5	 -1.7 -0.36	 — —	mA
Output Low Current V_{OL} = 0.4 V V_{OL} = 0.8 V	I_{OL}	 5 5	 0.36 0.8	 — —	mA
Operating Current (DC = 128 kHz, BC = 4.096 MHz)	I_{DD}	5	—	2.0	mA

SWITCHING CHARACTERISTICS (C_L = 50 pF, V_{DD} = 5 V, T_A = 25°C)

Characteristic	Min	Typ	Max	Unit
Baud Clock Bit Rate Input Frequency (BR1, BR2, BR3) = (0,0,0) (BR1, BR2, BR3) = non-zero	 — —	 — —	 2.1 4.1	MHz
Baud Clock Pulse Width	100	—	—	ns
Data Clock Frequency	—	—	2.1	MHz
Data Clock Pulse Width	200	—	—	ns

MC145428 DSI PIN DESCRIPTIONS

V_{DD}, POSITIVE POWER SUPPLY

The most positive power supply pin, normally 5 volts.

V_{SS}, NEGATIVE POWER SUPPLY

The most negative supply pin, normally 0 volts.

TxD, TRANSMIT DATA INPUT

Input for asynchronous data. Idle is logic high; break is 11 baud or more of logic low. One stop bit is required.

RxD, RECEIVE DATA OUTPUT

Output for asynchronous data. The number of stop bits and the data word length are selected by the SB and DL pins. Idle is logic high; break is a continuous logic low.

TxS, TRANSMIT STATUS OUTPUT

This pin will go low if the transmit FIFO holds 2 or more data words or if $\overline{\text{RESET}}$ is low.

RxS, RECEIVE STATUS OUTPUT

This pin will go low if framing of the synchronous channel is lost or not established or if $\overline{\text{RESET}}$ is low, or if the receive FIFO is overwritten.

SB, STOP BITS INPUT

This pin controls the number of stop bits the DATA FORMATTER will re-create when outputting data at the RxD asynchronous output. A high on this pin selects two stop bits; a low selects one stop bit.

DL, DATA LENGTH INPUT

This pin instructs the DSI to look for either 8 or 9 bits of data to be input at the TxD asynchronous input between the start and stop bits. The DL input also instructs the DSI's SYNCHRONOUS CHANNEL RECEIVER and SYNCHRONOUS CHANNEL TRANSMITTER to expect 8 or 9 bit data words and also instructs the DSI's DATA FORMATTER to re-create 8 or 9 data bits between the start and stop bits when outputting data at its RxD asynchronous output. A high on this pin selects a 9 bit data word; a low selects an 8 bit data word length.

MC145428 DSI PIN DESCRIPTIONS — cont'd.

BC, BAUD CLOCK INPUT

This pin serves as an input for an externally supplied 16 times data clock. Otherwise, the BC pin expects a 4.096 MHz clock signal which is internally divided to obtain the 16 times clock for the most frequently used standard bit rates (see BR1-BR3 pin description).

BRCLK, 16 TIMES CLOCK INTERNAL OUTPUT

This pin outputs the internal 16 times asynchronous data rate clock.

BR1, BR2, BR3, BIT RATE SELECT INPUTS

These three pins select the asynchronous bit rate, either externally supplied at the BC pin (16 times clock) or one of the internally supplied bit rates. (See Table 1.)

DCO, DATA CHANNEL OUTPUT

This pin is a three-state output pin. Synchronous data is output when DOE is high. This pin will go high impedance when DOE or $\overline{\text{RESET}}$ are low. When CM is low, synchronous data is output on DCO on the falling edges of DC as long as DOE is high. When CM is high, synchronous data is output on DCO on the rising edges of DC, while DOE is held high. No more than eight data bits can be output during a given DOE high interval when CM = high. This feature allows the DSI to interface directly with the MC145422/26 Universal Digital Loop Transceivers (UDLT's) and PABX time division multiplexed highways.

DOE, DATA OUTPUT ENABLE INPUT

See DCO pin description and the SYNCHRONOUS CHANNEL INTERFACE section.

DIE, DATA INPUT ENABLE INPUT

See DCI pin description and the SYNCHRONOUS CHANNEL INTERFACE section.

DC, DATA CLOCK INPUT

See DCI and DCO pin descriptions and the SYNCHRONOUS CHANNEL INTERFACE section.

CM, CLOCK MODE INPUT

See the SYNCHRONOUS CHANNEL INTERFACE section and the SYNCHRONOUS CLOCKING MODE SUMMARY. (See Table 2.)

$\overline{\text{RESET}}$, RESET INPUT

When held low, this pin clears the internal FIFO's, forces the TxD asynchronous input to appear high to the DSI's internal circuitry, forces TxS and RxS low. When returned high, normal operation results.

When the $\overline{\text{RESET}}$ input is returned high the DSI's SYNCHRONOUS CHANNEL RECEIVER will not accept or transfer any incoming data words on the DCI pin to the Rx FIFO until one "flag" word is input at the DCI pin. (Also see RxS pin description.)

DCI, DATA CHANNEL INPUT

Synchronous data is input on this pin on the falling edges of DC when DIE is high.

Table 1. Programmable Baud Rates

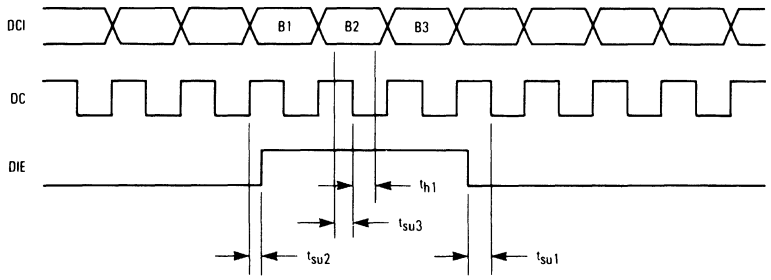
BR3	BR2	BR1	Bit Rate (bps)	BC in MHz	BRCLK
0	0	0	Variable 0 to 128 kbps	0 to 2.1 MHz	0 to 2.1 MHz
0	0	1	38.4 k	4.096	614.4 kHz
0	1	0	19.2 k	4.096	307.2 kHz
0	1	1	9600	4.096	153.6 kHz
1	0	0	4800	4.096	76.8 kHz
1	0	1	2400	4.096	38.4 kHz
1	1	0	1200	4.096	19.2 kHz
1	1	1	300	4.096	4.8 kHz

CM = LOW, SYNCHRONOUS CHANNEL RECEIVER INPUT SWITCHING CHARACTERISTICS

(C_L = 50 pF, V_{DD} = 5 V, T_A = 25°C) (See Figure 1A)

Characteristic	Symbol	Min	Typ	Max	Unit	Notes
DIE Fall Before DC Falls	t_{su1}	40	-9	—	ns	1
DIE Rise After Rise of DC	t_{su2}	40	+24	—	ns	2
DCI Data Stable Before DC Falling Edge	t_{su3}	40	-5	—	ns	3
DCI Data Stable After DC Falling Edge	t_{h1}	40	0	—	ns	4

NOTES:
1. Time DIE must fall before DC falls in order to avoid reading the bit after B3.
2. Time DC must be high before DIE rise in order to avoid clocking in the bit before B1. (See Synchronous Channel Interface for further details and see Figure 1A.)
3. Time data must be stable on the DCI pin before falling edge of the data clock DC.
4. Time data must be stable on the DCI pin after the falling edge of the data clock DC.



NOTE: When CM = 0, data bits are read into the DSI's SYNCHRONOUS CHANNEL RECEIVER at the DCI pin on the falling edge of the signal formed by the LOGICAL NAND of $\overline{DC}$ and DIE.
i.e. ↓ of $\overline{DC \bullet DIE}$

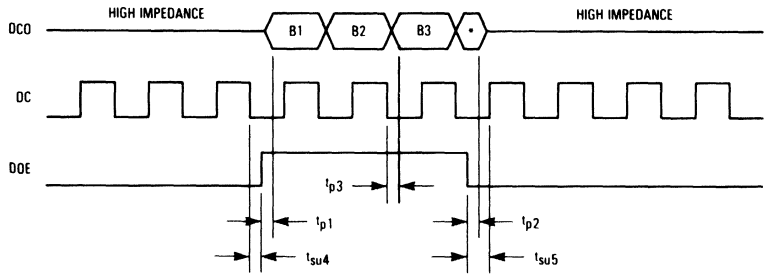
Figure 1A. CM = Low, Synchronous Channel Receiver Input Switching Characteristics

CM = LOW, SYNCHRONOUS CHANNEL TRANSMITTER OUTPUT SWITCHING CHARACTERISTICS

(C_L = 50 pF, V_{DD} = 5 V, T_A = 25°C) (See Figure 1B)

Characteristic	Symbol	Min	Typ	Max	Unit	Notes
DC Falling to DOE Rising	t_{su4}	0	10	—	ns	5
DOE Falling to DC Rising	t_{su5}	40	-5	—	ns	6
DOE Rising to DCO Active	t_{p1}	50	28	—	ns	7
DOE Falling to High-Z of DCO	t_{p2}	50	26	—	ns	8
DC Falling to DCO	t_{p3}	80	71	—	ns	9

NOTES:
5. Time DC must be low before the rising edge of DOE in order to avoid clocking out a data bit before B1. (See Synchronous Channel Interface section for further details and also Figure 1B.)
6. Time DOE must be low before the rising edge of DC in order for the (*) bit to be output in the B1 position in the next cycle.
7. Propagation delay time from the rising edge of DOE to the low output impedance state of the DCO pin.
8. Propagation delay time from the falling edge of DOE to the high output impedance state of the DCO pin.
9. Propagation delay time from the falling edge data of the data clock DC to valid data on the DCO pin.



*This bit will be output in the B1 position on the next cycle of DOE.

NOTE: When CM = Low, data bits are advanced from the DSI's SYNCHRONOUS CHANNEL TRANSMITTER at the DCO pin on the rising edge of the signal formed by the LOGICAL NAND of DC and DOE. i.e. ↑ of $\overline{DC \bullet DOE}$

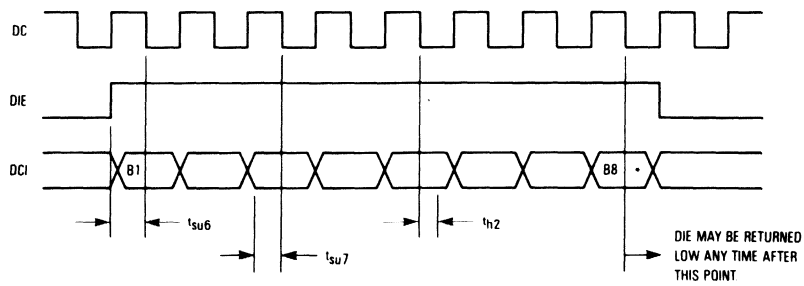
Figure 1B. CM = Low, Synchronous Channel Transmitter Output Switching Characteristics

CM = HIGH, SYNCHRONOUS CHANNEL RECEIVER INPUT SWITCHING CHARACTERISTICS

(C_L = 50 pF, V_{DD} = 5 V, T_A = 25°C) (See Figure 1C)

Characteristic	Symbol	Min	Typ	Max	Unit	Notes
DIE Rising to DC Falling	t_{su6}	100	76	—	ns	10
DCI to DC Falling	t_{su7}	40	-4	—	ns	11
DC Falling to DCI	t_{h2}	20	0	—	ns	12

NOTES:
10. Time DIE must be high before the falling edge of DC in order for the data bit to be accepted by the synchronous data input of the DSI. (See Synchronous Channel Interface for further details.)
11. Time DCI data must be stable before the falling edge of the data clock DC.
12. Time DCI data must be stable after the falling edge of the data clock DC.



*Last bit accepted.

NOTE: When CM = 1, data bits are read into the DSI's SYNCHRONOUS CHANNEL RECEIVER at the DCI pin on the falling edge of the signal formed by the LOGICAL AND of DC and DIE. (DC ● DIE)

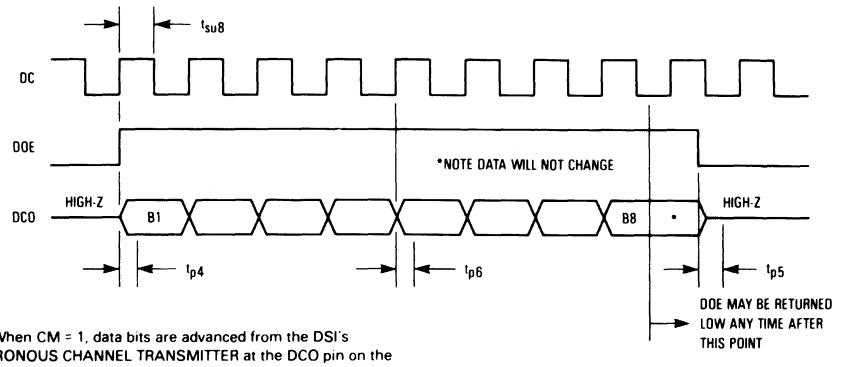
Figure 1C. CM = High, Synchronous Channel Receiver Input Switching Characteristics

CM = HIGH, SYNCHRONOUS CHANNEL TRANSMITTER OUTPUT SWITCHING CHARACTERISTICS

(C_L = 50 pF, V_{DD} = 5 V, T_A = 25°C) (See Figure 1D)

Characteristic	Symbol	Min	Typ	Max	Unit	Notes
DC Falling to DOE Rising	t_{su8}	100	82	—	ns	13
DOE Rising to Active Data on DCO	t_{p4}	105	87	—	ns	14
DOE Falling to High-Z on DCO	t_{p5}	50	28	—	ns	15
DC Rising to DCO	t_{p6}	100	74	—	ns	16

NOTES:
13. Time DOE must be high before the falling edge of the data clock DC.
14. Time delay between the rise of the DOE pin and the time the DCO reaches the low impedance state.
15. Time delay between the fall of the DOE pin and the time the DCO pin reaches the high impedance state.
16. Delay from the rising edge of the data clock DC to the valid data on the DCO pin.



NOTE: When CM = 1, data bits are advanced from the DSI's SYNCHRONOUS CHANNEL TRANSMITTER at the DCO pin on the rising edge of the signal formed by the LOGICAL AND of DC and DOE. (DC • DOE)

Figure 1D. CM = High, Synchronous Channel Transmitter Output Switching Characteristics

CIRCUIT DESCRIPTION

The MC145428 Data Set Interface provides a means for conversion of an asynchronous (start/stop format) data channel to a synchronous data channel and synchronous to asynchronous data channel conversion. Although primarily intended to facilitate the implementation of RS-232 compatible asynchronous data ports in digital telephone sets using the MC145422/26 UDLTs, this device is also useful in many applications that require the conversion of synchronous and asynchronous data.

TRANSMIT CIRCUIT

Asynchronous data is input on the TxD pin. This data is expected to consist of a start bit (logic low) followed by eight or nine data bits and one or more stop bits (logic high). The length of the data word is selected by the DL pin. The data baud rate is selected with the BR1, BR2, and BR3 pins to obtain the internal sampling clock. This internal sampling clock is selected to be 16 times the baud rate at the TxD pin. An externally supplied 16 times clock may also be used, in which case, the BR1, BR2, and BR3 pins should all be at logic zero and the 16 times sampling clock supplied at the BC pin.

Data input at the TxD pin is stripped of start and stop bits and is loaded into a four-word deep FIFO register. A break condition is also recognized at the TxD pin and this information is relayed to the synchronous channel transmitter which codes this condition so it may be re-created at the remote receiving device.

The synchronous channel transmitter sends one bit at a time under control of the DC, CM, and DOE pins. The synchronous channel transmitter transmits one of three possible data patterns based on whether or not the top of the Tx FIFO is full and whether or not a break condition has been recognized by the data stripper. When no data is available at the top of the Tx FIFO for transmission, the synchronous data transmitter sends a special synchronizing flag pattern (01111110). When a break condition is detected by the data stripper and no data is available at the top of the Tx FIFO, the break pattern (11111110) is sent. Figure 2A depicts this operation.

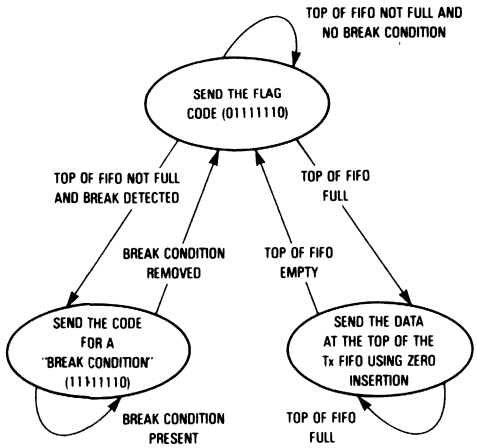


Figure 2A. Synchronous Data Channel Transmitter Operation

When stripped data words reach the top of the Tx FIFO they are loaded into the SYNCHRONOUS CHANNEL TRANSMITTER and are sent using a special zero insertion technique. When stripped data is being transmitted, the synchronous data transmitter will insert a binary 0 after any succession of five continuous 1's of data. Therefore, using this technique, no pattern of (01111110) or (11111110) can occur while sending data. This also allows the DSI to synchronize itself to the incoming synchronous data word boundaries based on the data alone.

The receive section of the DSI (synchronous channel receiver) performs the reverse operation by removing a binary 0 that follows five continuous 1's in order to recover the transmitted data. (Note that a binary 1 which follows five continuous 1's is not removed so that flags and breaks may be detected.) Figure 2B shows an example of this process.

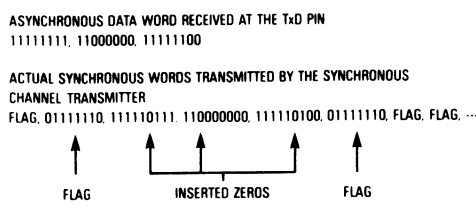


Figure 2B. Data Format Protocol

If the incoming data rate at TxD exceeds the rate at which it is output at DCO, the FIFO will fill. The TxS pin will go low when the FIFO contains two or more words. TxS may, therefore, be used as a local Clear-to-Send control line at the asynchronous interface port to avoid transmit data over-runs.

In order to insure synchronization during the transfer of a continuous stream of data the DSI's synchronous channel transmitter will insert a flag synchronizing word (01111110) every 61st data word. The DSI's synchronous channel receiver checks for this synchronizing word and if not present, the loss of synchronization will be indicated by the RxS pin being latched low until the flag synchronizing word is received. Note that under these conditions the data will continue to output at RxD.

RECEIVE CIRCUIT

Data incoming from the synchronous channel is loaded into the MC145428 at the DCI pin under the control of the DC and DIE pins (see SYNCHRONOUS CHANNEL INTERFACE section). Framing information, break code detection, and data word recovery functions are performed by the SYNCHRONOUS CHANNEL RECEIVER. Recovered data words are loaded into the four word deep Rx FIFO. When the recovered data words reach the top of the Rx FIFO they are taken by the DATA FORMATTER, start and stop bits are re-inserted and the reconstructed asynchronous data is output at the RxD pin at the same baud rate as the transmit side. The number of stop bits and word length are those selected by the SB and DL pins.

Loss of framing, if it occurs, is indicated by the RxS pin going low. Data will continue to be output under these conditions, but RxS will remain low until frame synchronization, i.e., the detection of a framing flag word, is re-established. If the output data rate is less than the data rate of the incoming synchronous data channel, data will be lost at a rate of one word at a time due to the bottom word on the Rx FIFO being overwritten. In order to prevent data loss (in the form of asynchronous terminal to asynchronous terminal over-runs) due to clock slip between remote DSI links, (during long bursts of continuous data) the DSI purposely reduces the length of the stop bit which it re-creates at its RxD output by 1/32nd. This action allows the originator of a transmission (of asynchronous data) to be up to 3% faster than the receive device is expecting for any given data rate. This tolerance is well within the normally expected differences in clock frequencies between remote stations. If the Rx FIFO is overwritten the RxS line will pulse low for one DC clock period following the over-writing of the bottom level of the Rx FIFO.

INITIALIZATION

Initialization is accomplished by use of the $\overline{\text{RESET}}$ pin. When held low, the internal FIFOs are cleared, the TxD input appears high to the data strippers internal circuitry, DCO is forced to a high impedance state, TxS and RxS are forced low. When brought high normal operation resumes and the synchronous channel transmitter sends the flag code until data has reached the top of the Tx FIFO. Note that the TxS line will immediately go high after $\overline{\text{RESET}}$ goes high, while RxS

will remain low until framing is detected. The synchronous channel receiver section of the DSI is forced into a "HOLD" state while the $\overline{RESET}$ line is low. The synchronous channel receiver remains in the "HOLD" state after $\overline{RESET}$ goes high until a flag code word (01111110) is received at the DCI pin. While in the "HOLD" state no data words can be transferred to the Rx FIFO and, therefore, the DATA FORMATTER and RxD line are held in the MARK idle state. After receiving the flag code pattern the RxS line goes high and normal operation proceeds. $\overline{RESET}$ should be held low when power is first applied to the DSI. $\overline{RESET}$ may be tied high permanently, if a short period of undefined operation at initial power application can be tolerated.

SYNCHRONOUS CHANNEL INTERFACE

3

The synchronous channel interface is generally operated in one of three basic modes of operation. The first is a continuous mode. A new data bit is clocked out of the DCO pin on each successive falling edge of the DC clock, and a new data bit is accepted by the DSI at its DCI pin on each successive falling edge of the DC clock. In this mode of operation, the CM control line is always low and the DOE and DIE enable control lines are always high. This is the typical setup when interfacing the DSI to the 8 kbps signal bit inputs and outputs of the MC145422/26 UDLTs. (See Figures 3A and 4.)

The second synchronous clocking mode is one in which 8 bits at a time are clocked out of the SYNCHRONOUS CHANNEL TRANSMITTER, and 8 bits are read by the SYNCHRONOUS CHANNEL RECEIVER at a time. The transferring of these 8 bit groups of data would normally be repeated on some cyclic basis. An example is a time division multiplexed data highway. In this mode (CM = 1), the rising edge of the enable signal DIE and DOE should be roughly aligned to the rising edge of the DC clock signal. When enabled, the data is clocked out on the rising edge of the DC clock through the DCO pin and clocked in on the falling edge of the DC clock through the DCI pin. A variation of this clocking mode is to transfer less than 8 bits of data into or out of the DSI on a cyclic basis. If less than eight bits are to be transmitted and received, enable pins DIE and DOE should be returned low while the DC clock is low. This is illustrated in Figure 3D where five bits are being clocked out of the DSI through the DCO pin and four bits are being input to the DSI through the DCI pin.

This restriction does not apply if eight bits are to be clocked into or out of the synchronous channels of the DSI; i.e., the DSI has internal circuitry to prevent more than eight clocks following the rising edge of the respective enable signals). Figure 3B illustrates a timing diagram depicting an eight bit data format. If the DOE enable is held high beyond the eight clock periods the last data bit B8 will remain at the output of the DCO pin until the DOE enable is brought low to reinitialize the sequence. Similarly the DSI's SYNCHRONOUS CHANNEL RECEIVER will read (at its DCI input) a mixmum of eight data bits for any given DIE high period.

The CM = high mode, using 8 bits of data, is the typical setup for interfacing the DSI to the 64 kbps channel of the MC145422 or MC145426 Universal Digital Loop Transceivers. (See Figure 3B and Figure 5.)

In the third mode of operation, an unlimited variable number of data bits may be clocked into or out of the synchronous side of the DSI at a time. When the CM line is low, any number of data bits may be clocked into or out of the DSI's synchronous channels provided that the respective enable signal is high. Figure 3C illustrates three data bits being clocked out of the DCO pin and three data bits being clocked into the DCI pin.

In the CM = low mode of operation, an internal clock is formed, which is the logical NAND of DC, DOE and $\overline{CM}$, ($\overline{DC \bullet DOE \bullet \overline{CM}}$). It is on the rising edge of this signal that a new data bit is clocked out of the DCO pin. Therefore, the DOE signal should be raised and lowered following the falling edge of the DC clock (i.e., when the DC clock is low).

Also in the CM = low mode of operation, another internal clock is formed which is the logical NAND of $\overline{DC}$, DIE, and $\overline{CM}$ ($\overline{\overline{DC} \bullet DIE \bullet \overline{CM}}$). It is on the falling edge of this signal that a new bit is clocked into the DCI pin. Therefore the DIE signal should be raised and lowered following the rising edge of the DC clock (i.e., when the DC clock is high).

The following table summarizes when data bits are advanced from the synchronous channel transmitter and when data bits are read by the synchronous channel receiver dependent on the CM control line. (Shown below in Table 2.)

Table 2. Synchronous Clocking Mode Summary

Mode	Bits Advanced From The Synchronous Channel Transmitter On;	Bits Read By The Synchronous Channel Receiver On:
CM = 0	The rising edge of an internal clock formed by the logical NAND of DOE and DC. i.e. ↑ of $\overline{DOE \bullet DC}$	The falling edge of an internal clock formed by the logical NAND of DIE and $\overline{DC}$. i.e. ↓ of $\overline{DIE \bullet \overline{DC}}$
CM = 1	The rising edge of an internal clock formed by the logical AND of DOE and DC. i.e. ↑ of DOE • DC	The falling edge of an internal clock formed by the logical AND of DIE and DC. i.e. ↓ of DIE • DC

TIMING DIAGRAMS

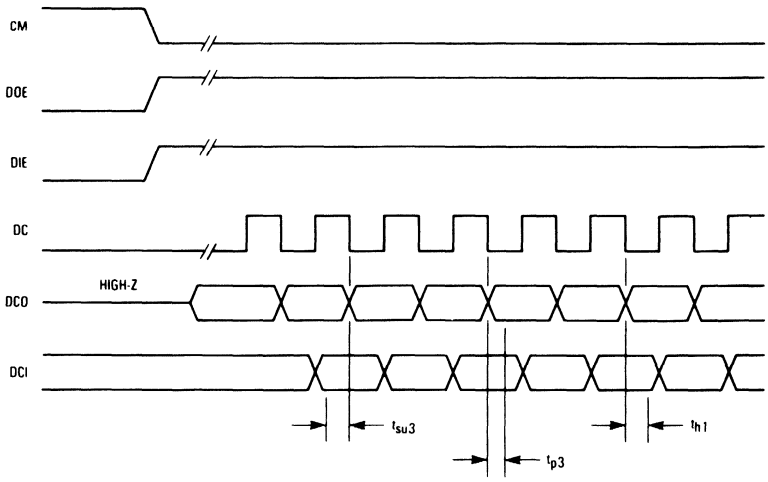


Figure 3A. Synchronous I/O, Continuous Bit Rate, Clock Mode Low

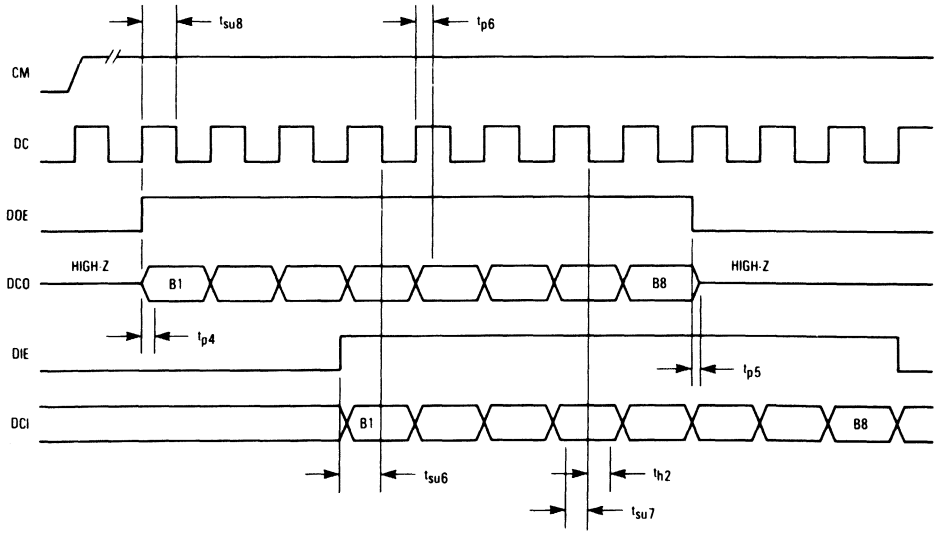


Figure 3B. Synchronous I/O, Eight Bit, Clock Mode High

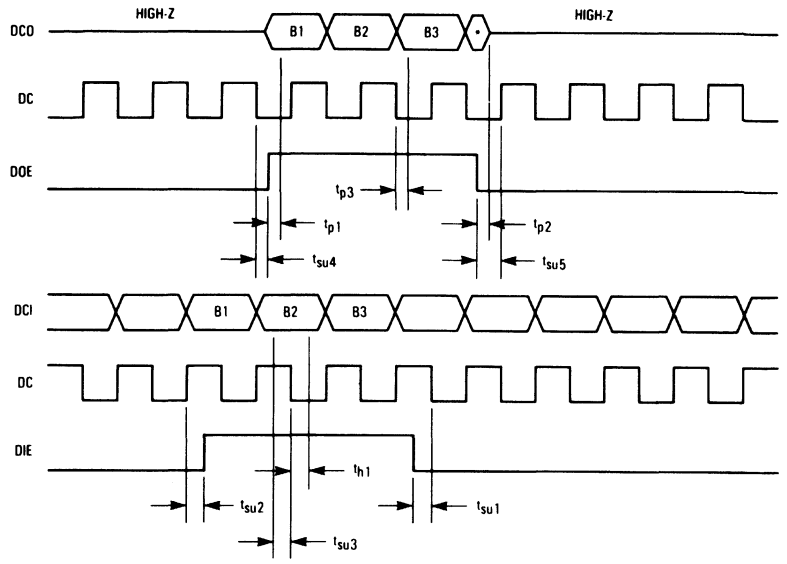


Figure 3C. Synchronous I/O, Variable Bit Length, Clock Mode Low

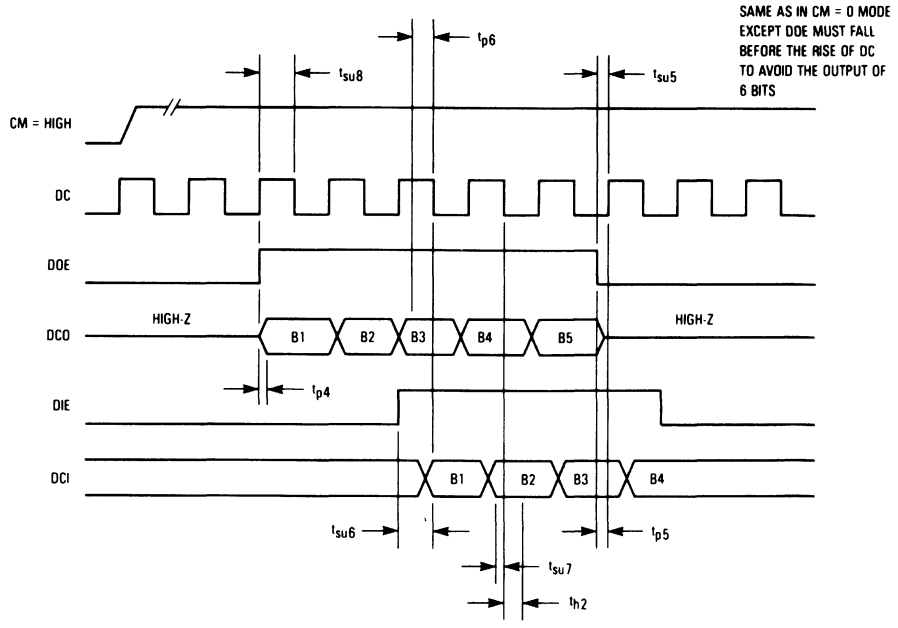
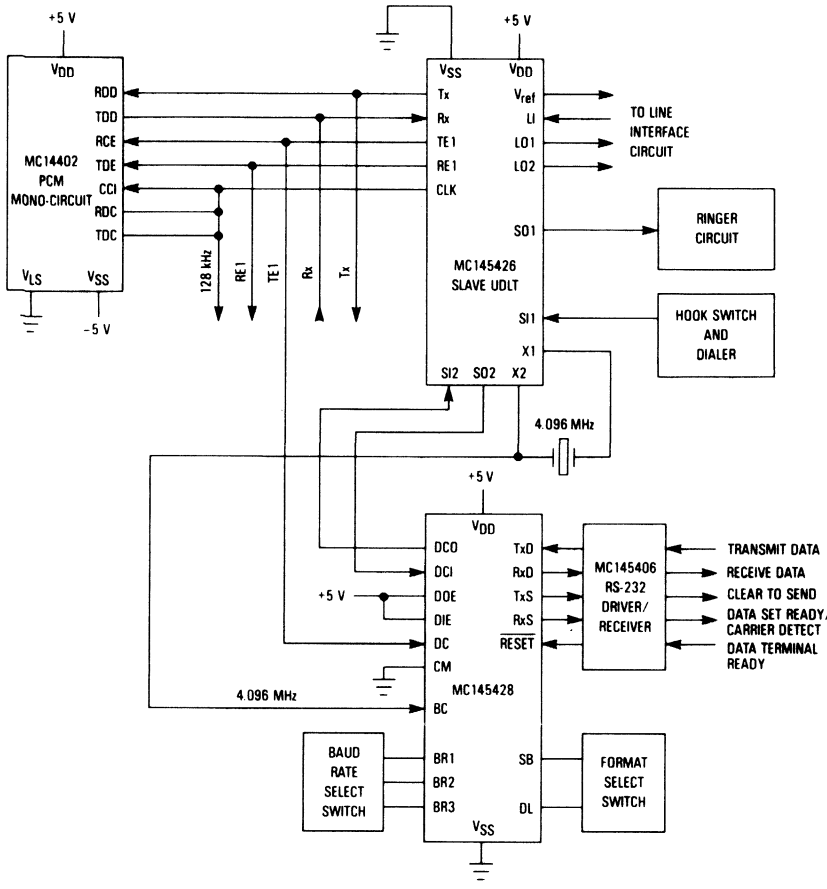
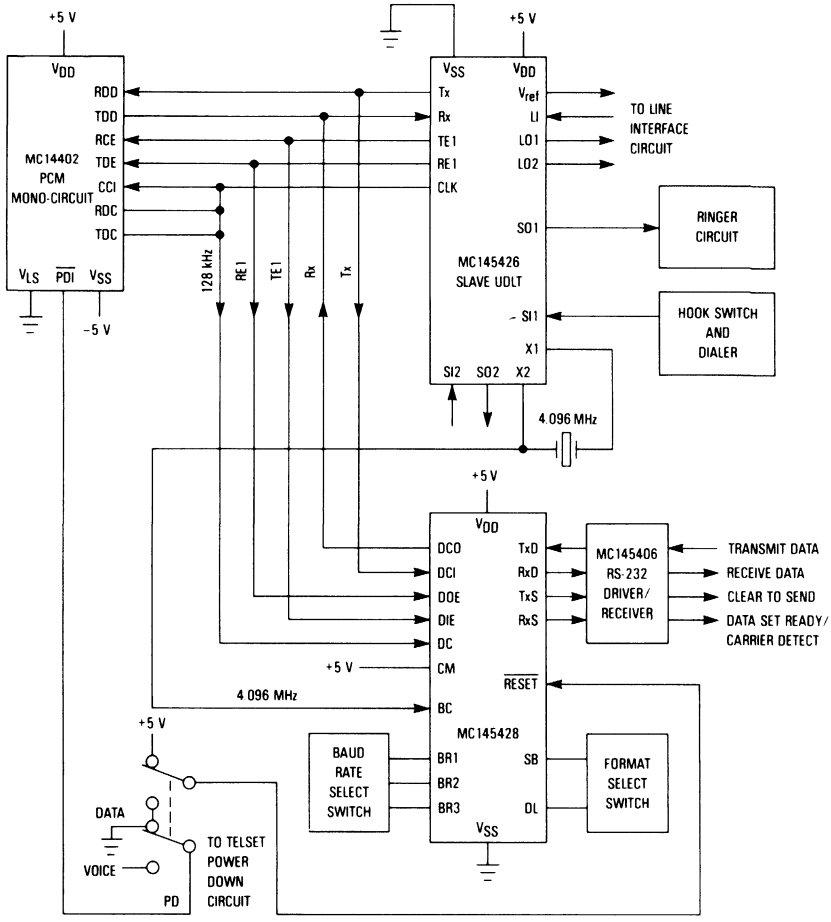


Figure 3D. Synchronous I/O, Variable Bit Length, Clock Mode High



NOTE: Some pin connections on the MC145426 and MC14402 have been omitted. Consult MC145426 and MC14402 data sheets for more details.

Figure 4. Digital Telset RS-232 Port Using 8 Kilobits/Second Channel of MC145426



NOTE: Some pin connections on the MC145426 and MC14402 have been omitted. Consult MC145426 and MC14402 data sheets for more details.

Figure 5. Digital Telset RS-232 Port Using 64 Kilobits/Second Channel of MC145426 for Voice or Data

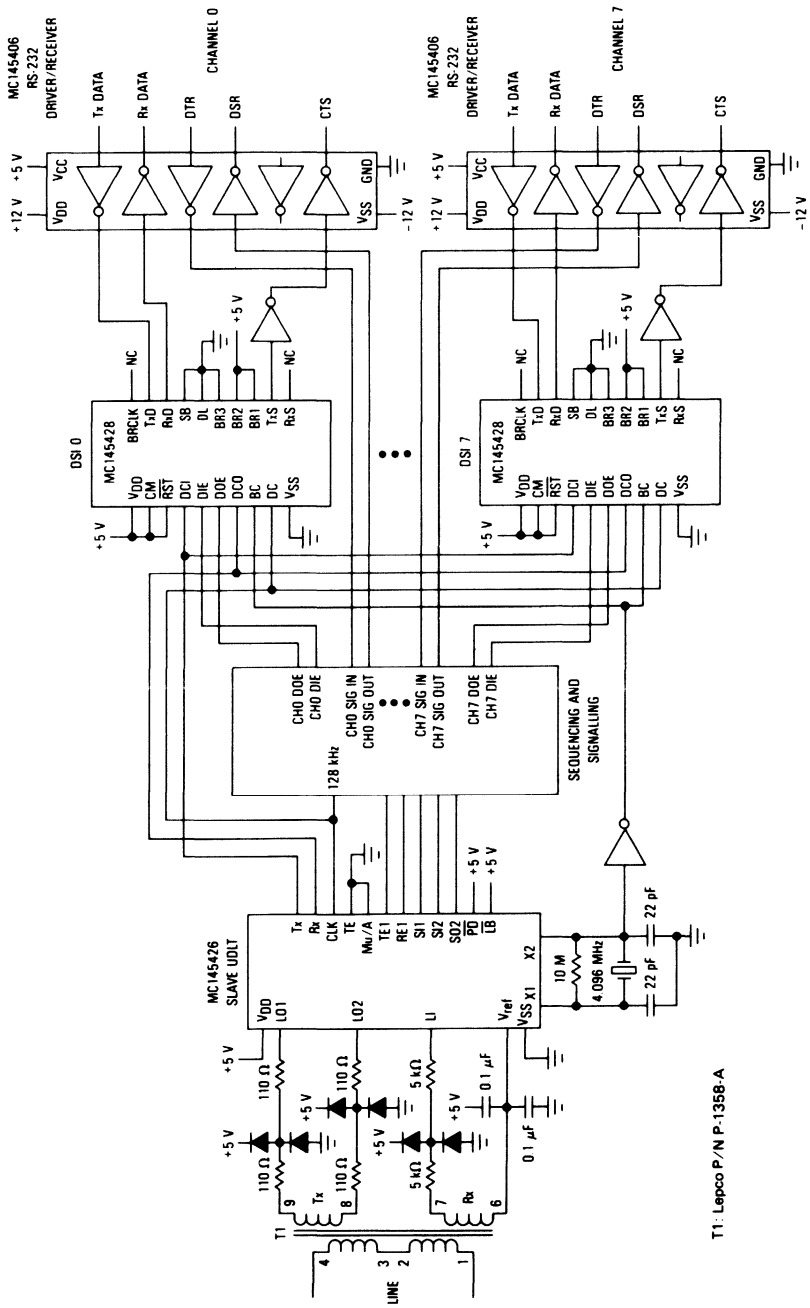


Figure 6. Multiplexing Eight RS-232 Telset Ports Into 64 Kilobits/Second Channel of MC145426

MOTOROLA

MC145429

Advance Information

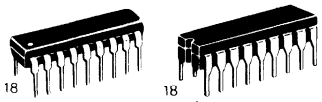
TELSET AUDIO INTERFACE

The MC145429 is a silicon-gate CMOS Telset Audio Interface IC intended for microcomputer controlled digital or analog telset applications. The device provides the interface between a codec/filter or analog speech network and the telset mouthpiece, earpiece, ringer/speaker amplifier, and an auxiliary input and output. The configuration of the device is programmed via a serial digital data port. Features provided on the device include:

- Independent Adjustment of Earpiece, Speaker, and Ringer Volume
- Transient Suppression Circuitry to Prevent Acoustic "Pops"
- Receive Low-Pass Filter for 8 kHz Attenuation
- Sixteen Possible Audio Configurations
- Power-Down Mode with Data Retention
- 20 dB Mouthpiece Input Gain
- Receive to Transmit Loopback Test Mode
- Provision for Auxiliary Input and Output
- Externally Adjustable Auxiliary Input Gain
- PCM Mono-circuit Compatible Power Supply Range
- Digital Output for Speaker Amplifier Control
- Versatile Logic Input Levels
- 18-Pin Package

CMOS
(LOW-POWER COMPLEMENTARY MOS)

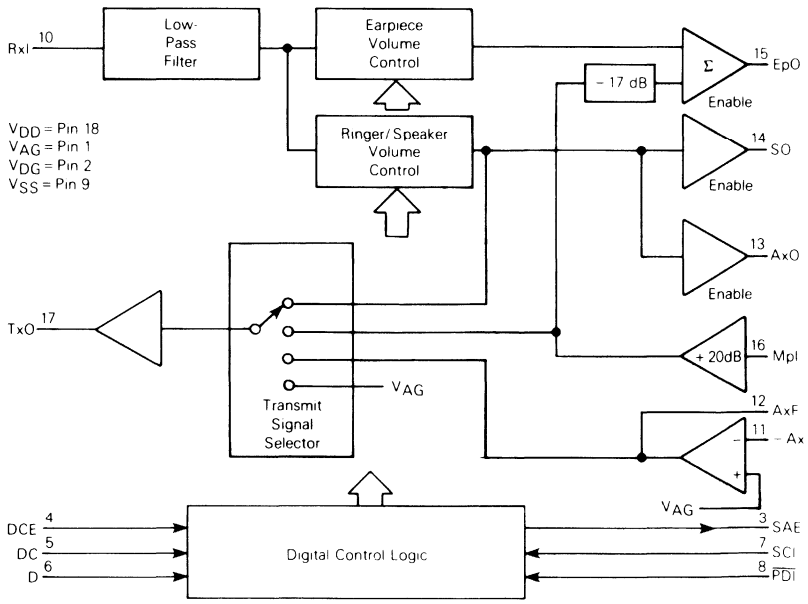
TELSET
AUDIO INTERFACE



P SUFFIX
PLASTIC PACKAGE
CASE 707

L SUFFIX
CERAMIC PACKAGE
CASE 726

SIMPLIFIED BLOCK DIAGRAM



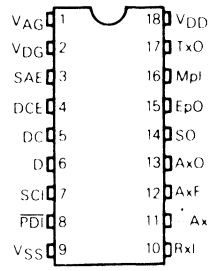
This document contains information on a new product. Specifications and information herein are subject to change without notice.

ADI965

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	$V_{DD} - V_{SS}$	−0.5 to 13	V
Voltage, Any Pin to V_{SS}	V	0.5 to V_{DD} + 0.5	V
DC Current Drain per Pin (Excluding V_{DD}, V_{SS})	I	10	mA
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−85 to +150	°C

PIN ASSIGNMENTS



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	$V_{DD} - V_{SS}$	6	10 to 12	13	V
DC Supply Voltage Nominally $(V_{DD} - V_{SS})/2$	$V_{DD} - V_{DG}$	3	5 to 7	7.5	V
Power Dissipation	P_D				mW
$V_{DD} - V_{SS}$ = 10 V		–	25	50	
$V_{DD} - V_{SS}$ = 12 V		–	30	60	
Power Down Dissipation	P_D				mW
$V_{DD} - V_{SS}$ = 12 V		–	3	5	
Full Scale Input Levels					Vpk
$V_{DD} - V_{SS}$ = 10 V RxI, AxF		–	–	3.15	
MpI		–	–	0.315	
$V_{DD} - V_{SS}$ = 12 V RxI, AxF		–	–	3.8	
MpI		–	–	0.38	
Sampling Clock Input Frequency		–	128	–	kHz

TRANSMISSION CHARACTERISTICS

(V_{DD} to V_{SS} = 10 to 12 V ±5%, T_A = 0 to 70°C, 0 dBm0 = 6 dBm ref 600 Ω, +3.17 dBm0 = 3.15 Vp, SCI = 128 kHz)

Characteristic		Min	Max	Unit
Gain				dB
840 Hz @ 0 dBm0, Max Gain Setting	RxI to EpO	−0.3	0.3	
	RxI to SO	−0.3	0.3	
	RxI to AxO	−0.3	0.3	
	RxI to TxO	0.3	0.3	
	AxF to TxO	−0.3	0.3	
840 Hz @ −20 dBm0	MpI to TxO	19.5	20.5	
	MpI to EpO	2.5	3.5	
Gain vs Volume				dB
Relative to Volume Setting, with 840 Hz @ 0 dBm0 Input				
(−3 to −21 dB)	RxI to EpO	−0.5	0.5	
(−5 to −35 dB)	RxI to SO or AxO	−0.5	0.5	
Idle Noise				
0 to 15 kHz, AxF = −Ax, RxI = MpI = 600 Ω to V_{AG}	TxO, EpO, SO, or AxO	–	−75.0	dBm0
C-Message		–	9.0	dBrnC0
In-Band Spurious Outputs				dBm0
840 Hz @ 0 dBm0, 0.3 to 3.4 kHz, 2nd and 3rd Harmonic		–	−43.0	
Out-Band Spurious Outputs				dBm0
840 Hz @ 0 dBm0, 0 to 20 kHz		–	−40.0	
Gain vs Frequency				dB
Relative to 840 Hz @ 0 dBm0				
(0.3 to 3.0 kHz, All Gain Paths)		−0.25	0.25	
(3.4 kHz, Rx Path)		−1.0	0.25	
(8.0 kHz, Rx Path)		–	−26.0	
Crosstalk				dBm0
840 Hz @ 0 dBm0	Rx to Tx and Tx to Rx	–	−65.0	
Isolation from Any Input to Any Deselected Output				dBm0
Input = 840 Hz @ 0 dBm0		–	−75.0	

ANALOG ELECTRICAL CHARACTERISTICS ($V_{DD} - V_{SS}$ = 10 to 12 V ±5%, T_A = 0 to 70°C)

Characteristic		Min	Typ	Max	Unit
Input Leakage Current	SCI, D, DC, DCE, RxI, – Ax	–	±10	±30	nA
	V_{AG}, MpI	–	±50	±60	μA
AC Input Impedance	RxI	100	200	–	kΩ
	MpI to V_{AG}	8	10	–	
$\overline{PDI}$ Internal Input Pull Down Resistor Impedance to V_{SS}		50	100	200	kΩ
Output Voltage Range	TxO, EpO, SO, AxO				V
$V_{DD} - V_{SS}$ = 10 V, R_L = 600 to V_{AG}		–3.2	–	3.2	
$V_{DD} - V_{SS}$ = 12 V, R_L = 900 to V_{AG}		–3.8	–	3.8	
Output Current	TxO, EpO, SO, AxO				mA
Source		–5.5	–	–	
Sink		5.5	–	–	
Power Supply Rejection Ratio	TxO, EpO, SO, AxO	20	30	–	dB
V_{AC} = 100 mVrms, 0 to 20 kHz, V_{DD}, V_{SS}					

3

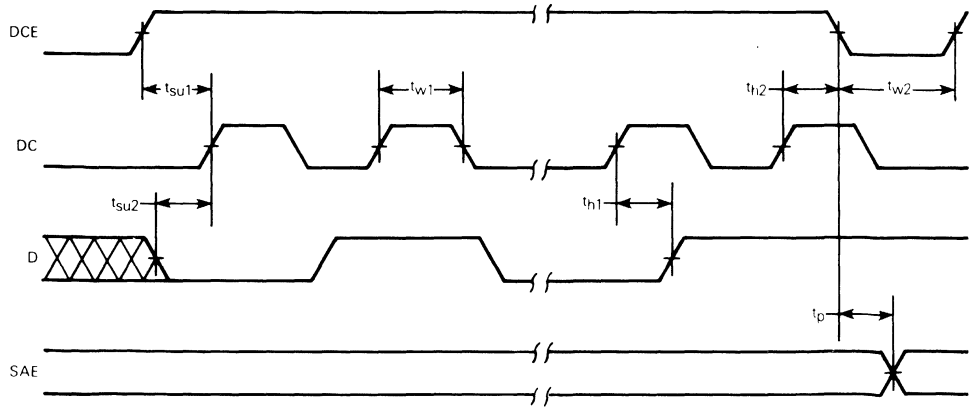
DIGITAL ELECTRICAL CHARACTERISTICS (T_A = 0 to 70°C, V_{DD} = 5.0 V, V_{SS} = –5.0 V, V_{DG}, V_{AG} = 0)

Characteristic		Symbol	Min	Max	Unit
Logic Input Voltage (V_{DG} = 0 V)	SCI, D, DC, DCE, $\overline{PDI}$				V
V_{SS} to V_{DD} Mode		V_{IL}	–	–3.5	
		V_{IH}	2.0	–	
V_{DG} to V_{DD} Mode		V_{IL}		0.8	
		V_{IH}	2.0	–	
V_{SS} to V_{DG} Mode		V_{IL}		–3.5	
		V_{IH}	–1.5	–	
Logic Output Voltage (V_{DG} = 0 V, $\|I_O\| < 1$ μA)	SAE	V_{OL}	–	–4.95	V
		V_{OH}	4.95	–	
Output Current (V_O = –4.5 V)	SAE	I_{OL}	0.9	–	mA
(V_O = 4.5 V)		I_{OH}	–0.3	–	

SWITCHING CHARACTERISTICS (T_A = 0 to 70°C, V_{DD} = 5.0 V, V_{SS} = –5.0 V, V_{DG}, V_{AG} = 0)

Characteristic		Symbol	Min	Max	Unit
Maximum Frequency	DC (Data Clock)	f_{max}	–	1.0	MHz
Minimum Pulse Width	DC	t_{w1}	0.5	–	μs
Minimum Pulse Width Low (SCI = 128 kHz)	DCE	t_{w2}	33	–	
Propagation Delay (SCI = 128 kHz)	DCE to SAE	t_p	30	60	μs
Setup Times	DCE to DC	t_{su1}	0.5	–	μs
	D to DC	t_{su2}	0.5	–	
Hold Times	D to DC	t_{h1}	0.5	–	μs
	DCE to DC	t_{h2}	0.5	–	

FIGURE 1 – DATA INPUT TIMING



PIN DESCRIPTIONS

V_{DD}, POSITIVE POWER SUPPLY (PIN 18) – Typically +3 to +6.5 volts with V_{AG} = 0 volts.

V_{SS}, NEGATIVE POWER SUPPLY (PIN 9) – Typically −3 to −6.5 with V_{AG} = 0 volts.

V_{AG}, ANALOG GROUND (PIN 1) – Typically 0 volts supplied by a mono-circuit in digital telset applications. All analog signals are referenced to this pin.

V_{DG}, DIGITAL GROUND (PIN 2) – Typically common to logic ground. All internal digital logic operates between V_{DG} and V_{DD}. V_{DG} preferably equals $(V_{DD} - V_{SS})/2$.

SAE, SPEAKER AMPLIFIER ENABLE (PIN 3) – The SAE output will be at V_{DD} whenever the external speaker amplifier is required, otherwise SAE is at V_{SS}.

DCE, DATA CLOCK ENABLE (PIN 4) – This digital input enables the serial data entry circuitry and also latches the serial data into the appropriate data register.

DC, DATA CLOCK (PIN 5) – This digital input allows data on the D pin to be shifted into the serial input data register on rising edges of DC whenever DCE is active.

D, DATA (PIN 6) – Digital data, required to set the configuration or gain of the audio interface, is applied to the D pin and will be shifted into the serial input register by DC whenever DCE is active.

SCI, SAMPLING CLOCK INPUT (PIN 7) – The clock applied to this digital input is used to sample the audio signals. This frequency is nominally 128 kHz and is typically provided by the slave Universal Digital Loop Transceiver such as the MC145426 in digital telset applications. This clock must be applied during data transfers.

$\overline{PDI}$, POWER-DOWN INPUT (PIN 8) – This pin allows all analog circuitry on the device to be powered down while retaining all digital data. An internal pull-down resistor connected to V_{SS} will insure the powered down state during system power up.

RxI, RECEIVE INPUT (PIN 10) – This pin is the input to the receive low-pass filter and volume controls, and is typically driven from RxO of a mono-circuit in digital telset applications.

−Ax, INVERTING AUXILIARY INPUT (PIN 11), AxF, AUXILIARY FEEDBACK (PIN 12) – These two pins are the inverting input and output, respectively, of the auxiliary input operational amplifier and are used to set the gain of the auxiliary input. The noninverting input of the Ax amp is internally connected to V_{AG}.

AxO, AUXILIARY OUTPUT (PIN 13) – This output drives the input to an external auxiliary circuit and will be at V_{AG} when disabled.

SO, SPEAKER OUTPUT (PIN 14) – This output drives an external speaker amplifier, and when disabled will be at V_{AG}.

EpO, EARPIECE OUTPUT (PIN 15) – This output drives the handset earpiece which may require a series resistor to set the correct signal level. This output will be at V_{AG} when disabled.

MpI, MOUTHPIECE INPUT (PIN 16) – The mouthpiece microphone circuit is connected to this pin.

TxO, TRANSMIT OUTPUT (PIN 17) – This is the audio output pin of the device and is typically used to drive the TxI pin of a mono-circuit in digital telset applications.

DEVICE OPERATION

The telset audio interface IC consists of two major sections: an analog subsystem and a digital subsystem. The digital subsystem provides an interface to a microcomputer and generates the necessary control signals to configure the analog subsystem as desired.

ANALOG SUBSYSTEM

The analog subsystem provides the low-pass filtering, audio-signal routing, gain adjustment, and signal summing required for a digital or analog telset application. This subsystem consists of a receive and a transmit signal path.

RECEIVE SIGNAL PATH

The receive audio signal, typically from the RxO output of a PCM mono-circuit or a speech network, is input to the audio interface via the RxI pin. Once buffered into the device and passed through the low-pass filter, the audio signal has four possible destinations: earpiece output, speaker output, auxiliary output, or loopback to the TxO output.

The audio path to the earpiece output consists of an earpiece volume control and summing output amplifier. The volume control is an eight-step attenuation circuit with −3 dB steps and unity gain at the maximum setting. The steps are selected by a 3-bit binary code with 0_8 and 7_8, the minimum and maximum settings, respectively. The output of the earpiece volume control is summed (0 dB gain) with a sidetone (−17 dB gain) from the mouthpiece input. The earpiece output is capable of driving an earpiece transducer which typically requires 200 mVp-p into 150 ohms. The gain to the earpiece to attain the proper sound pressure level may be adjusted with a resistor in series with the earpiece. When the audio interface is configured such that the earpiece is not selected, the earpiece volume control and the summing output amplifier are powered down.

The audio path to the speaker output consists of a volume control and an output driver. The volume control is an eight-step attenuation circuit with −5 dB steps and unity gain at the maximum setting. The steps are selected by a 3-bit binary code with 0_8 and 7_8, the minimum and maximum settings, respectively. The binary code may be from either of two volume registers: the speaker volume register, selected when the speaker is used for voice, or the ringer volume register, selected when the speaker is used for ringing. The register used is determined by the current configuration of the audio interface. The output of the volume control is fed into a unity gain output buffer which is intended to drive a speaker power amplifier. The speaker/ringer volume control and output buffer power down when not selected.

The auxiliary output is similar to the speaker output and is powered down when not needed. This output can be used to drive a conference phone circuit or the receive portion of a modem.

The three analog outputs, EpO, SO, and AxO, have a transient suppression circuit which eliminates the possibility of acoustic "pops" during configuration or volume changes. This same circuit keeps the output at V_{AG} when it is not selected. When enabled, the output signal slews directly from V_{AG} to the audio signal.

The other possible destination for the receive audio is the TxO audio output. This is an audio loopback configuration

which allows a system to test the operation of the audio path in the telset. In the loopback configuration, the output of the ringer/speaker volume control is switched into the TxO output amplifier input.

TRANSMIT SIGNAL PATH

The transmit portion of the analog subsystem consists of a unity gain output driver which has three possible inputs. The input selection depends upon the current configuration of the audio interface. One of these inputs is used in the loopback configuration discussed above. The auxiliary inputs, AxF and – Ax, allow gain adjustment from an auxiliary circuit, and the third input, Mpl, is from the mouthpiece microphone and is amplified 20 dB by the input amplifier. Two configurations allow use of the auxiliary inputs as a mouthpiece input without sidetone, which is useful in analog telset applications.

3

DIGITAL SUBSYSTEM

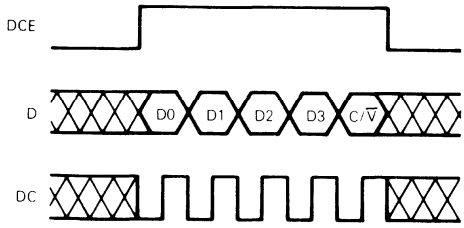
The digital subsystem provides a three-wire serial input which allows a microcomputer to program the audio configuration of the audio interface.

Data is clocked into the audio interface using the DCE, DC, and D pins. DCE going high enables the data input circuitry. While DCE is high, data appearing on the D pin is clocked into the serial input data register on rising edges of DC. The falling edge of DCE latches the serial data into the appropriate register.

The serial data input format consists of five bits as shown in Figure 2.

Configuration/$\overline{\text{Volume}}$ bit (C/$\overline{\text{V}}$), loaded last, indicates the type of data contained in the data field D0-D3. When C/$\overline{\text{V}}$ is a "1", the data indicates the device configuration to be established. When C/$\overline{\text{V}}$ is a "0", the data indicates a volume level. The volume control which receives the data depends upon the current configuration of the audio interface.

FIGURE 2 – DATA FORMAT



When C/$\overline{\text{V}}$ is "1", D0-D3 are loaded into the configuration register. The four configuration register bits then address a ROM which has outputs to control the analog subsystem elements, enable the appropriate volume register, select the appropriate volume register for the speaker/ringer volume control, and provide the SAE output.

When C/$\overline{\text{V}}$ is "0", the data bits D1-D3 are loaded into the volume register which has been selected by the ROM. For volume changes, only D1-C/$\overline{\text{V}}$ need be transferred. However, if five bits are loaded into the serial input data register and C/$\overline{\text{V}}$ is low, D0 will be ignored.

If six or more data bits are clocked in while DCE is high, the last five bits clocked will be accepted when DCE goes low.

The digital input SCI is used by the analog subsystem as a sampling clock for signal processing and by the data input circuitry as a sequencing clock during data transfers.

The $\overline{\text{PDI}}$ input, when low, powers down the analog subsystem; however, all data is retained in the data registers and data may still be loaded into the serial input data register as usual as long as SCI is present. An internal pull-down resistor to V_{SS} is connected to $\overline{\text{PDI}}$ to insure the power-down state upon application to V_{DD} and V_{SS}.

The five digital inputs are DCE, DC, D, SCI and PDI. After one logic transition change, the input logic determines which of the three possible input voltage swings is used, and responds accordingly to future input levels.

There are two input logic circuits per input pin. The first operates from V_{DG} to V_{DD} with TTL levels referenced from V_{DG}. The second circuit uses V_{DG} as the positive supply and V_{SS} as the negative, sensing CMOS input levels from V_{SS} to V_{DG}. The internal logic looks at the output of these two circuits and determines the input logic levels used. This permits logic level swings of V_{SS} to V_{DG}, V_{DG} to V_{DD}, or V_{SS} to V_{DD}.

CONFIGURATION MODES

The audio interface configuration set provides a total of 16 possible configurations. A description of each of the modes follows.

LOOPBACK

This is a system test mode which loops received audio through the ringer/system volume control and out the TxO output amp.

The ring volume register controls the ringer/speaker volume control and new volume data enters the same register.

STANDBY

This mode accomplishes the same result as the $\overline{\text{PDI}}$ pin except for powering down the TxO amplifier. All other amplifiers are powered down and all transmission gates are turned off. Volume data is latched into the ring volume register.

STANDARD A

The standard A mode resembles that of the ordinary telephone. Rxl audio is passed through the earpiece volume control and summed with a sidetone from the mouthpiece before being presented to the earpiece. Tx audio originates at the mouthpiece input, receives 20 dB of gain, and is then passed to the TxO output. New volume data is stored in the earpiece volume register. Transmit mute in this mode disable the path from the mouthpiece amplifier to the TxO amplifier.

RING

This is a receive only mode in which the receive audio is passed through the ringer/speaker volume control and output via the SO output. The ring volume register is selected to properly attenuate the ringing signal in the ringer/speaker volume control and any new volume data is written into the same register. Transmit mute has no effect in this mode and SAE goes high.

ON HOOK DIALING

This mode will allow a user to dial without taking the handset off hook. Audible feedback from the speaker could indicate dial tone, key depressions, etc. Receive audio passes through the ringer/speaker volume control and out the SO output. The transmit signal will originate at the auxiliary input which could be used for a DTMF dialer input. The speaker volume register is applied to the volume control and new volume data is latched into the same register. Mute will disable the transmit path from the auxiliary input. SAE will be high in this mode, enabling the speaker amplifier.

RECEIVER MONITOR A

This mode is similar to the standard A mode except the receive audio is also applied to the speaker output. Receive audio passes through both volume controls and out the EpO and SO pins. The speaker volume register controls the ringer/speaker volume control and new volume data is written into the speaker volume register. Transmit audio is taken from the mouthpiece input and output via the TxO amplifier. Transmit mute disables and mouthpiece amp to TxO amp path. SAE is high, enabling the speaker amplifier.

AUXILIARY

A suggested application for this mode would be for an optional conference phone circuit to be connected to the auxiliary input and output pins. Basically, a conference phone is a voice activated half-duplex controller which allows hands free conversation without audio feedback problems. Another useful application would be to connect a modem to the auxiliary input and output, thus eliminating the requirement for several components. In this mode the receive audio is passed through the ringer/speaker volume control and out the AxO pin. The SAE pin goes high, enabling the speaker amplifier. The transmit audio enters the audio interface via the auxiliary input amplifier and is connected directly to the TxO output amp. The speaker volume register controls the volume control and new volume data enters the same register. Transmit mute disables AxF from the input to the TxO output amp, disables AxO and enables the SO output.

STANDARD B

This mode is identical to the Standard A mode with one exception: the TxO signal originates at the auxiliary input instead of Mpl. This allows use of the Telset Audio Interface in applications that generate sidetone in a speech network. Mute disables the transmit path from the auxiliary input.

RECEIVE MONITOR B

This mode is identical to the Receive Monitor A mode with the same exception as the Standard B mode described above.

MODE AND VOLUME CONTROL

The data patterns required to program the audio interface mode or set the volume levels are summarized in Figures 3 and 4.

FIGURE 3 – MODE CONTROL SUMMARY

Mode	C/$\overline{V}$	D3	D2	D1	D0	Volume Register Selected	SAE State
Loopback	1	0	0	0	0	Ring	0
Standby	1	0	0	0	1	Ring	0
Standard A	1	0	0	1	0	Earpiece	0
Standard A/Mute	1	0	0	1	1	Earpiece	0
Ring	1	0	1	0	0	Ring	1
Ring/Mute	1	0	1	0	1	Ring	1
On-Hook Dialing	1	0	1	1	0	Speaker	1
On-Hook Dialing/Mute	1	0	1	1	1	Speaker	1
Receive Monitor A	1	1	0	0	0	Speaker	1
Receiver Monitor A/Mute	1	1	0	0	1	Speaker	1
Auxiliary	1	1	0	1	0	Speaker	1
Auxiliary/Mute	1	1	0	1	1	Speaker	1
Standard B	1	1	1	0	0	Earpiece	0
Standard B/Mute	1	1	1	0	1	Earpiece	0
Receive Monitor B	1	1	1	1	0	Speaker	1
Receive Monitor B/Mute	1	1	1	1	1	Speaker	1

FIGURE 4 – VOLUME CONTROL SUMMARY

Attenuation (dB)						
Earpiece	Speaker/ Ringer	C/$\overline{V}$	D3	D2	D1	D0
0	0	0	1	1	1	X
3	5	0	1	1	0	X
6	10	0	1	0	1	X
9	15	0	1	0	0	X
12	20	0	0	1	1	X
15	25	0	0	1	0	X
18	30	0	0	0	1	X
21	35	0	0	0	0	X

X = Don't Care

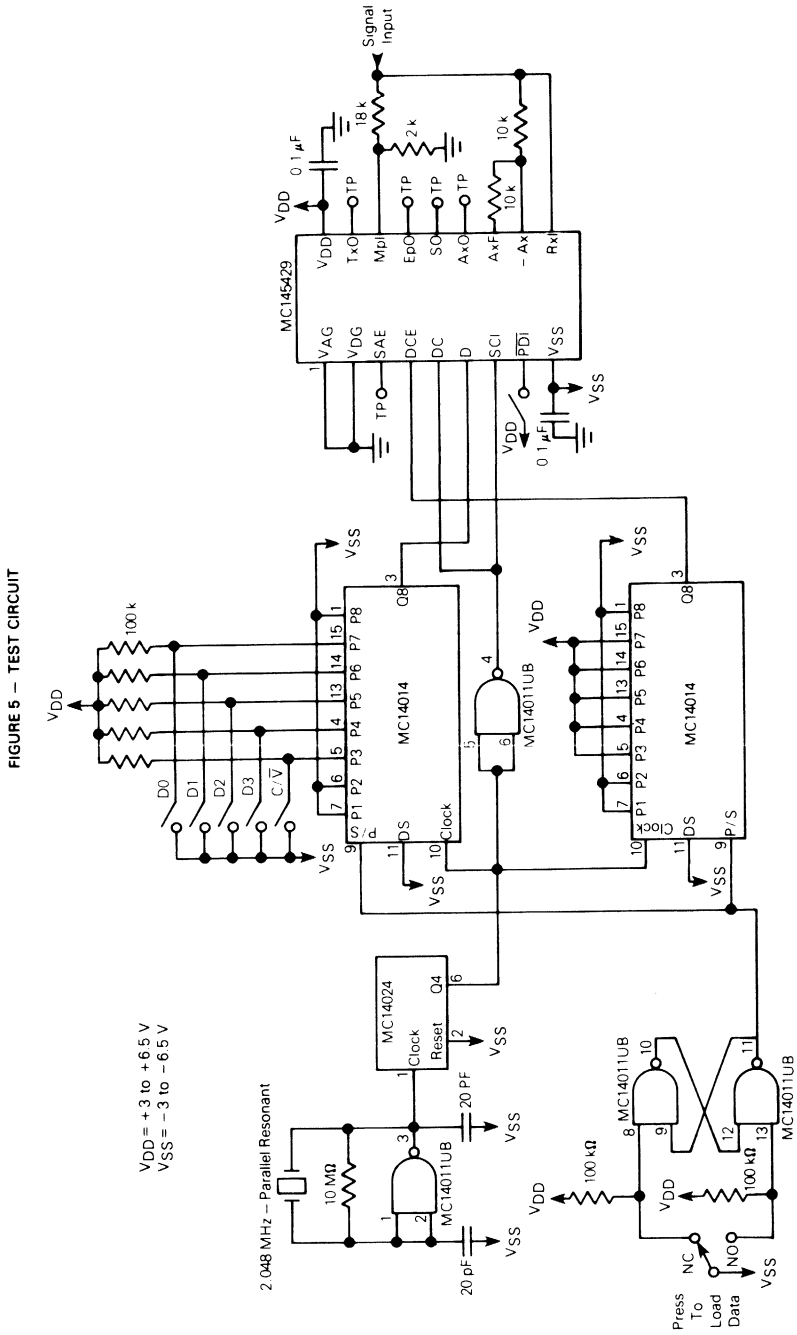


FIGURE 5 – TEST CIRCUIT

3

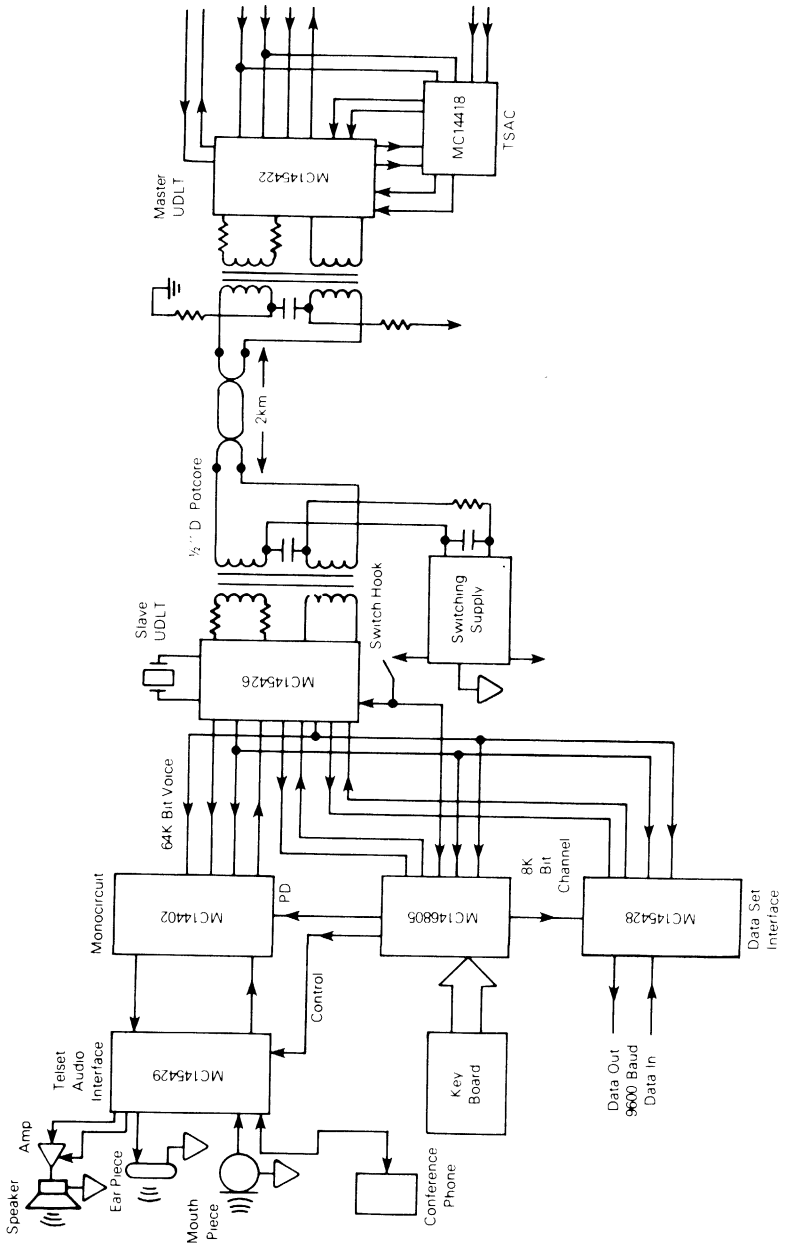


FIGURE 6 – DIGITAL WORK STATION

MOTOROLA

MC145432

Advance Information

CMOS
(LOW POWER COMPLEMENTARY MOS)

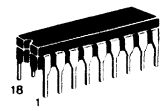
2600 Hz TONE SIGNALLING FILTER

3

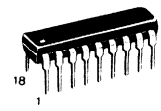
2600 Hz SF FILTER

This device contains a bypassable 6 pole 2600 Hz notch filter, a 2600 Hz band-pass filter and a 2600 Hz sinewave generator for SF signalling/detection applications.

- ± 5 V to ± 8 V Single or Split Supply Operation
- Low Power Consumption, 80 mW @ 10 V
  200 mW @ 15 V
- On-Board Crystal Oscillator or External Clocks
- Notch Filter Gain Adjustable
- Uncommitted Op Amp Capable of Driving 600 Ω Loads
- TTL or CMOS Compatible Inputs
- 18 Pin Package

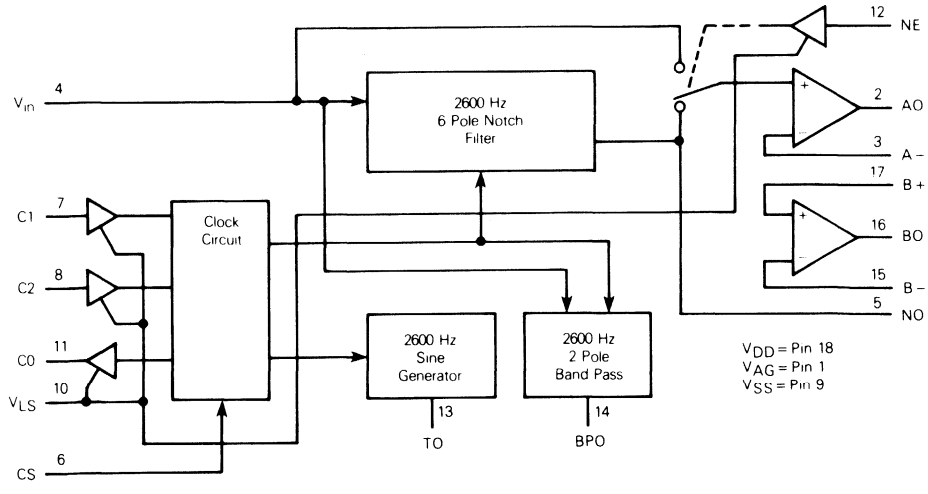


L SUFFIX
CERAMIC PACKAGE
CASE 726



P SUFFIX
PLASTIC PACKAGE
CASE 707

BLOCK DIAGRAM



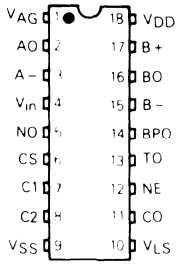
This document contains information on a new product. Specifications and information herein are subject to change without notice.

ADI966

MAXIMUM RATINGS (V_{SS} = 0 V)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	− 0.5 to 18	V
Input Voltage, All Pins	V_{in}	− 0.5 to V_{DD} + 0.5	V
DC Current Drain Per Pin (Not V_{DD} or V_{SS})	I	10	mA
Operating Temperature Range	T_A	− 40 to 85	°C
Storage Temperature Range	T_{stg}	− 65 to 150	°C

PIN ASSIGNMENT



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	$V_{DD} - V_{SS}$	9.5	15	16	V

3

DIGITAL ELECTRICAL CHARACTERISTICS (V_{SS} = 0 V, V_{DD} = 10 V, T_A = − 40 to 85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Operating Current (CMOS Mode) @ 2.048 MHz		I_{DD}	–	8.0	10	mA
(TTL Mode) @ 2.048 MHz			–	12	15	
Input Capacitance		Cin	–	5.0	7.5	pF
MODE CONTROL LOGIC LEVELS						
V_{LS} (TTL Mode)		–	V_{SS}	–	V_{DD} − 4	V
V_{LS} (CMOS Mode)		V_{IH}	V_{DD} − 0.5	–	V_{DD}	V
Clock Select (CS), $V_{AG} = (V_{DD} - V_{SS})/2$	State 1	V_{IH}	V_{DD} − 0.5	–	V_{DD}	V
	State 2	V_{IM}	V_{AG} − 0.5	–	V_{AG} + 0.5	
	State 3	V_{IL}	V_{SS}		V_{SS} + 0.5	
TTL LOGIC LEVELS (V_{LS} = 0 V, V_{SS} = 0 V)						
Input Current (C1, C2, CS, NE)	"1" Level	I_{IH}	–	–	± 0.3	μA
	"0" Level	I_{IL}	–	–	± 0.3	
Input Voltage (C1, C2, CS, NE)	"1" Level	V_{IH}	V_{LS} + 2.0	–	–	V
	"0" Level	V_{IL}	–	–	V_{LS} + 0.8	
Output Voltage (CO) I_O = 8 mA	"1" Level	V_{OH}	2.4	–		V
I_O = 2.5 mA	"0" Level	V_{OL}	–	–	0.8	
CMOS LOGIC LEVELS ($V_{LS} = V_{DD}$, V_{SS} = 0 V)						
Input Current (C1, C2, CS, NE)	"1" Level	I_{IH}	–	–	± 0.3	μA
	"0" Level	I_{IL}	–	–	± 0.3	
Input Voltage (C1, C2, CS, NE)	"1" Level	V_{IH}	7.5	5.6	–	V
	"0" Level	V_{IL}	–	4.4	3.0	
Output Current (CO)	V_{OH} = 9.5 V	I_{OH}	− 1.3	− 2.25	–	mA
	V_{OL} = 0.5 V	I_{OL}	1.1	2.25	–	

ANALOG ELECTRICAL CHARACTERISTICS (V_{DD} = 10 V, V_{AG} = V_{DD}/2, V_{SS} = 0 V, T_A = 0 to 70°C)

Characteristic		Symbol	Min	Typ	Max	Unit
DC Input Current (V_{AG})		I_I	–	–	± 50	μA
DC Input Current (V_{in})		I_I	–	–	± 10	μA
AC Input Impedance (1 kHz) (V_{in})		Z_{in}	0 2	0 1		MΩ
Input Voltage Range (V_{in})		V_{in}	V_{SS} + 1 5	–	V_{DD} 1 5	V
Output Drive Current (TO, BPO, NO)	V_{OH} = V_{DD} – 1 2 V V_{OL} = V_{SS} + 1 2 V	I_{OH} I_{OL}	– 0 4 + 0 9	–	–	mA

OP AMP PERFORMANCE (V_{DD} = 10 V, V_{AG} = V_{DD}/2, V_{SS} = 0 V, NE = V_{SS}, V_{LS} = V_{DD}, T_A = 0 to 70°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Offset Voltage (AO, BO)		V_{IO}	– 50		+ 50	MV
Open Loop Gain (AO, BO)	Z_L = 600 Ω + 200 pF to V_{AG}	A_{OL}	–	45		dB
Input Bias Current (V_{in}, A –, B –, B +)		I_{IB}	–	± 0 1	–	μA
Output Voltage Range (AO, BO) (R_L = 20 kΩ to V_{AG}) (R_L = 900 Ω to V_{AG}) (R_L = 600 Ω to V_{AG})		V_O	 1 0 1 1 1 8	 – – –	 9 0 8 9 8 2	V
Output Current (AO, BO)	V_{OH} = V_{DD} – 1 2 V VOL = V_{SS} + 1 2 V	I_{OH} I_{OL}	– 5 + 5	– –	– –	mA
Output Noise (AO, BO), 900 Ω		P_N	–	3	–	dBrnc
Slew Rate (AO, BO)		S_R	–	2	–	V/μs

NOTCH FILTER CHARACTERISTICS (V_{DD} = 10 V, V_{AG} = V_{DD}/2, CS = V_{SS} = 0 V, T_A = 0 to 70°C, NE = V_{DD})

Characteristics	Min	Max	Unit
Input Overload Voltage	–	7 0	Vpp
Gain (+ 2 dBm into 900 Ω @ 1 kHz)	– 0 5	+ 0 5	dB
Idle Noise, V_{in} = V_{AG}, 900 Ω	–	25	dBrnC
Pass-Band Gain, Ref. 1 kHz Note Figure 1 300 Hz to 2 kHz 2 kHz to 2 2 kHz 2 2 kHz to 2 4 kHz 2 8 kHz to 3 kHz 3 kHz to 3 38 kHz 3 38 kHz to 4 kHz	 – 0 25 – 0 5 – 5 0 – 5 0 – 0 5 – 0 5	 + 0 25 + 0 5 + 0 5 + 0 5 + 0 5 + 0 5	dB
Rejection, Ref. 1 kHz 2 58 kHz to 2 59 kHz 2 59 kHz to 2 61 kHz 2 61 kHz to 2 62 kHz	 – 45 – 55 – 45	 – – –	dB
Output Offset	– 500	+ 500	mV

BY-PASS CHARACTERISTICS (V_{in} to AO, NE Low, V_{DD} = 10 V, V_{AG} = V_{DD}/2, CS = V_{SS} = 0, T_A = 0 to 70°C)

Characteristics	Min	Max	Unit
Gain, 400 Hz to 4 kHz	−0.1	+0.1	dB
Noise, V_{in} = V_{AG}, 900 Ω	–	23	dBrnC
Output Offset	−50	+50	mV

BAND-PASS CHARACTERISTICS (V_{DD} = 10 V, V_{AG} = V_{DD}/2, CS = V_{SS} = 0, T_A = 0 to 70°C)

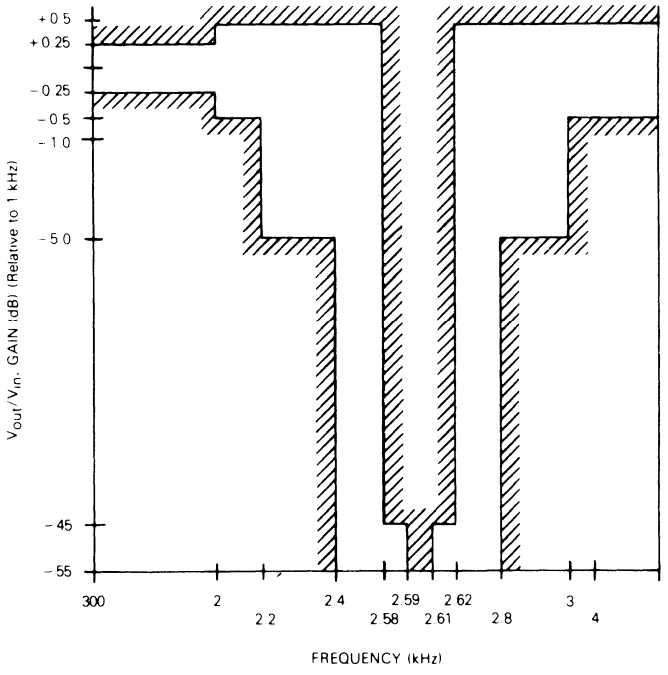
Characteristics	Min	Max	Unit
Center Frequency, f_0	2590	2610	Hz
Q	20	23	–
Gain (+2 dBm into 900 Ω @ 2.6 kHz)	−0.5	+0.5	dB
Idle Noise, V_{in} = V_{AG}, 900 Ω	–	45	dBrnC
Output Offset	−500	+500	mV

3

TONE OUT CHARACTERISTICS (V_{DD} = 10 V, V_{AG}/2, CS = V_{SS} = 0, T_A = 0 to 70°C)

Characteristics	Min	Max	Unit
Center Frequency	2598	2602	Hz
Output Level	0.40	0.725	Vp-p
Output Offset	−300	+300	mV

FIGURE 1 — NOTCH RESPONSE PARAMETER



PIN DESCRIPTIONS

V_{DD}, POSITIVE POWER SUPPLY (PIN 18)

Most positive supply.

V_{SS}, NEGATIVE POWER SUPPLY (PIN 9)

Most negative supply.

V_{AG}, ANALOG GROUND (PIN 1)

This pin is a high impedance input which serves as analog ground reference. This pin is nominally held at $(V_{DD} - V_{SS})/2$.

AO, OP-AMP OUT (PIN 2)
A−, OP-AMP IN (PIN 3)

These pins are for the output buffer amp which is capable of driving 600 Ω loads. A− is the inverting input of this amp while AO is its output. This amp buffers either the output of the notch filter or the input signal at V_{in} depending on the state of the NE pin.

V_{in}, INPUT (PIN 4)

This pin is the input to the notch filter, band-pass filter, and notch by-pass switch.

NO, NOTCH OUTPUT (PIN 5)

This pin is the output of the notch filter and can drive 20 kΩ loads.

NE, NOTCH ENABLE (PIN 12)

When high (see V_{LS} pin) the notch filter output is applied to the line buffer output amp. When held low (see V_{LS} pin) the input at V_{in} is applied to this op amp.

TO, TONE OUTPUT (PIN 13)

A 2600 Hz sine wave is output at this pin. This pin can drive a 20 kΩ load.

BPO, BAND-PASS OUT (PIN 14)

This pin is the output of the 2600 Hz band-pass filter and can drive a 20 kΩ load.

B+, OP-AMP NONINVERTING INPUT (PIN 17)

This pin is the noninverting input to the uncommitted op-amp provided on the circuit.

B−, OP-AMP INVERTING INPUT (PIN 15)

This pin is the inverting input of the uncommitted op-amp provided on the circuit.

BO, OP-AMP OUTPUT (PIN 16)

This pin is the inverting input of the uncommitted op-amp provided on the circuit.

CS, CLOCK SELECT (PIN 6)
C1, C2, CLOCK INPUTS (PINS 7 AND 8)

When held at V_{DD}, CS selects the internal crystal oscillator clock mode. A 3.579545 MHz crystal is connected between pins C1 and C2. A 10 MΩ resistor should be tied across C1 and C2 along with 20 pF capacitors to V_{SS} to insure stable oscillator operation. When tied to V_{SS}, a 2.048 MHz external clock should be applied to C2. When tied to V_{AG}, a 1.536 MHz external clock should be applied to C2. In both external clock modes, C1 should be tied to V_{SS}.

V_{LS}, LOGIC SHIFT VOLTAGE (PIN 10)

This pin determines CMOS or TTL level compatibility for C1, C2, NE and CO. If tied to V_{DD}, CMOS device levels are expected; if tied to a voltage less than $V_{DD} - 4$ V, TTL levels are expected with V_{LS} equal to logic ground.

CO, CLOCK OUTPUT (PIN 11)

A 128 kHz square wave is available at this pin. This is the sample clock of both the notch and band-pass filters.

FIGURE 2 — FUNCTIONAL TRUTH TABLE

Clock Select (CS)	Source	Frequency	CO	Tone Out (TO)
V_{DD}	Crystal (C1, C2)	3.579 MHz	127.8 kHz	2601 Hz
V_{AG}	External (C1 = V_{SS})	1.536 MHz	128 kHz	2603.4 Hz
V_{SS}	External (C1 = V_{SS})	2.048 MHz	128 kHz	2599 Hz

FIGURE 3 — TEST CIRCUIT

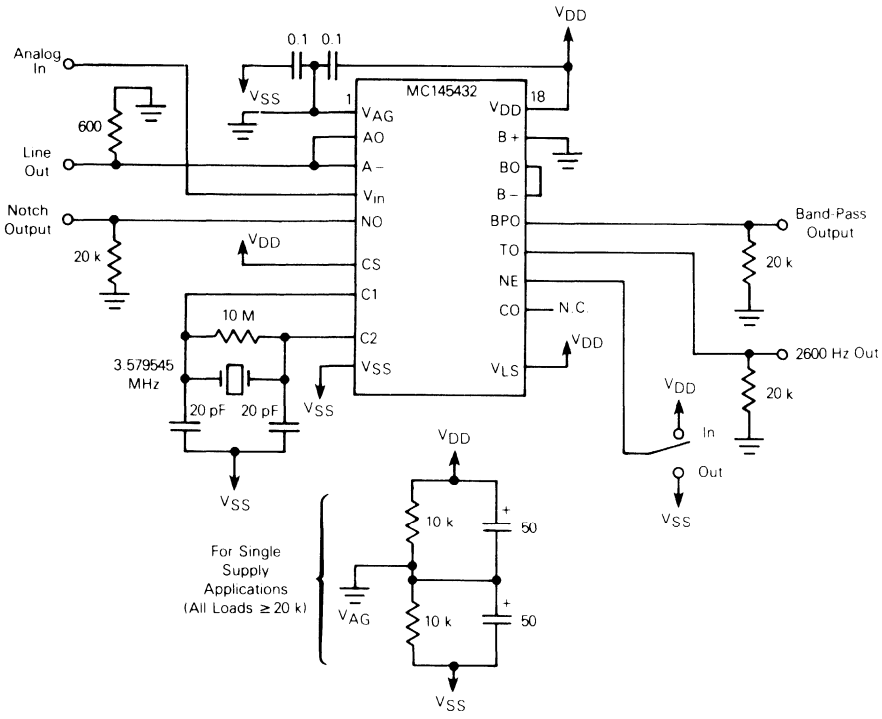
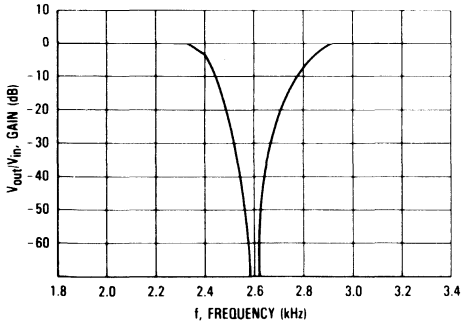
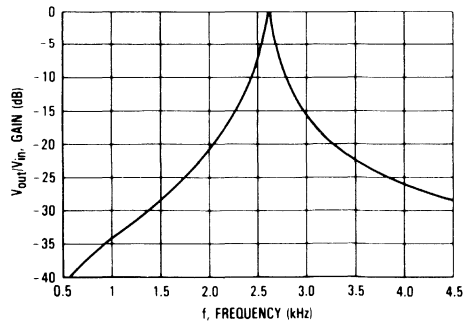


FIGURE 4 — TYPICAL RESPONSE CURVES

NOTCH FREQUENCY RESPONSE



BAND-PASS FREQUENCY RESPONSE



MOTOROLA

MC145433

Advance Information

CMOS
(LOW-POWER COMPLEMENTARY MOS)

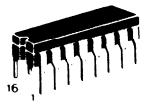
TUNEABLE NOTCH/ BAND-PASS FILTER

3

NOTCH/BAND-PASS FILTERS

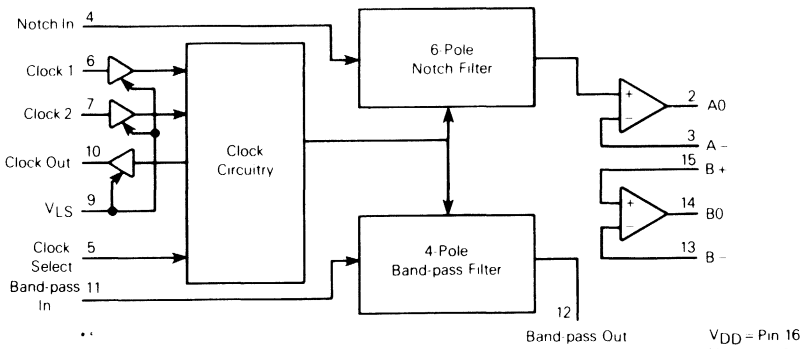
This device contains a 6-pole filter and 4-pole band-pass filter.

- ±5 to ±8 V Supply Operation
- Low Power Consumption, 150 mW Typical
- Tuneable Notch and Band-pass Filters
- On-board Crystal Oscillator or External Clocks
- Clock Output Pin
- An Uncommitted Op-Amp Is Provided, Capable of Driving 600 Ω Loads
- Notch Filter Output Gain Adjustable
- TTL or CMOS Compatible Inputs
- 16-Pin Package



L SUFFIX
CERAMIC PACKAGE
CASE 620

BLOCK DIAGRAM



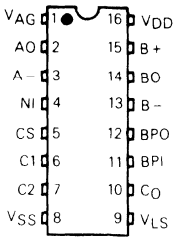
This document contains information on a new product. Specifications and information herein are subject to change without notice.

ADI1030

MAXIMUM RATINGS (V_{SS} = 0 V)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to 18	V
Input Voltage, All Pins	V_{in}	−0.5 to V_{DD} + 0.5	V
DC Current Drain Per Pin (Not V_{DD} or V_{SS})	I	10	mA
Operating Temperature Range	T_A	−40 to 85	°C
Storage Temperature Range	T_{stg}	−65 to 150	°C

PIN ASSIGNMENT



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	$V_{DD} - V_{SS}$	9.5	15	16	V

3

DIGITAL ELECTRICAL CHARACTERISTICS (V_{SS} = 0 V, V_{DD} = 10 V, T_A = −40 to 85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Operating Current (CMOS Mode) @ 2.048 MHz		I_{DD}	–	10	18	mA
(TTL Mode) @ 2.048 MHz			–	15	22	
Input Capacitance		Cin	–	5.0	7.5	pF
MODE CONTROL LOGIC LEVELS						
V_{LS} (TTL Mode)		–	V_{SS}	–	V_{DD} − 4	V
V_{LS} (CMOS Mode)		V_{IH}	V_{DD} − 0.5	–	V_{DD}	V
Clock Select (CS), $V_{AG} = (V_{DD} - V_{SS})/2$	State 1	V_{IH}	V_{DD} − 0.5	–	V_{DD}	V
	State 2	V_{IM}	V_{AG} − 0.5	–	V_{AG} + 0.5	
	State 3	V_{IL}	V_{SS}	–	V_{SS} + 0.5	
TTL LOGIC LEVELS (V_{LS} = 0 V, V_{SS} = 0 V)						
Input Current (C1, C2, CS)	"1" Level	I_{IH}	–	–	±0.3	μA
	"0" Level	I_{IL}	–	–	±0.3	
Input Voltage (C1, C2, CS)	"1" Level	V_{IH}	V_{LS} + 2.0	–	–	V
	"0" Level	V_{IL}	–	–	V_{LS} + 0.8	
Output Voltage (CO) I_O = 8 mA	"1" Level	V_{OH}	2.4	–	–	V
I_O = 2.5 mA	"0" Level	V_{OL}	–	–	0.8	
CMOS LOGIC LEVELS ($V_{LS} = V_{DD}$, V_{SS} = 0 V)						
Input Current (C1, C2, CS)	"1" Level	I_{IH}	–	–	±0.3	μA
	"0" Level	I_{IL}	–	–	±0.3	
Input Voltage (C1, C2, CS)	"1" Level	V_{IH}	7.5	5.6	–	V
	"0" Level	V_{IL}	–	4.4	3.0	
Output Current (CO)	V_{OH} = 9.5 V	I_{OH}	−1.3	−2.25	–	mA
	V_{OL} = 0.5 V	I_{OL}	1.1	2.25	–	

ANALOG ELECTRICAL CHARACTERISTICS (V_{DD} = 10 V, V_{AG} = V_{DD}/2, V_{SS} = 0 V, T_A = 0 to 85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
DC Input Current (V_{AG})		I_I	–	–	± 75	μA
DC Input Current (NI and BPI)		I_I	–	–	± 10	μA
AC Input Impedance (1 kHz) (NI and BPI)		Z_{in}	0 2	0 1		MΩ
Input Voltage Range (NI and BPI)		V_{in}	V_{SS} + 1 5	–	V_{DD} – 1 5	V
Output Drive Current (BPO)	V_{OH} = V_{DD} – 1 2 V V_{OL} = V_{SS} + 1 2 V	I_{OH} I_{OL}	– 0 4 + 0 9	–	–	mA

OP AMP PERFORMANCE (V_{DD} = 10 V, V_{AG} = V_{DD}/2, V_{SS} = 0 V, V_{LS} = V_{DD}, T_A = 0 to 85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Offset Voltage (BO)		V_{IO}	– 50	–	+ 50	MV
Open Loop Gain (BO)	Z_L = 600 Ω + 200 pF to V_{AG}	A_{OL}	–	45	–	dB
Input Bias Current (A –, B –, B +)		I_{IB}	–	± 0 1	–	μA
Output Voltage Range (BO) (R_L = 20 kΩ to V_{AG}) (R_L = 900 Ω to V_{AG}) (R_L = 600 Ω to V_{AG})		V_O	 1 0 1 1 1 8	 – – –	 9 0 8 9 8 2	V
Output Current (BO)	V_{OH} = V_{DD} – 1 2 V VOL = V_{SS} + 1 2 V	I_{OH} I_{OL}	– 5 + 5	–	–	mA
Output Noise (BO), 900 Ω		P_N	–	– 3	–	dBrnC
Slew Rate (BO)		S_R	–	2	–	V/μs

NOTCH FILTER CHARACTERISTICS (V_{DD} = 10 V, V_{AG} = V_{DD}/2, CS = V_{SS} = 0 V, T_A = 0 to 85°C, BPI = V_{AG})

Characteristics	Min	Max	Unit
Input Overload Voltage	–	7 0	Vpp
Gain (+ 2 dBm into 900 Ω @ 1 kHz)	– 1 0	+ 1 0	dB
Idle Noise, NI = V_{AG}, R_L = 900 Ω	–	28	dBrnC
Pass-Band Gain, Ref 1 kHz (Note Figure 1) 300 Hz to 2 2 kHz 2 2 kHz to 2 4 kHz 2 8 kHz to 3 kHz 3 kHz to 4 kHz	 – 1 0 – 7 0 – 7 0 – 1 0	 + 1 0 + 1 0 + 1 0 + 1 0	dB
Rejection, Ref 1 kHz 2.58 kHz to 2.62 kHz	 – 45	 –	dB
Output Offset	– 750	+ 750	mV
Dynamic Range (VFS/Idle Noise)	– 70	–	dB

BAND—PASS FILTER ELECTRICAL CHARACTERISTICS (V_{DD} = 10 V, NI = V_{AG}, V_{AG} = V_{DD}/2, V_{SS} = 0 V, T_A = 0 to 85°C)

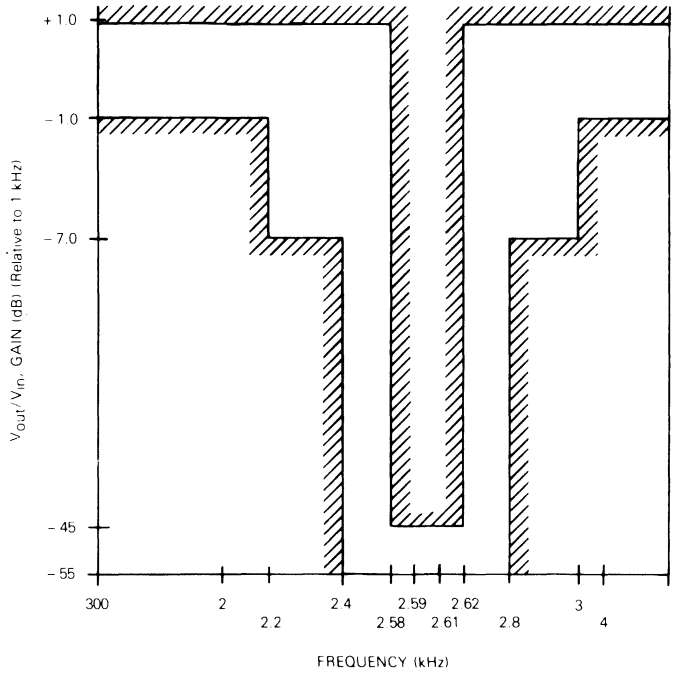
Characteristic*	Symbol	Min	Typ	Max	Unit
Full Scale Input Voltage (+3 dbm0)	V_{FS}	7	–	–	VPP
Gain (+2 dBm into 900 Ω @ 2.6 kHz	A_r	−1	0.0	+1	dB
Idle Noise, BPI = V_{AG}, R_L = 900 Ω	P_N	–	–	35	dBrnC
Dynamic Range (V_{FS}/Idle Noise)	DR	63	–	–	dB
Total Harmonic Distortion (0 dbm into 900 Ω)	THD	–	–	1.0	%
Output offset		−500	–	+500	mV
Q (−3db bandwidth/center frequency)	Q	28	–	38	–

DIGITAL SWITCHING CHARACTERISTICS (V_{DD} = 10 V, V_{SS} = 0, V_{AG} = V_{DD}/2 T_A = 0 to 85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Rise and Fall Times	C1, C2	t_r, t_f	–	–	1.5	μs
Input Pulse Width (TTL Mode)	C1, C2	t_w	200	–	–	ns
Clock Frequency (TTL Mode)	C1, C2	f_C	–	–	2.048	MHz
Clock Frequency (CMOS Mode)	C1, C2	f_C	–	–	6	MHz
Crystal Frequency	C1, C2	f_x	1	–	6	MHz
Input Pulse Width (CMOS Mode)	C1, C2	t_w	125	–	–	ns
Switching Frequency (Internal)		f_s	10	–	256	kHz

3

NOTCH RESPONSE PARAMETER



PIN DESCRIPTIONS

V_{DD} (PIN 16)
Most positive supply, nominally + 12 V to + 15 V.

V_{SS} (PIN 8)
Most negative supply, nominally 0 V.

V_{AG} (PIN 1)
Analog ground. This pin is a high impedance input which serves as analog ground reference. This pin is nominally held at $(V_{DD} - V_{SS})/2$.

CS, CLOCK SELECT (PIN 5)
This pin controls the configuration of the digital section of the circuit. Three different clock divide configurations can be obtained by tying this pin to either V_{DD}, V_{AG} or V_{SS}.

V_{LS}, LOGIC SHIFT VOLTAGE (PIN 9)
This determines the logic levels expected at the digital input C1 and C2. If tied to V_{DD}, CMOS logic levels are expected; if tied to a voltage less than $V_{DD} - 4$ V, TTL levels are expected with V_{LS} equal to logic ground. This pin also controls the output swing at pin CO in a similar manner, i.e., TTL or CMOS levels.

CO, CLOCK OUT (PIN 10)
This pin is the digital clock output pin. It is equal to the switching frequency, f_S of the notch and band-pass filters.

C1, C2, CLOCK 1, CLOCK 2 (PINS 6 AND 7)
When CS is tied to V_{DD}, a 1 to 4 MHz crystal is tied to C1 and C2. The switching frequency, f_S, of both filters is determined by the crystal frequency and is given by:

$$\frac{f_{crystal}}{28} = f_S$$

With CS tied to V_{AG}, an external clock frequency must be applied into C1 and C2 tied together. The switching frequency f_S for the notch and band-pass filters are equal to the external clock frequency divided by 16. When CS is tied to V_{SS}, operation is identical to that when tied to V_{AG}, except that the clock is divided by 1 instead of 16.

NI, NOTCH INPUT (PIN 4)
This pin is the analog input to the notch filter.

AO, OP-AMP OUT (PIN 2), A−, OP-AMP INOUT (PIN 3)
These pins are for the output buffer amp of the notch filter. A− is the inverting input of this amp while AO is its output. This op-amp is capable of driving a 600 ohm load.

B+, OP-AMP NONINVERTING INPUT (PIN 15)
This pin is the non inverting input to the uncommitted op-amp provided on chip.

B−, OP-AMP INVERTING INPUT (PIN 13)
This pin is the inverting input to the uncommitted op-amp.

BO, OP-AMP OUTPUT (PIN 14)
This pin is the output of this uncommitted op amp. This op-amp is capable of driving a 600 ohm load.

BPI, BAND-PASS IN (PIN 11)
This is the input to the band-pass filter.

BPO, BAND-PASS OUT (PIN 12)
This is the output of the band-pass filter.

FUNCTIONAL TRUTH TABLE

Clock Select CS	Clock	Filter Switching Frequency f_S	Notch/Bandpass Center Frequency f_C	Digital Clock Out CO
V_{DD}	Crystal	$\frac{\text{Clock (Hz)}}{28}$	$\frac{\text{Clock (Hz)}}{137.844}$	f_S
V_{AG}	External	$\frac{\text{Clock (Hz)}}{16}$	$\frac{\text{Clock (Hz)}}{787.69}$	f_S of Notch
V_{SS}	External	Clock (Hz)	$\frac{\text{Clock (Hz)}}{49.23}$	f_S of Notch

NOTE: Switching Frequency (f_S) Range = 10 kHz to 256 kHz

FIGURE 1 – TEST CIRCUIT

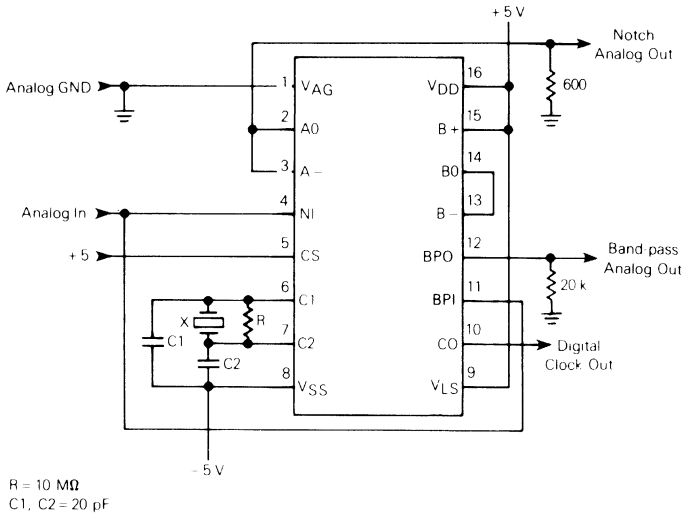


FIGURE 2 – TYPICAL NOTCH FILTER RESPONSE CURVES

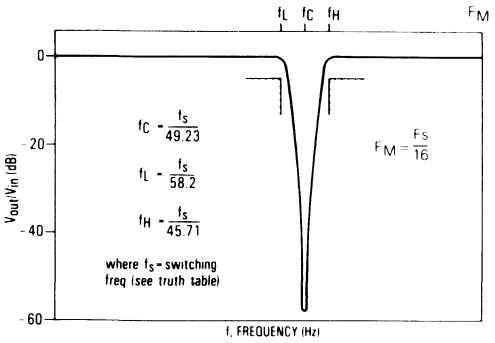
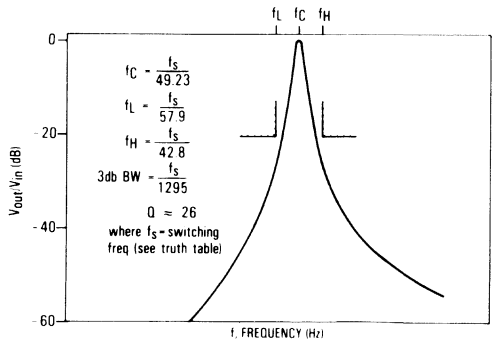
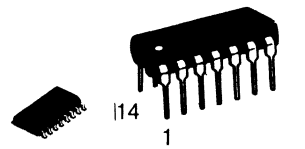


FIGURE 3 – TYPICAL BAND-PASS FILTER RESPONSE CURVES



MOTOROLA

MC145436

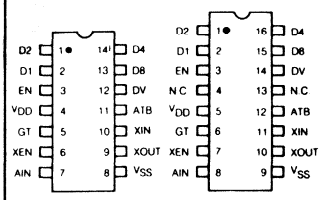


DW SUFFIX
CASE 751B—02
SOIC

P SUFFIX
PLASTIC
CASE 646—05

3

PIN ASSIGNMENT



P PACKAGE DW PACKAGE

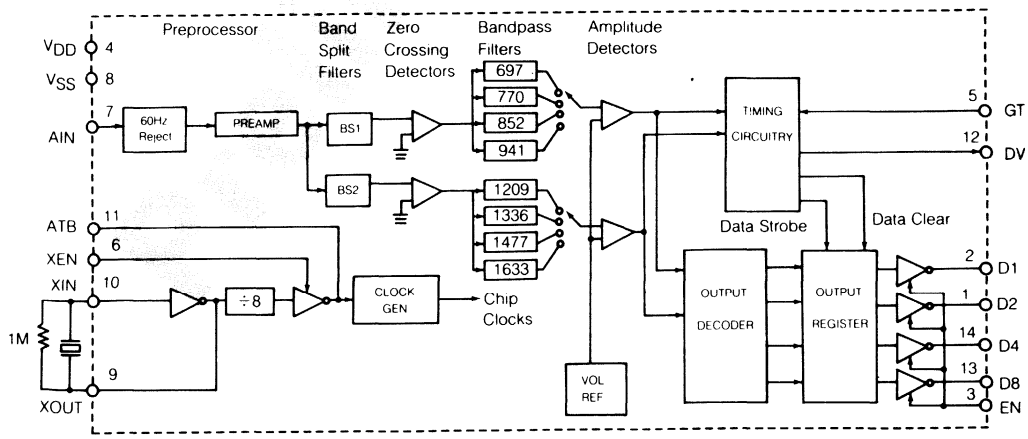
Advance Information

Dual Tone Multiple Frequency (DTMF) Receiver Silicon-Gate CMOS

The MC145436 is a CMOS LSI device containing the filter and decoder for detection of a pair of tones conforming to the DTMF standard with outputs in hexdecimal. Switched capacitor filter technology is used together with digital circuitry for the timing control and output circuits. The MC145436 provides excellent power line noise and dial tone rejection and is suitable for applications in central office equipments, PABX and keyphone system, remote control equipment and consumer telephony products.

- 5-Volt Supply
- Detects all 16 standard digits
- Uses inexpensive 3.58 MHz Crystal
- Provides Guard Time Control to improve Speech Immunity
- Output in 4-bit Hexadecimal Code

BLOCK DIAGRAM



This document contains information on a new product. Specification and information herein are subject to change without notice.

Pin Descriptions

V_{DD}, POSITIVE POWER SUPPLY (PIN4)
This is usually 5.0V.

V_{SS}, NEGATIVE POWER SUPPLY (PIN 8)
This is usually 0V.

D1; D2; D4; D8, DATA OUTPUT (PIN 2, 1, 14, 13)

These digital outputs provide the hexidecimal code corresponding to the detected digit. The digit outputs become valid after a tone pair has been detected and they are then cleared when a valid pause is timed. Table 1 describes the hexidecimal codes.

EN, ENABLE (PIN 3)

Outputs D1, D2, D4, and D8 are enabled when EN is at logical '1',and high impedanced when disabled by pulling EN low.

GT, GUARD TIME (PIN 5)

The Guard Time control input provides two sets of detect time and release time, both within the allowed ranges of tone-on and tone-off. A longer tone detect time rejects signals too short to be considered valid. Thus GT = 1 improves talk-off preformance, since it reduces the probability that tones simulated by speech will maintain signal condition long enough to be accepted. Also a shorter release time reduces the probability a pause to be interrupted by tones simulated by speech.

On the other hand, a shorter tone detect time with a long release time would be appropriate for extremely noisy environments where fast acquisition time and immunity to drop-outs would be required. In general practice, the tone signal duration generated by telephone is 100mS nominal and the pause time is also about 100mS.

A high-to-low or low-to-high transition on the GT input reset the internal logic of the device, after the reset, DV is low and the MC145436 is immediately ready to accept new DTMF tones.

XEN, OSCILLATOR ENABLE (PIN 6)

A "1" on XEN enables the on chip crystal oscillator, when using alternate time base from ATB pin, XEN should be tied to V_{SS}.

AIN, ANALOG IN (PIN 7)

This pin accepts the analog input. It is internally biased so that the input signal may be AC coupled. The input may be DC coupled as long as it does not exceed the positive supply. Proper input coupling is illustrated in Fig. 1

XIN, OSCILLATOR INPUT (PIN 10)
XOUT, OSCILLATOR OUTPUT (PIN 9)

These pins connect to an internal crystal oscillator. In operation, a parallel resonant crystal is connected from XIN to XOUT as well as a 1M Ω resistor in parallel with the crystal. When using alternate clock source from ATB pin, XIN should be tied to V_{DD}.

ATB, ALTERNATE TIME BASE (PIN 11)

This pin serves as frequency reference when more than one MC145436 is used, such that only one crystal is required for multiple MC145436. When doing so, all ATB pins should be tied together as shown in Fig. 2

When only one MC145436 is used, this pin should be left unconnected.

DV, DATA VALID (PIN 12)

DV signals a detection by going high after a valid tone pair is sensed and decoded at the output pins D1, D2, D4, D8. DV remains high until a valid pause occurs.

GENERAL DESCRIPTION

The MC145436 is an integrated DTMF receiver fabricated using advanced CMOS silicon gate technology. It contains all the analog signal processing circuits, switched capacitor bandpass filters and digital timing logic circuits. The MC145436 only requires a low cost 3.579 MHz crystal to make it a complete DTMF detection subsystem. The 3.579 MHz reference frequency is used to derive the sampling frequency for the internal switched capacitor filters and timing logic.

A DTMF tone pair, to be valid, should meet both the frequency and duration specifications.

The input signal at pin 7 is pre-processed by the high pass filter and the preamp filter in order to reject the dial tone (which is 350 Hz + 440 Hz) and bandlimit the signal below 6 KHz.

The signal is then separated into two bands by two band reject filters. One of the filters rejects the 697-941 Hz range of frequencies and the other rejects the 1209-1633 Hz range. By separating these two groups of frequencies, the interference to the band being detected will be reduced.

These two groups of signals are then converted to square wave by zero-crossing detectors, which are then passed to the band pass filters. The centre frequencies of these eight bandpass filters are designed to conform to the Bell standard as shown in Fig.3.

If the frequency of the signal coming from the zero crossing detectors is within bandwidth of any of the bandpass filters, the output from that bandpass filter will have an output level above the detect threshold of the amplitude detectors.

The logic and timing portion of the MC145436 will then determine whether a valid tone pair has been detected by the analog circuitry. If a valid tone pair is detected, it will have to present for a minimum duration of 40 ms before the Data Valid and Data Pins are activated.

3

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
DC Supply Voltage (Referenced to V_{SS})	V_{DD}	−0.5 to +6.0	V
Operating Temperature	T_A	0 to +70	℃
Storage Temperature	T_{stg}	−65 to +150	℃
DC Current Drain per pin	I	10	mA
Maximum Voltage (Any pin except AIN)	V_{in1}	$V_{SS}-0.5$ to $V_{DD}+0.5$	V
Maximum Voltage (AIN)	V_{in2}	$V_{DD}-10$ to $V_{DD}+0.5$	V

This device contains protection circuitry to guard against damage due to high static voltages or electric field. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range $V_{SS} \leq$ (Vin or Vout) $\leq V_{DD}$.

Unused inputs must always be tied to an appropriate voltage level (e. g., either V_{SS} or V_{DD}). Unused output must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{DD}	DC Supply Voltage (Referenced to V_{SS})	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage	0	V_{DD}	V
T_A	Operating Temperature	0	+70	℃

ELECTRICAL CHARACTERISTICS (V_{DD}=5V, T_A=25°C)

CHARACTERISTICS		SYMBOL	MIN.	TYP	MAX.	UNIT
OPERATING VOLTAGE		V_{DD}	4.5	5	5.5	V
INPUT VOLTAGE V_{out} =0.5V OR V_{DD} −0.5V	0 LEVEL	V_{IL}	—	—	1.5	V
	1 LEVEL	V_{IH}	3.5	—	—	V
OUTPUT CURRENT (D1, D2, D4, D8, DV, ATB) V_{out} =4.5V	SOURCE	I_{OH}	800	—	—	μA
V_{out} =0.5V	SINK	I_{OL}	1.5	—	—	mA
OPERATING CURRENT		I_{DD}	—	10	16	mA
INPUT IMPEDANCE−AIN		R_{in}	90	100	—	KΩ
INPUT CURRENT −GT		I_{in}	—	—	200	μA
INPUT CURRENT −ATB		I_{in}	—	—	20	μA
INPUT CURRENT−OTHER INPUT PINS		I_{in}	—	—	±1	μA
LEAKAGE CURRENT−DATA PINS (EN=V_{SS})		I_{LKG}	—	—	±1	μA

ANALOG CHARACTERISTICS (V_{DD}= 5V, T_A=25°C)

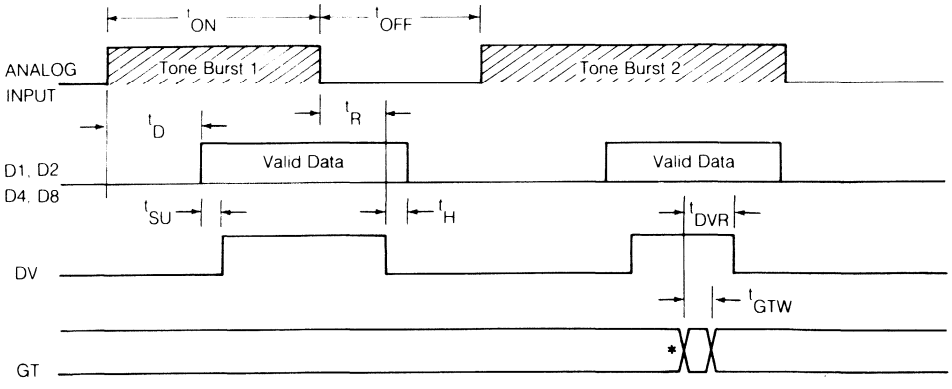
CHARACTERISTICS	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SIGNAL LEVEL FOR DETECTION (EACH TONE)		−32	—	−2	dBm(1)
TWIST ($=\frac{\text{HIGH TONE}}{\text{LOW TONE}}$)		±10	—	—	dB
FREQUENCY DETECT BANDWIDTH		$\pm(1.5+2H_Z)$	±2.5	±3.5	% of fo
60Hz TOLERANCE		—	—	0.8	Vrms
DIAL TONE TOLERANCE	Dial Tone Used: 330+440Hz	—	—	0	dB(2)
NOISE TOLERANCE (3)		—	—	−12	dB(2)
POWER SUPPLY NOISE	Wide Band	—	—	10	mV p-p
TALK OFF	MITEL tape #CM7290	—	2	—	hits

(1)OdBm referenced to lmW into a 600 ohm load
(2)Referenced to lower amplitude tone
(3)Bandwidth limited (0 to 3.4KHz) Gaussian Noise

AC CHARACTERISTICS

Parameter		Symbol	Min.	Typ.	Max.	Units
Tone On Time	: for detection for rejection	t_{ON}	40 —	— —	— 20	mS
Pause Time	: for detection for rejection	t_{OFF}	40 —	— —	— 20	mS
Detect Time	: GT=O GT=1	t_D	22 32	— —	40 50	mS
Release Time	: GT=0 GT=1	t_R	28 18	— —	40 30	mS
Data Setup Time		t_{SU}	7	—	—	μS
Data Hold Time		t_H	4.2	4.6	5.0	mS
GT Width		t_{GTW}	36	—	—	μS
DV Reset Lag Time		t_{DVR}	—	—	5.0	mS
OUTPUT ENABLE TIME CL=50pF R_L=1KΩ		—	—	200	—	nS
OUTPUT DISABLE TIME C_L=35pF R_L=500Ω		—	—	150	—	nS
OUTPUT RISE TIME C_L=50pF		—	—	200	—	nS
OUTPUT FALL TIME C_L=50pF		—	—	160	—	nS

TIMING



✱ NOTE: Can be rising or falling edge

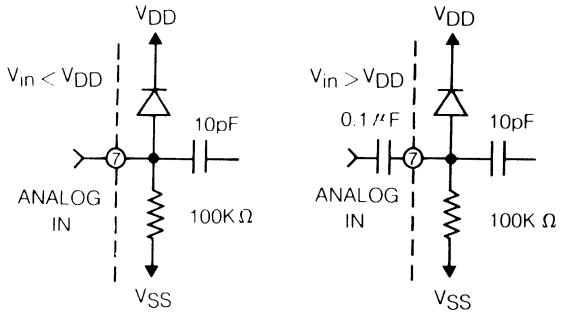


FIGURE 1. ANALOG INPUT PIN

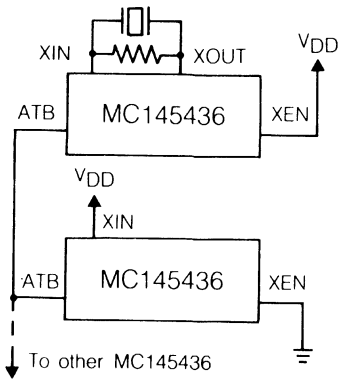


FIGURE 2. ATB CONNECTION

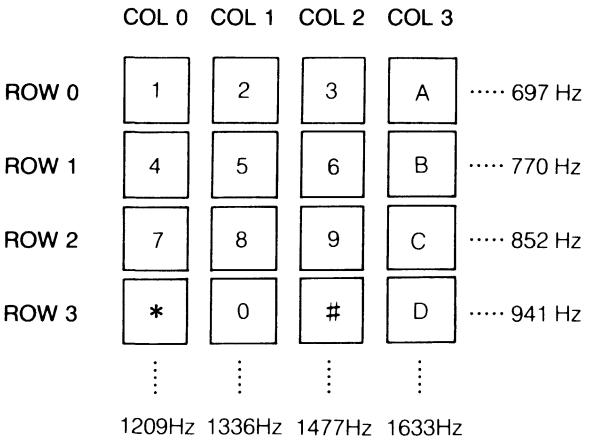


FIGURE 3. DTMF DIALING MATRIX

Digit	OUTPUT CODE D8	D4	D2	D1
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
0	1	0	1	0
*	1	0	1	1
#	1	1	0	0
A	1	1	0	1
B	1	1	1	0
C	1	1	1	1
D	0	0	0	0

TABIE 1. DTMF CODE

APPLICATION EXAMPLE

Historically DTMF receivers found their main application in central office or PABX type switching equipments, where they are used for decoding digits dialed by DTMF telephones, but the adoption of DTMF receivers in consumer telecom products is starting to increase.

Following the office and factory, the home will be the next area to be automated. Home automation includes functions such as home security, energy and finance management, tele-controller and tele-monitor. Among these areas, DTMF receivers will find application in tele-controller and monitor.

Using a tele-controller, a user away from his home can switch ON or OFF any of his appliances which are attached to the controller (see Fig. 4). The user activates the tele-controller by entering preset codes on a DTMF phone. If he wants to switch on any appliance, he can push ✳ and the appliance number. Similarly, he can switch off any appliance by entering # and the appliance number. These command tones would be first decoded by MC145436 and the MCU would then take appropriate actions. (Fig. 5 shows the block diagram of a simplified telecontroller).

To confirm the operation of the control functions, different tones will be sent back to the user by the telecontroller. The feedback can be a synthesised voice generated by the VMAC as in the case of an answer phone.

The user can also enter commands to monitor the security conditions of his house.

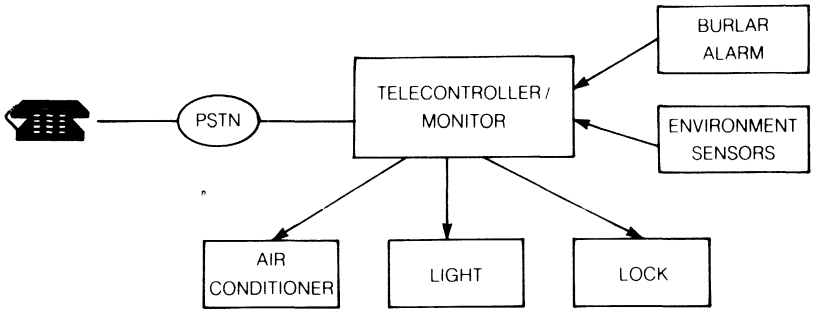


FIGURE 4. USING TELEPHONE NETWORK AS MEDIA FOR REMOTE CONTROL

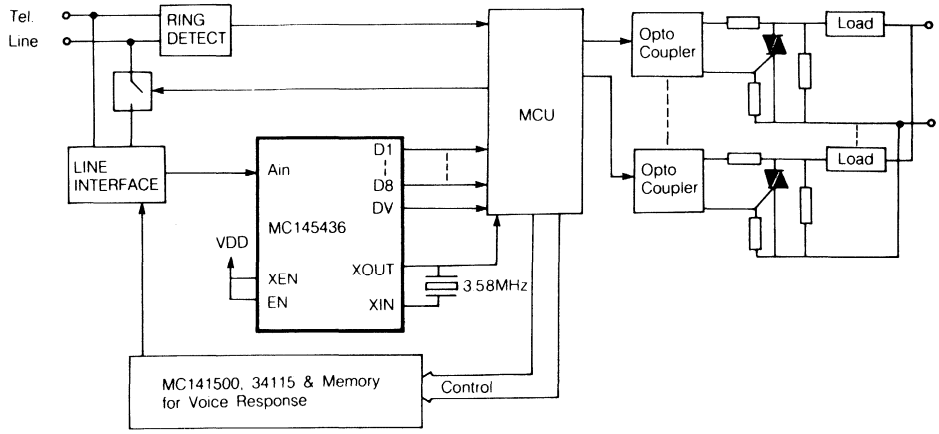


FIGURE 5. MC145436 USED IN A SIMPLIFIED TELECONTROLLER / MONITOR

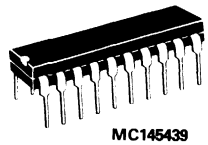
MOTOROLA

MC145439
MC142103

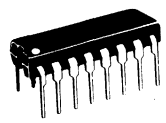
Advance Information

Encoder/Decoder (Transcoder)

For Transmission Applications



MC145439
PLASTIC
CASE 738



MC142103
PLASTIC
CASE 648

3

The MC145439 and MC142103 are high speed CMOS integrated circuits designed to perform the coding translation of clocked serial data into two streams of return to zero (RZ) digital pulses, which are externally mixed to form either AMI, HDB3, B6ZS, or B8ZS (MC142103—AMI or HDB3 only) ternary signals for driving transmission lines. They perform the reverse operation by translating two streams of clocked pulses [which have been derived from an incoming AMI, HDB3, B6ZS, or B8ZS (MC142103—AMI or HDB3 only) ternary encoded signal] into a single stream of clocked binary data. They also feature loopback and error monitoring functions. The coding and decoding functions perform independently at clock rates from zero (dc) to 9 megabits per second. The HDB3 coding and decoding are performed in a manner consistent with the CCITT G.703 recommendations.

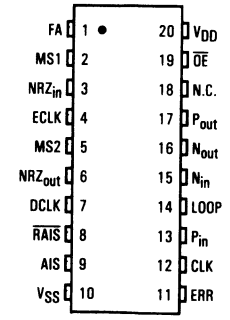
Both Devices:
- Low Power CMOS Operation
- Single 5 Volt Power Supply Operation
- Error Monitor Functions Provided
- Loopback Feature Provided
- Encode and Decode Clock Rates to 9 Megabits per Second
- Pin Selectable Modes of Operation
- TTL Compatible Inputs and Outputs

MC145439 Only:
- 20-Pin Package
- NRZ to AMI, HDB3, B6ZS, B8ZS; AMI, HDB3, B6Z6, B8ZS to NRZ
- Force Alarm and Output Enable Function
- Pin Compatible with HC-5560

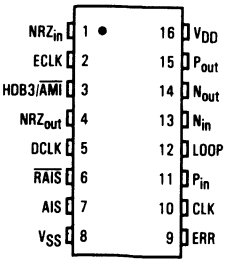
MC142103 Only:
- 16-Pin Package
- NRZ to AMI, HDB3; AMI, HDB3 to NRZ
- Pin Selectable HDB3 or AMI Operation
- Pin Compatible with CD22103 and MJ1471

PIN ASSIGNMENTS

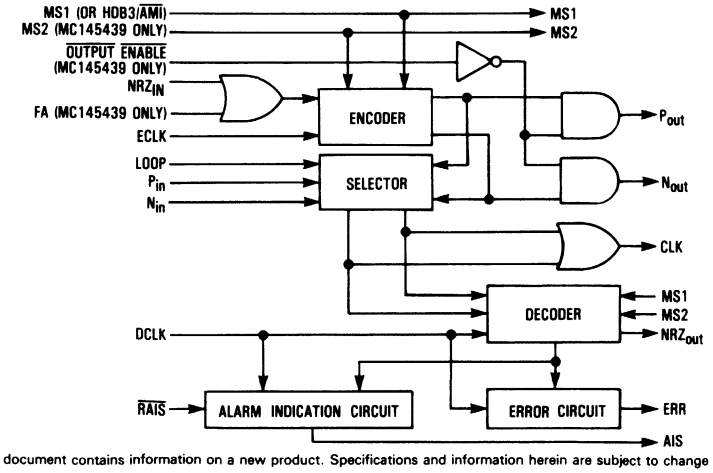
MC145439



MC142103



BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

ADI1295

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	$V_{DD} - V_{SS}$	−0.5 to 6	V
Voltage, Any Pin to V_{SS}	V	−0.5 to V_{DD} + 0.5	V
DC Current Drain per Pin (Excluding V_{DD}, V_{SS})	I	±10	mA
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−85 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than the maximum rated voltages to this high impedance circuit.

For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

RECOMMENDED OPERATING CONDITIONS

Parameter	Pins	0 to 70°C Min	25°C Typ	0 to 70°C Max	Unit
DC Supply Voltage	V_{DD} to V_{SS}	4.5	5.0	5.5	V
Power Dissipation @ 5.0 V					
Static	V_{DD} to V_{SS}	–	50	500	μA
Dynamic—ECLK = DCLK = 9 MHz	V_{DD} to V_{SS}	–	5	8.5	mA
Encoder Clock Frequency	ECLK	–	–	9	MHz
Decoder Clock Frequency	DCLK	–	–	9	MHz
Encoder Clock Duty Cycle	ECLK	40	50	60	%
Decoder Clock Duty Cycle	DCLK	40	50	60	%

DIGITAL ELECTRICAL CHARACTERISTICS (V_{DD} = 5 V, V_{SS} = 0 V, T_A = 0 to 70°C)

Characteristic		Symbol	Min	Max	Unit
High Level Input Voltage		V_{IH}	2.2	–	V
Low Level Input Voltage		V_{IL}	–	0.8	V
Input Current		I_{in}	–	±1.0	μA
Input Capacitance		C_{in}	–	10	pF
High Level Output Voltage (NRZ_{out}, AIS, ERR, CLK)	I_{out} = −0.36 mA I_{out} = −1.7 mA	V_{OH}	4.6 2.5	– –	V
High Level Output Voltage (P_{out}, N_{out})	I_{out} = −0.7 mA I_{out} = −3.4 mA	V_{OH}	4.6 2.5	– –	V
Low Level Output Voltage (NRZ_{out}, AIS, ERR, CLK)	I_{out} = 0.36 mA I_{out} = 0.8 mA	V_{OL}	– –	0.4 0.8	V
Low Level Output Voltage (P_{out}, N_{out})	I_{out} = 1.7 mA I_{out} = 3.5 mA	V_{OL}	– –	0.4 0.8	V

SWITCHING CHARACTERISTICS (V_{DD} = 4.75 V, T_A = 0 to 70°C, C_L = 50 pF)

Characteristic	Figure	Symbol	Min	Max	Unit
ECLK and DCLK Rise and Fall Times	A	t_r, t_f			ns
@ 1.544 MHz			–	60	
@ 2.048 MHz			–	40	
@ 6.312 MHz			–	30	
@ 8.488 MHz			–	10	
Minimum ECLK and DCLK Pulse Width Low or High		t_{WL}, t_{WH}	47	–	ns
ECLK to P_{out} or N_{out} Propagation Delay	B	t_{PLH}, t_{PHL}	–	60	ns
DCLK to NRZ_{out} Propagation Delay	B	t_{PLH}, t_{PHL}	–	40	ns
P_{in} or N_{in} to CLK Propagation Delay	B	t_{PLH}, t_{PHL}	–	50	ns
DCLK to ERR Propagation Delay	B	t_{PLH}, t_{PHL}	–	50	ns
$\overline{RAIS}$ to AIS Propagation Delay	B	t_{PLH}, t_{PHL}	–	60	ns
NRZ_{in} Setup Time to the Falling Edge of ECLK	C	t_{su}	20	–	ns
NRZ_{in} Hold Time After the Falling Edge of ECLK	C	t_h	0	–	ns
P_{in} or N_{in} Setup Time to Rising Edge of DCLK	D	t_{su}	20	–	ns
P_{in} or N_{in} Hold Time After the Rising Edge of DCLK	D	t_h	0	–	ns
Minimum $\overline{RAIS}$ Low Setup Time to DCLK Rising Edge to Include the Current Decoded Bit in the AIS Count	E	t_{su}	20	–	ns
Minimum $\overline{RAIS}$ High Setup Time to DCLK Rising Edge to Ensure the Next Bit on NRZ_{out} will be Included in the AIS Count	E	t_{su}	–	10	ns

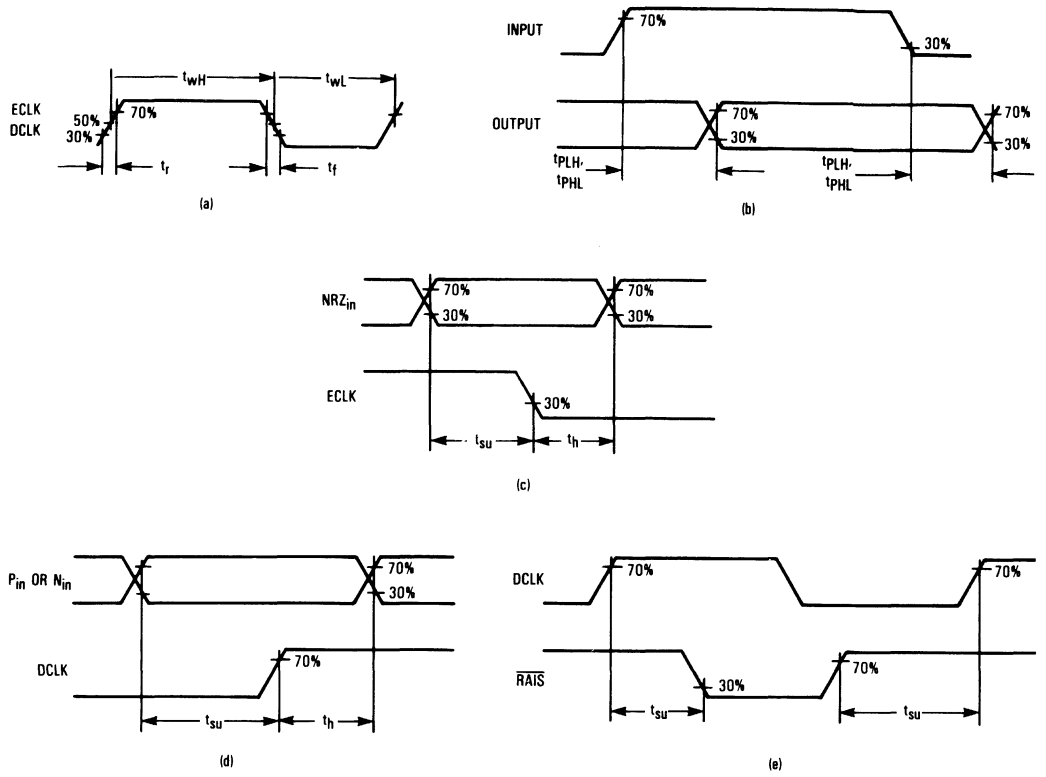


Figure 1. AC Timing Diagrams

PIN DESCRIPTIONS

V_{DD}—POSITIVE SUPPLY

This is the most positive power supply input. Normally +5 volts with respect to V_{SS}.

V_{SS}—NEGATIVE SUPPLY

This pin is the most negative power supply input and is logic ground. Normally 0 volts.

NRZ_{in}—NRZ DATA IN

This input accepts binary inputs for encoding into ternary form according to the appropriate rules. Data is clocked in on the high to low transition of the encoder clock (ECLK).

P_{out}—POSITIVE DRIVE OUTPUT
N_{out}—NEGATIVE DRIVE OUTPUT

These two RZ outputs are clocked out of the encoder on the low to high transition of the encoder clock. The length (high time) of the drive pulses is set by the length of the high level of the encoder clock signal. These two outputs are to be externally mixed to form the ternary transmission line code.

ECLK—ENCODER CLOCK

A negative transition of this input is used to clock NRZ data into the encoder section of the device. The high level time of this clock signal also controls the output pulse width of the encoder output drive signals.

P_{in}—POSITIVE INPUT
N_{in}—NEGATIVE INPUT

These two inputs are RZ representations of the received ternary inputs which have been externally separated. These inputs are clocked into the decoder on the positive (low to high) edge of the decoder clock signal simultaneously.

NRZ_{out}—NRZ DATA OUTPUT

This is the decoded output of the ternary encoded data after being decoded from the positive and negative inputs to the decoder. Data is clocked out serially on the low to high transition of the decoder clock (DCLK) and remains valid for the entire DCLK period.

DCLK—DECODER CLOCK

This input is used to clock in the negative and positive inputs to the decoder on the low to high transition of this line. This

pin also serves as a synchronous clock output for decoded data. The decoded data is updated on each low to high transition of the decoder clock.

CLK—CLOCK OUT

This output is the logical OR of the two RZ inputs to the decoder (i.e., the logical OR of the positive and negative inputs).

MS1—MODE SELECT 1 (MC145439 ONLY)
MS2—MODE SELECT 2 (MC145439 ONLY)

These two inputs work together to select the operating mode of the transcoders encoder, decoder, and error criterion, etc., according to the following truth table.

MS1	MS2	Mode of Operation
0	0	AMI
0	1	B8ZS
1	0	B6ZS
1	1	HDB3

HDB3/$\overline{\text{AMI}}$—MODE SELECT (MC142103 ONLY)

This pin determines the operation mode of the MC142103. A logic one (high) selects HDB3 operation and a logic zero (low) selects AMI operation.

HDB3/$\overline{\text{AMI}}$	Mode of Operation
0	AMI
1	HDB3

AIS—ALARM INDICATION SIGNAL

This output is updated on the falling edge of the $\overline{\text{RAIS}}$ input and functions as delineated in the $\overline{\text{RAIS}}$ pin description.

$\overline{\text{RAIS}}$—RESET AIS

This input, when low, resets and holds a counter which counts the number of zeros decoded by the decoder. The counter is enabled while $\overline{\text{RAIS}}$ is high. The falling edge of the $\overline{\text{RAIS}}$ input sets the AIS output low if three or more zeros have been decoded in the preceding $\overline{\text{RAIS}} = 1$ period. The falling edge of the $\overline{\text{RAIS}}$ input also causes the AIS output to go high if less than three zeros have been decoded in the preceding two successive $\overline{\text{RAIS}}$ high periods.

ERR—ERROR

This output is flagged (the term "flagged" is defined to be: setting the error output pin high for one decoder clock cycle following the input of the error) for one decoder clock period following the reception of an error at the decoder input. The error output is updated on the rising edge of the decoder clock pin. In all modes if both inputs to the decoder are high at the rising edge of the decoder clock an error is flagged (on the next rising edge of the decode clock). In the AMI mode, an error is flagged if a bipolar violation is discovered. In the HDB3 mode, an error is flagged if a violation is detected of the same polarity as a previously detected violation (for example three marks in a row of the same polarity). An error is also flagged (in the HDB3 mode) if the polarity of the violation pulse is correct but not preceded by two zeros. In the B8ZS and B6ZS modes of operation, an error is flagged if a violation pulse is received which is not preceded by a zero.

LOOP—LOOP TEST

This input when high, disconnects the normal inputs to the decoder and internally ties the two encoder outputs (positive and negative drive outputs) to the decoder inputs. In this mode, an external decoder clock must be supplied. Also note that the clock out line is a function of whichever set of inputs are selected for the decoder.

$\overline{\text{OE}}$—$\overline{\text{OUTPUT ENABLE}}$ (MC145439 ONLY)

This input, when high forces both encoder outputs low. When the output enable input is low, normal operation proceeds.

FA—FORCE ALARM (MC145439 ONLY)

The force alarm input inhibits the normal input to the encoder by logically "ORing" a "one" in with the incoming NRZ data. This forces the coder to code the all ones alarm pattern. The encoder operates normally when this pin is low.

N.C.—NO CONNECT (MC145439 ONLY)

This pin is not connected to any internal circuitry and may be either high or low. The line is ignored by the MC145439 Transcoder.

BACKGROUND

The basic goal of the international Integrated Services Digital Network (ISDN) standards effort is to develop a 64 kbps customer data channel. Thus, in order to expand the capabilities of the emerging digital network, support future services, and be compatible with the ISDN movement throughout the international community, the U.S. network is evolving to a 64 kbps clear channel capability (64 CCC) from the present 56 kbps capability. Today the T1 network is constrained by the line code restriction of at least a 1/8 average mark density, and is further constrained by a restriction of not more than 15 consecutive spaces (zeros) on DS1 signals, which is imposed by the clock recovery circuits of some T1 repeaters. The clock recovery circuit of these repeaters will begin to lose timing accuracy in the presence of long strings of zeros or low marks density. These restrictions do not limit PCM voice signals, however, they are a constraint on the transmission of digital data. Due to these restrictions, existing T1 and T1C transmission systems do not provide 64 CCC. To provide this capability, a coding and decoding scheme which allows the transmission of any data pattern and still satisfy the line code restrictions will be required. This coding scheme has been specified in the U.S. and is known as B8ZS for T1 systems and B6ZS for T2 systems. The CCITT on the other hand has recommended a scheme known as HDB3. Each of these coding schemes are variants of the existing alternate mark inversion (AMI) scheme, and each has specific rules for the coding of strings of consecutive zeros. AMI is a three level line code, where binary ones are coded as pulses above or below the mid level, and zeros are coded as no signal (the mid level). In this coding scheme, each mark is coded as pulses of a polarity opposite to the polarity of the preceding pulse (mark). The HDB3, B8ZS, and B6ZS coding schemes have special rules

for the coding of strings of binary zeros with pulses that violate the rule of alternate mark inversion. These purposeful violations can be detected by the decoder and the true data (a string of zeros) substituted by the decoder. The B8ZS and B6ZS schemes substitute (for strings of eight or six zeros) one of two possible patterns to represent the string of zeros based on the polarity of the previous mark. (See Figures 2 and 3.) Note that there are bipolar violations in the 2nd and 5th bit positions in the B6ZS scheme and bipolar violations in the 4th and 7th bit positions in the B8ZS coding scheme. The HDB3 scheme selects one of four possible code patterns for a string of four zeros based on the polarity of the previous pulse and if an even or odd number of pulses have occurred since the previous code violation (see Figure 4). Coding of a binary signal into an HDB3 signal is done (per CCITT G703 annex) according to the following rules:

1) HDB3 signal is pseudo ternary; the three states are denoted B+, B−, and 0.
2) Spaces in the binary signal are coded as spaces in the HDB3 signal. For strings of four spaces, however special rules apply (see item 4 following).
3) Marks in the binary signal are coded alternately in the HDB3 signal (alternate mark inversion). Violations of the rule of alternate mark inversion are introduced when coding strings of four spaces.
4) Strings of four spaces in the binary signal are coded according to the following rules:
   a) The first space of a string is coded as a space if the polarity of the preceding mark of the HDB3 signal has a polarity opposite to the preceding violation and is not a violation by itself.
   b) It is coded as a mark (i.e., not a violation) if the preceding mark of the HDB3 signal has the same polarity as that of the preceding violation or is by itself a violation. This rule ensures that successive violations are of alternate polarity so that no dc component is introduced. The second and third spaces of a string are always coded as spaces. The last space of a string of four zeros is always coded as a mark, the polarity of which is such that it violates the rule of alternate mark inversion.

CIRCUIT OPERATION

The MC145439 encoder/decoder performs AMI, HDB3, B6ZS, or B8ZS (MC142103 AMI or HDB3 only) coding and decoding functions with error detection. They are generally used in telephony transmission applications and are operated in the 0 to 9 megabits per second frequency range. Coding and decoding are performed in independent sections. The encoder accepts a serial NRZ unipolar input signal and a synchronous transmission clock and creates two binary RZ output signals (positive and negative output drives) which are externally mixed to generate the ternary bipolar signals for driving transmission lines. The decoder section accepts ternary bipolar signals which have been externally split to provide two binary RZ input signals (positive and negative inputs) which are clocked into the decoder by an externally supplied synchronous clock signal.

ENCODER SECTION

The encoder of the MC145439 and MC142103 operate on 4-bit serial strings of data while operating in the AMI and HDB3 modes of operation. When operating in the B8ZS or B6ZS modes (MC145439 only), the encoder operates on 8- or 6-bits of serial data respectively. In all cases binary data is serially clocked into the encoder on the high to low transition of the encoder clock. The outputs of the encoder (positive and negative drive) are delayed from the input data by four, six, or eight encoder clock pulses depending on the mode selection of the device. (See timing diagrams.) The duty cycle or high time of the encoders drive lines is equal to the high time of the encoder clock.

DECODER SECTION

The Decoder Section of the MC145439 and the MC142103 operates on serial strings of ternary data that have been split into two RZ inputs (positive and negative inputs). The decoder however, accepts these two inputs simultaneously on the positive transition of the decoder clock. The output of the decoder is delayed from the input by four, six, or eight decoder clocks and appears as binary NRZ data on the NRZ output pin on the positive transition of the decoder clock. The NRZ data is updated on each successive positive transition of the decoder clock.

ERROR DETECTION SECTION

The Error Detection circuitry of the MC145439 and MC142103 operates as follows, according to the mode selection of the device. In all cases, the error signal is flagged for one full decoder clock period following the input of the error. In all modes, when a high level appears simultaneously on both positive and negative inputs to the decoder, the error output is flagged for one period of the decoder clock. In this case, a positive input (logic one) is assumed as an input to the decoder. In the AMI mode, errors are flagged when a bipolar violation is received. In the HDB3 mode, the error output is flagged if a violation pulse is received of the same polarity as the last received violation pulse. For example, three or more received pulses of the same polarity. An error is also flagged if a bipolar violation is received without being preceded by two spaces. In the B8ZS and B6ZS modes of operation (MC145439 only), the error line is flagged if a violation is received and not preceded by a zero.

LOOP TEST

When in the Loop Test mode, the encoders positive and negative outputs are internally connected to the decoders positive and negative inputs. The normal inputs are ignored in this mode. In the Loop Test mode, the appropriate decoder clock must be supplied to the MC145439 or MC142103. The Clock Out line of the MC145439 and MC142103 are a logical OR of the decoder inputs and is generally used by external timing recovery circuits.

AIS SECTION

The AIS (Alarm Indication Signal) circuitry contains a counter that increments (to a maximum of three) each time a zero is decoded by the decoder. This counter is reset and held to zero by a low level on the $\overline{RAIS}$ input. A logic one on the $\overline{RAIS}$ input enables the decoder zero counter to increment on the positive edge of the decoder clock. The AIS output is set two zero (on the falling edge of $\overline{RAIS}$ input) provided three or more zeros have been decoded in the preceding $\overline{RAIS} = 1$ period. The AIS output is set high (on the falling edge of the $\overline{RAIS}$ input) if less than three zeros have been decoded in the preceding two $\overline{RAIS} = 1$ periods.

POLARITY OF PREVIOUS MARK	B6ZS CODING SCHEME CODE USED FOR SIX CONSECUTIVE ZEROS						
+	0	+	−	0	−	+	
−	0	−	+	0	+	−	

*2ND *5TH

*NOTE: + implies a positive pulse
0 implies no pulse
− implies a negative pulse

Figure 2. B6ZS Coding Scheme

POLARITY OF PREVIOUS MARK	B8ZS CODING SCHEME CODE USED FOR EIGHT CONSECUTIVE ZEROS							
+	0	0	0	+	−	0	−	+
−	0	0	0	−	+	0	+	−

*4TH *7TH

*NOTE: + implies a positive pulse
0 implies no pulse
− implies a negative pulse

Figure 3. B8ZS Coding Scheme

POLARITY OF PREVIOUS MARK	ODD NUMBER OF PULSES SINCE VIOLATION					EVEN NUMBER OF PULSES SINCE VIOLATION			
+	0	0	0	+		−	0	0	−
−	0	0	0	−		+	0	0	+

VIOLATION *4TH VIOLATION *4TH

*NOTE: + implies a positive pulse
0 implies no pulse
− implies a negative pulse

Figure 4. HDB3 Coding Scheme

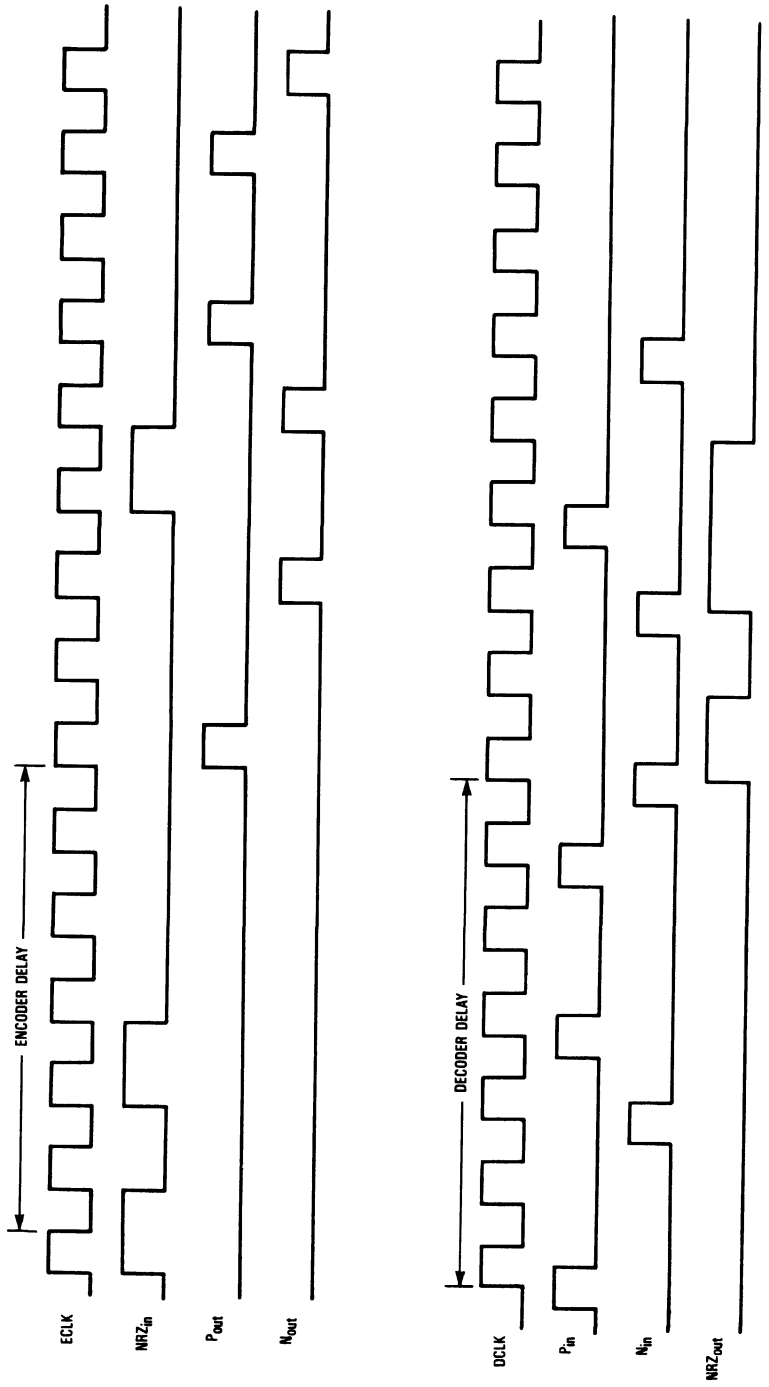


Figure 5. B6ZS Encode and Decode Timing

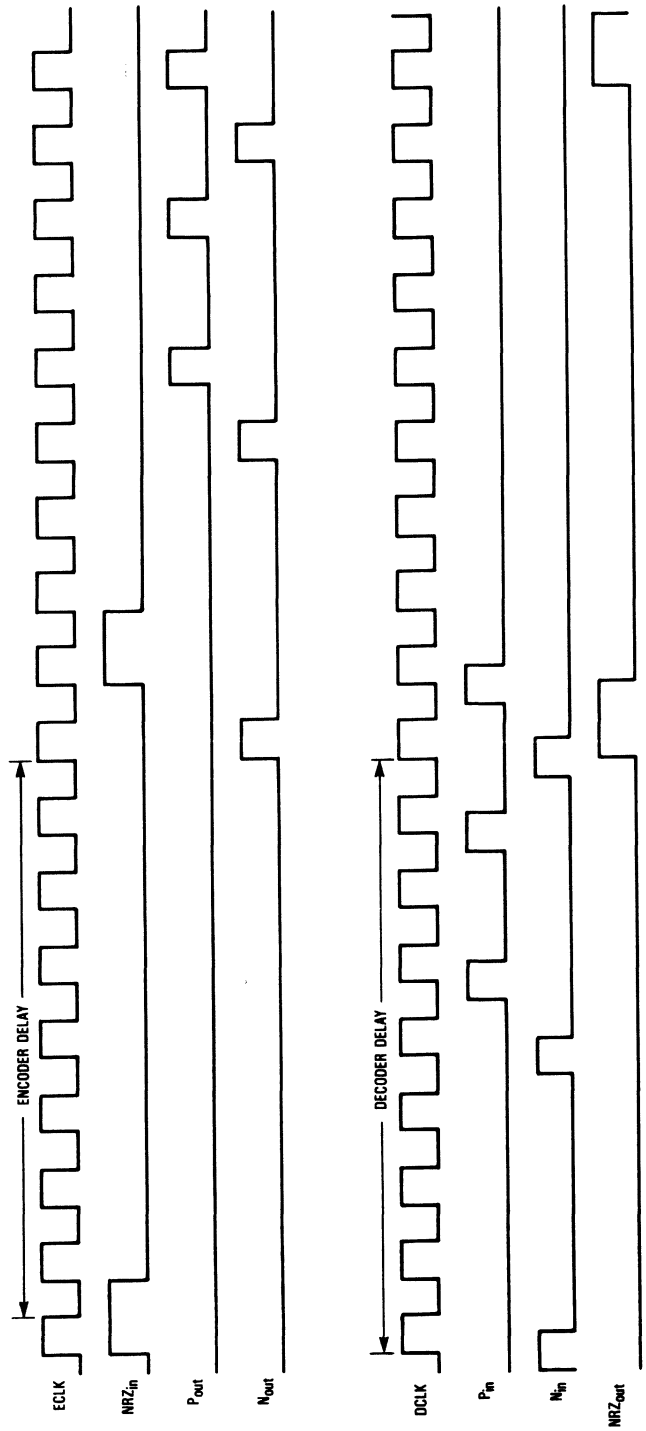


Figure 6. B8ZS Encode and Decode Timing

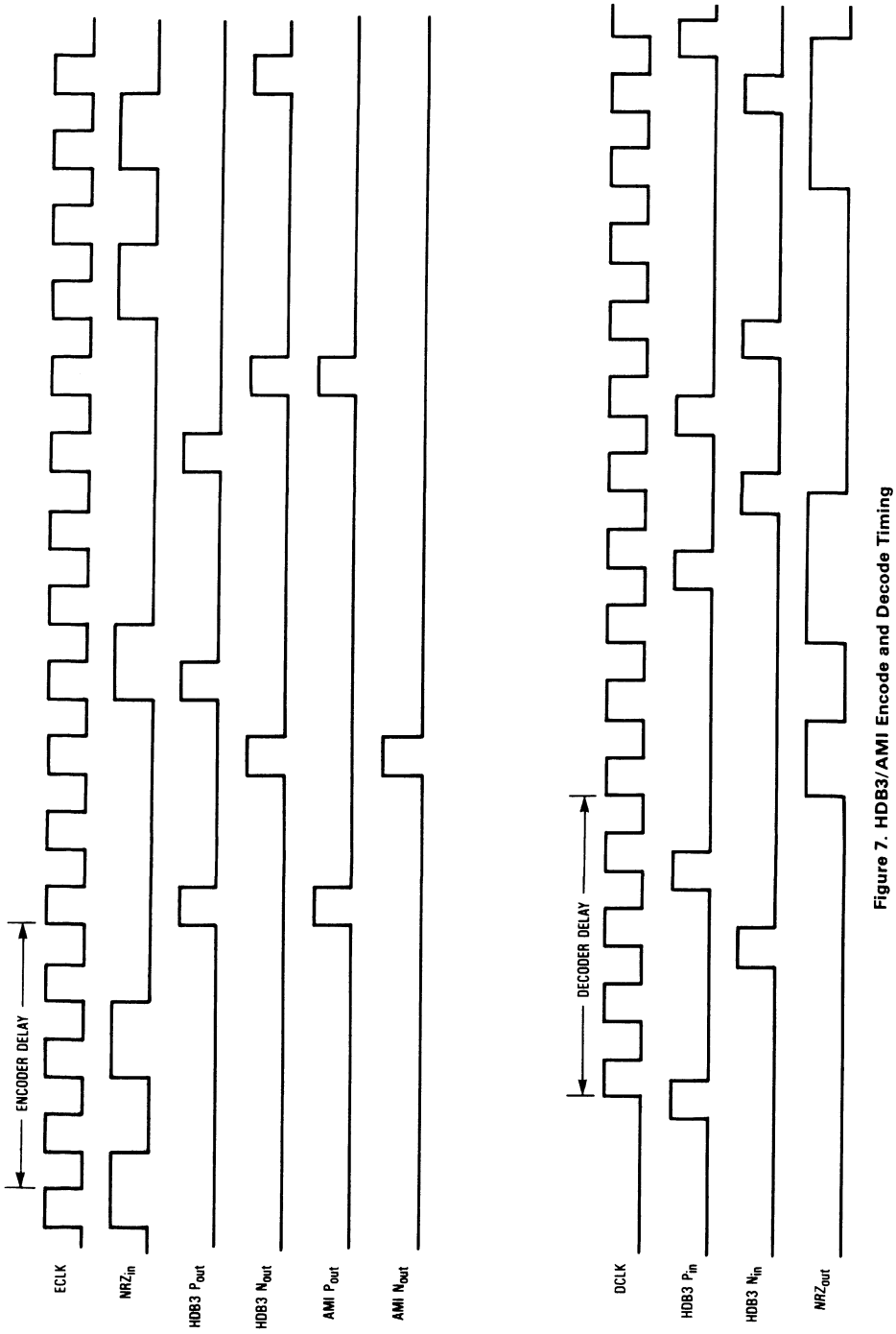


Figure 7. HDB3/AMI Encode and Decode Timing

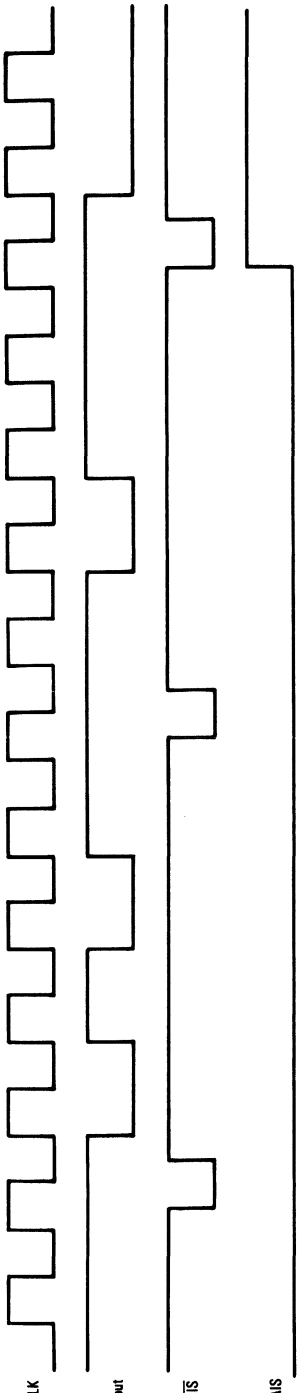


Figure 8. AIS Timing

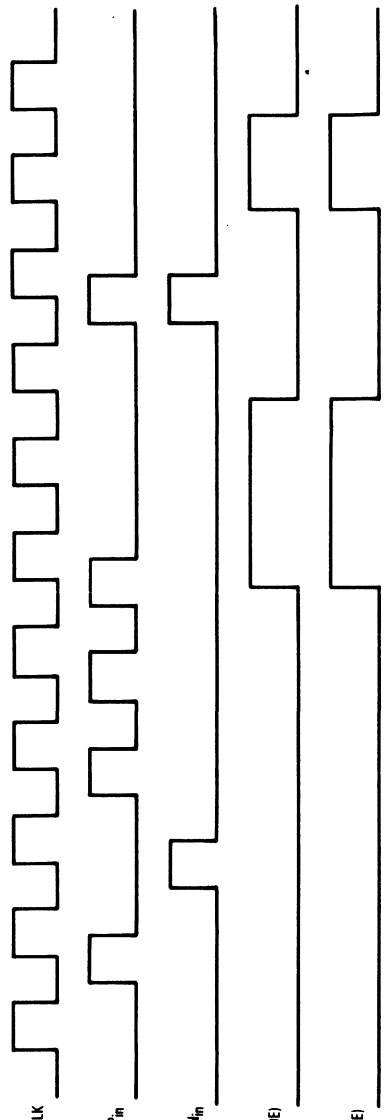


Figure 9. Error Timing

3

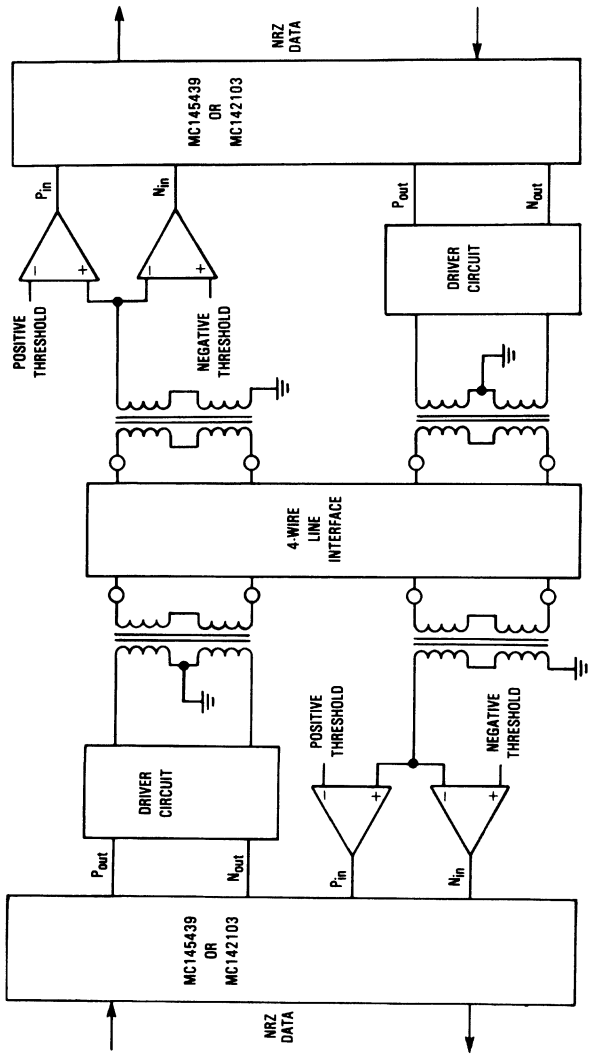


Figure 10. Typical Line Interface

MOTOROLA

MC145440

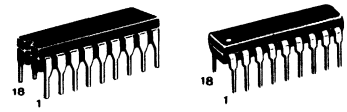
BELL 103 300 BAUD MODEM BAND-PASS FILTER

The MC145440 is a 300 baud modem filter designed to be used with the MC14412, MC145445, or MC6860 modems. These modem/filter combinations fulfill the major requirements of a complete Bell 103 300 baud modem system. The MC145441 is also available to fulfill the CCITT V.21 equivalent filtering function. Features of the MC145440 include:

- Low Band Band-pass Filter
- High Band Band-pass Filter
- Bell 103 Frequency Compatible
- Spare Operational Amplifier
- Answer or Originate Mode
- Self Test Loopback Configuration
- Single or Split Power Supply Operation
- 18-Pin Package

CMOS
(LOW-POWER COMPLEMENTARY MOS)

300 BAUD MODEM BAND-PASS SWITCHED CAPACITOR FILTER

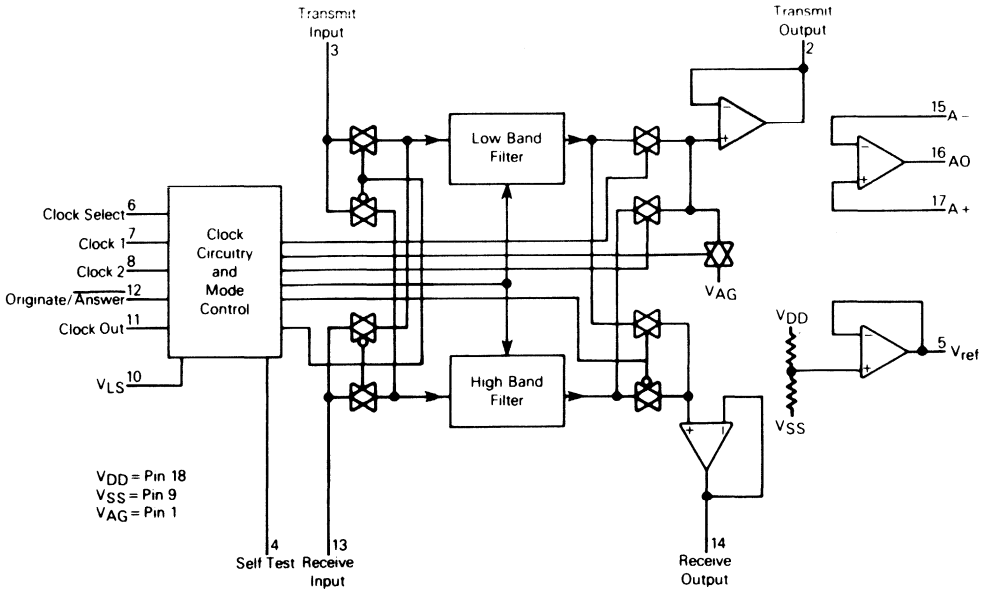


L SUFFIX
CERAMIC PACKAGE
CASE 726

P SUFFIX
PLASTIC PACKAGE
CASE 707

3

BLOCK DIAGRAM

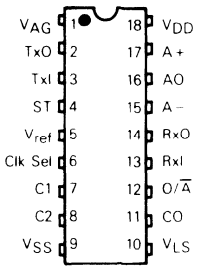


DS9887

MAXIMUM RATINGS (V_{SS} = 0 V)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to 18	V
Input Voltage, all pins	V_{in}	−0.5 to V_{DD} + 0.5	V
DC Current Drain per pin (Not V_{DD} or V_{SS})	I	10	mA
Operating Temperature Range	T_A	−40 to 85	°C
Storage Temperature Range	T_{stg}	−65 to 150	°C

PIN ASSIGNMENT



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}-V_{SS}	4.5	10	16	V

DIGITAL ELECTRICAL CHARACTERISTICS (T_A = −40 to 85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Operating Current, V_{DD} = 10 V, V_{SS} = 0 V, 1 MHz Crystal		I_{DD}	–	–	10	mA
Input Capacitance		C_{in}	–	5.0	7.5	pF
Mode Control Logic Levels						
V_{LS}	TTL Mode	–	V_{SS}	–	V_{DD} − 4.0	V
	CMOS Mode	V_{IH}	V_{DD} − 0.5	–	V_{DD}	
Clock Select (CS)	State 1, 4.0 MHz	V_{IH}	V_{DD} − 0.5	–	V_{DD}	V
	State 2, 3.684 MHz	V_{IM}	(V_{DD} − V_{SS})/2 − 0.5	–	(V_{DD} − V_{SS})/2 + 0.5	
	State 3, 1.0 MHz	V_{IL}	V_{SS}	–	V_{SS} + 0.5	
O/Ā TTL Logic Levels (V_{DD} = 5 V, V_{SS} = −5 V, V_{LS} = 0 V)						
Input Current	"1" level	I_{IH}	–	–	+ 0.3	μA
	"0" Level	I_{IL}	− 0.3	–	–	
Input Voltage	"1" level	V_{IH}	V_{LS} + 2.0	–	–	V
	"0" level	V_{IL}	–	–	V_{LS} + 0.8	
ST, C1, O/Ā CMOS Logic Levels (V_{LS} = V_{DD}, V_{SS} = 0 V)						
Input Current	"1" level	I_{IH}	–	–	+ 0.3	μA
	"0" level	I_{IL}	− 0.3	–	–	
Input Voltage	"1" level, V_{DD} = 10 V	V_{IH}	7.5	5.75	–	V
	"0" level, V_{DD} = 10 V	V_{IL}	–	4.25	3.0	
CO Output Characteristics (V_{DD} = 10, V_{SS} = 0 V)						
TTL Output Voltage (TTL Mode)	"1" level, I_O = 8 mA	V_{OH}	2.4	–	–	V
	"0" level, I_O = 2.5 mA	V_{OL}	–	–	0.8	
CMOS Output Current	V_{DD} = 10 V, V_{OH} = 9.5 V	I_{OH}	− 1.3	− 2.25	–	mA
	V_{DD} = 10 V, V_{OL} = 0.5 V	I_{OL}	1.1	2.25	–	

ANALOG ELECTRICAL CHARACTERISTICS (V_{DD} = 10 V, V_{AG} = 5 V, V_{SS} = 0 V, T_A = 0 to 70°C)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Input Current (V_{AG})	I_I	− 50	–	+ 50	μA
DC Input Current (TxI, RxI)	I_I	− 10	–	+ 10	μA
AC Input Impedance (TxI, RxI)	Z_{in}	0.2	1.0	–	MΩ
Input Voltage Range (TxI, RxI)	V_{in}	V_{SS} + 1.5	–	V_{DD} − 1.5	V

OP-AMP CHARACTERISTICS (V_{DD} = 5 to 10 V, V_{AG} = V_{DD}/2, V_{SS} = 0 V, T_A = 0 to 70°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (AO)	I_{IO}	− 50	–	+ 50	mV
Open Loop Gain (R_L = 10 kΩ)	A_{OL}	–	45	–	dB
Input Bias Current (A+, A−)	I_{IB}	–	± 0.1	–	μA
Output Noise (900 Ω)	P_N	–	− 3	–	dBrnC
Slew Rate	S_R	–	2	–	V/μs
Output Voltage Swing (R_L = 600 Ω to V_{AG})	–	1.5 V	–	V_{DD} − 1.5 V	V

DIGITAL SWITCHING CHARACTERISTICS (V_{DD} = 5 V, V_{SS} = 0 V, T_A = 25°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Rise and Fall Times	C1, O/A, ST	t_r, t_f	–	–	4	μs
Input Pulse Width	(TTL Mode) O/A	t_w	200	–	–	ns
	(CMOS Mode) C1, O/A, ST	t_w	125	–	–	
Clock Frequency (Driven by External Clock) (C1 Pin)	(CMOS)	f_c	–	1.0	4.0	MHz
Crystal Frequency	C1, C2	f_x	1.0	–	4.0	MHz

LOW-BAND FILTER CHARACTERISTICS (V_{DD} = 10 V, V_{AG} = V_{DD}/2, V_{SS} = 0 V, T_A = 0 to 70°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Full Scale Input Voltage (+3 dBmO)		V_{FS}	2.13	–	–	Vp-p
Gain at 1170 Hz, 0 dBmO		A_r	9.0	10.0	11.0	dB
Idle Noise, Input = V_{AG}, 900 Ω load		P_N	–	20	26	dBrnC
Dynamic Range (Full Scale Output/Idle Noise)		DR	72	78	–	dB
Total Harmonic Distortion		THD	–	1.0	–	%
Pass-Band Ripple	1070 Hz to 1270 Hz	–	–	–	2	dBp-p
Pass-band Response, Ref 1070 Hz, 0 dBmO	1270 Hz	–	−1.5	–	1.5	dB
Rejection (Ref 1170 Hz)	2025 Hz to 2225 Hz	–	−55	–	–	dB
Differential Group Delay	1070 Hz to 1270 Hz	–	–	–	600	μs

HIGH-BAND FILTER CHARACTERISTICS (V_{DD} = 10 V, V_{AG} = V_{DD}/2, V_{SS} = 0 V, T_A = 0 to 70°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Full Scale Input Voltage (+3 dBmO)		V_{FS}	2.13	–	–	Vp-p
Gain at 2125 Hz, 0 dBmO		A_r	9.0	10.0	11.0	dB
Idle Noise, Input = V_{AG}, 900 Ω load		P_N	–	20	26	dBrnC
Dynamic Range (Full Scale Output/Idle Noise)		DR	72	78	–	dB
Total Harmonic Distortion		THD	–	1.0	–	%
Pass-Band Ripple	2025 Hz to 2225 Hz	–	–	–	2	dBp-p
Pass-band Response, Ref 2025 Hz, 0 dBmO	2225 Hz	–	−1.5	–	1.5	dB
Rejection (Ref 2125 Hz)	1070 Hz to 1270 Hz	–	−55	–	–	dB
Differential Group Delay	2025 Hz to 2225 Hz	–	–	–	600	μs

V_{ref} CHARACTERISTICS (V_{DD} = 5 to 15 V, V_{ref} = V_{DD}/2, V_{SS} = 0 V, T_A = 0 to 70°C)

Characteristic		Symbol	Min	Typ	Max	Unit
V_{ref} Output Voltage	I_O = ±5 mA	V_{ref}	−250	±75	+250	mV

3

PIN DESCRIPTIONS

V_{DD} (PIN 18) – Positive power supply.

V_{SS} (PIN 9) – Negative power supply.

V_{AG} (PIN 1) – Analog ground. In single supply applications, V_{AG} is driven from V_{ref}.

V_{ref} (PIN 5) – This pin provides an output DC voltage at approximately $(V_{DD}-V_{SS})/2$ for use as an external analog ground in single supply applications. In symmetric dual power supply applications, V_{ref} is not used.

V_{LS}, LOGIC SHIFT VOLTAGE (PIN 10) – This pin determines the input/output logic level compatibility of O/$\overline{A}$ and CO. When the voltage on this pin is greater than $V_{DD}-0.5$ V and less than V_{DD}, these digital inputs and outputs are CMOS compatible. When the voltage on this pin is less than $V_{DD}-4$ V and greater than V_{SS}, these digital inputs and outputs are TTL compatible, and V_{LS} is connected to digital ground.

C1, C2, CLOCK 1, CLOCK 2 (PIN 7, PIN 8) – These pins connect to an internal crystal oscillator. In operation, a parallel resonant crystal is connected from C1 to C2 as well as a 10 MΩ resistor in parallel with the crystal and 20 pF capacitors from C1 and C2 to V_{SS}. Crystal frequencies of 1.0, 3.6864, or 4.0 MHz may be used. Alternatively, an external CMOS level signal at the crystal frequency may be applied to C1 in lieu of the crystal, capacitors, and resistor. The inverted clock signal will appear at C2 and will be a CMOS output from V_{SS} to V_{DD}.

Clk Sel, CLOCK SELECT (PIN 6) – This pin is a three-state selector used to select one of the three crystal/clock options. When at V_{DD}, V_{AG}, or V_{SS}, this pin selects the 4.0, 3.6864, or 1.0 MHz crystal/clock option, respectively, for C1 and C2.

Clock Select Pin 6	Clock Frequency *	Clock Output Pin 11
V_{DD}	4.0 MHz	1.0 MHz
V_{AG}	3.6864 MHz	N/A
V_{SS}	1.0 MHz	1.0 MHz

*Use either an external clock to drive C1 Pin 7 or external crystal across C1 and C2 Pins 7 and 8.

CO, CLOCK OUT (PIN 11) – This provides a 1.0 MHz output clock signal when either the 1.0 or 4.0 MHz clock is selected and is typically used to drive the clock input to a MC14412 or MC6860 modem. The clock output is not usable when the 3.6864 MHz option is used. The logic family compatibility (CMOS or TTL) of this output is determined by V_{LS}.

O/$\overline{A}$, ORIGINATE, ANSWER (PIN 12) – The mode of the device, originate or answer, is selected with this pin. In the originate mode, selected with a logic "1", the low band band-pass filter is switched into the transmit path and the high band band-pass filter is switched into the receive path. In the answer mode, the filters switch position. The input levels of this pin are determined by V_{LS}.

TxI, TRANSMIT INPUT (PIN 3) – TxI is the input to the transmit band-pass filter which is the low band filter in the originate mode and the high band filter in the answer mode. In the self test mode, this input is routed to the appropriate band-pass filter input so as to pass the modulated data to the demodulator.

TxO, TRANSMIT OUTPUT (PIN 2) – This pin is the output of the Tx output amplifier and typically drives the modulated data into the duplexer or hybrid circuit (see ST pin).

RxI, RECEIVE INPUT (PIN 13) – RxI is the input to the receive band-pass filter which is the high band filter in the originate mode and the low band filter in the answer mode. In the self test mode, this input is disabled.

RxO, RECEIVE OUTPUT (PIN 14) – The output of the receive band-pass filter, whether low band or high band, is provided at RxO. Typically, this signal is capacitively coupled to the input of the external carrier detector and limiter. The AC coupling capacitor is required because of the variable DC offset of the receive filter.

ST, SELF TEST (PIN 4) – A "1" on ST puts the device into a self test mode which routes the modulated carrier from TxI, through the appropriate filter, and out RxO back to the receive carrier input of the modem. TxO remains at V_{AG} during a self test operation. This pin is a standard CMOS input regardless of the state of V_{LS}.

A+ (PIN 17) – This is the noninverting input to the spare operational amplifier.

A– (PIN 15) – This is the inverting input to the spare operational amplifier.

AO (PIN 16) – This is the output of the spare operational amplifier.

FUNCTIONAL DESCRIPTION

This device is capable of four basic analog configurations determined by the state of O/$\overline{A}$ and ST. The normal (non-self test) and self test modes in both the answer and originate modes will be discussed.

In the normal originate mode, O/$\overline{A}$ is a "1" and self test, ST, is a "0". When in this mode, the Tx carrier from the modem is input on TxI and routed through the low band band-pass filter. The filter output is switched to the input of the Tx op amp which typically drives the Tx carrier off chip into a duplexer circuit which could be implemented with the spare operational amplifier. The output of the duplexer drives RxI which is switched to the input of the high band band-pass filter. The filter output is available at RxO which is typically the input to a limiter and carrier detector.

The normal answer mode is established by a "0" on both O/$\overline{A}$ and ST. This mode is identical to the normal originate mode with one exception: the band-pass filters swap positions, i.e., the high band band-pass filter is switched into the transmit path, and the low band band-pass filter is switched into the receive path.

When used with the MC14412 in the self test mode, the device will function as follows. A "1" on the self test pin of both devices enables the self test mode. The modem switches its demodulator to its modulator frequency and demodulates its own modulated carrier. The modem filter switches the transmit carrier of the modem from TxI through the low band filter and out the RxO pin to the limiter when in the originate mode. When the system is in the answer mode, the modulated signal is instead routed through the high-band filter. TxO will remain at mid-supply (V_{AG}) during self test operations.

3

FIGURE 1 – TEST CIRCUIT

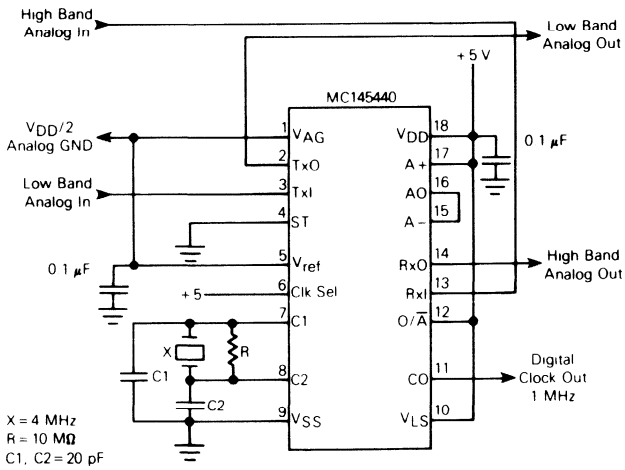
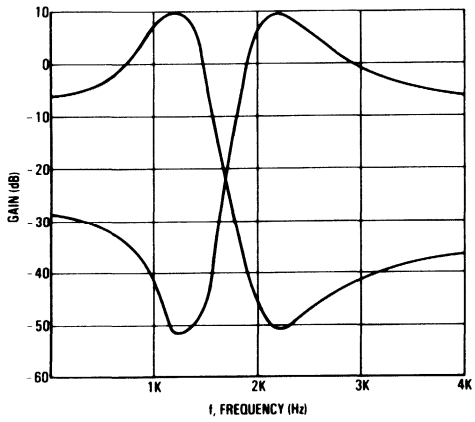


FIGURE 2 – MC145440 FREQUENCY RESPONSE



3

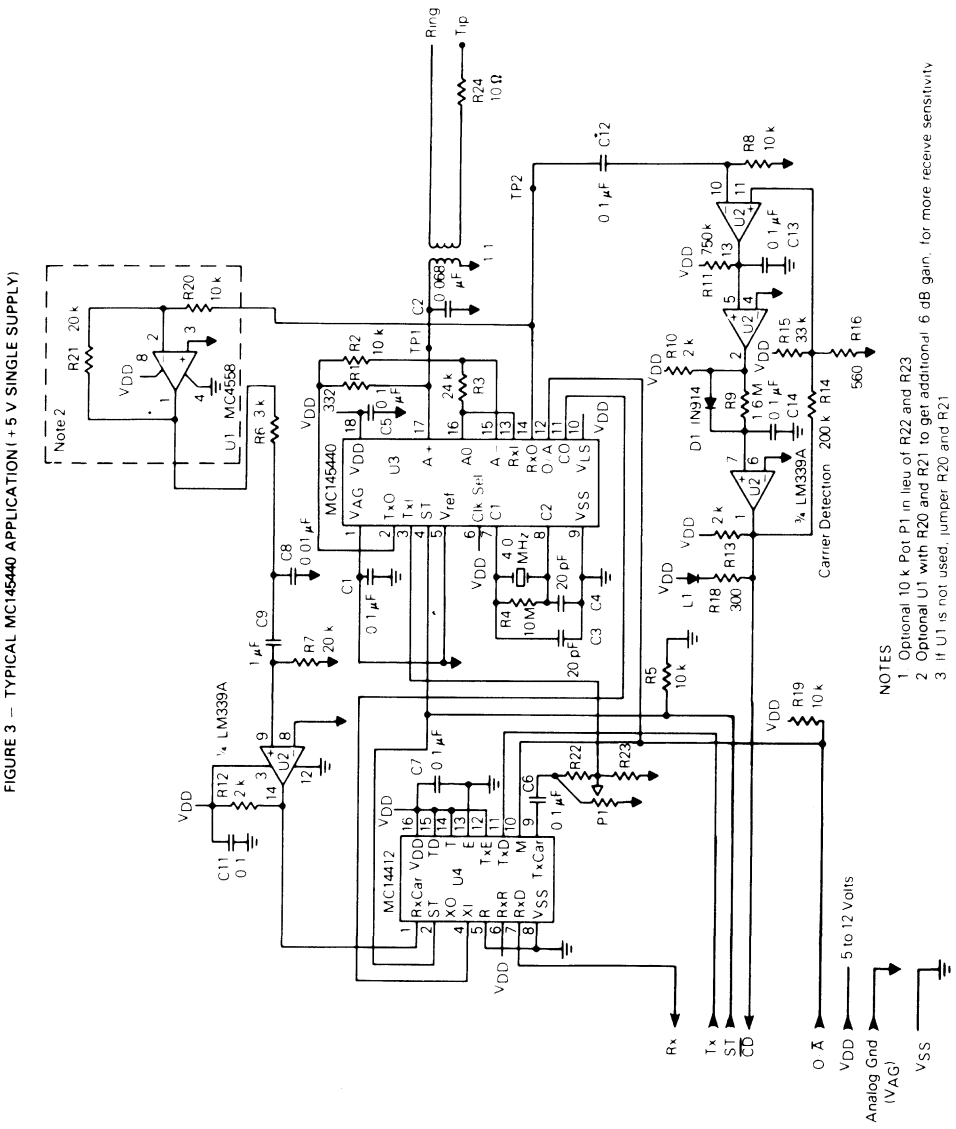


FIGURE 3 – TYPICAL MC145440 APPLICATION (+5 V SINGLE SUPPLY)

NOTES
1 Optional 10 k Pot P1 in lieu of R22 and R23
2 Optional U1 with R20 and R21 to get additional 6 dB gain for more receive sensitivity
3 If U1 is not used, jumper R20 and R21

MOTOROLA

MC145441

Advance Information

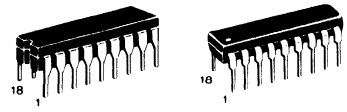
CCITT V.21 300 BAUD MODEM BAND-PASS FILTER

The MC145441 is a 300 baud modem filter designed to be used with the MC14412 or MC145445 modems. These modem/filter combinations fulfill the major requirements of a complete CCITT V.21 300 baud modem system. The MC145440 is also available to fulfill the Bell 103 equivalent filtering function. Features of the MC145441 include:

- Low Band Band-Pass Filter
- High Band Band-Pass Filter
- Spare Operational Amplifier
- Answer or Originate Mode
- Self Test Loopback Configuration (Optional)
- Single or Split Power Supply Operation
- 18-Pin Package
- CCITT V.21 Compatible

CMOS
(LOW-POWER COMPLEMENTARY MOS)

300 BAUD MODEM BAND-PASS SWITCHED CAPACITOR FILTER

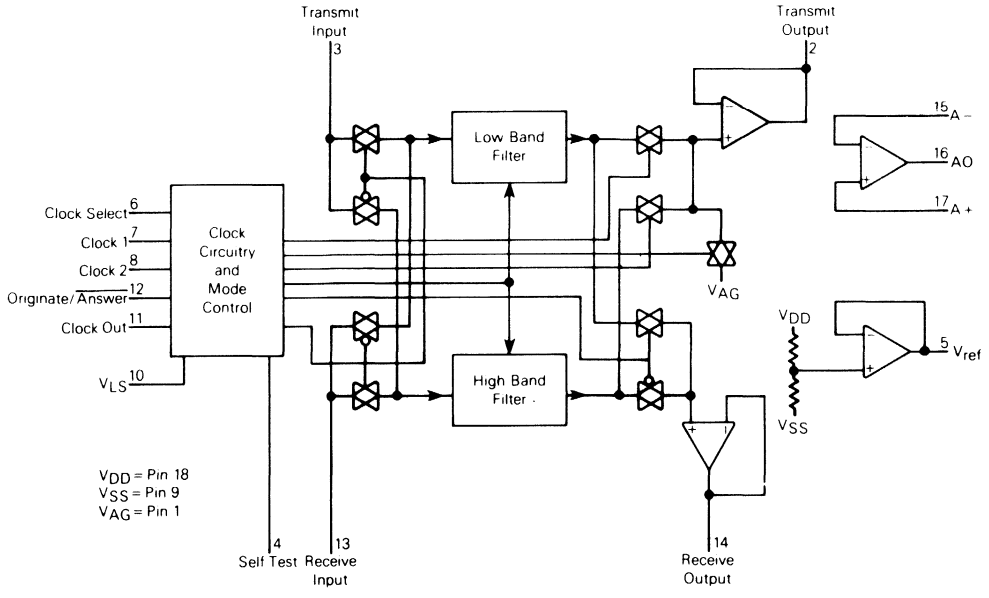


L SUFFIX
CERAMIC PACKAGE
CASE 726

P SUFFIX
PLASTIC PACKAGE
CASE 707

3

BLOCK DIAGRAM



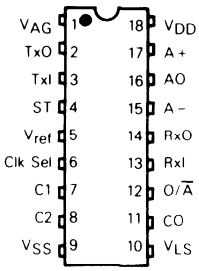
This document contains information on a new product. Specifications and information herein are subject to change without notice.

ADI1020

MAXIMUM RATINGS (V_{SS} = 0 V)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to 18	V
Input Voltage, all pins	V_{in}	−0.5 to V_{DD} + 0.5	V
DC Current Drain per pin (Not V_{DD} or V_{SS})	I	10	mA
Operating Temperature Range	T_A	−40 to 85	°C
Storage Temperature Range	T_{stg}	−65 to 150	°C

PIN ASSIGNMENT



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}-V_{SS}	4.5	10	16	V

DIGITAL ELECTRICAL CHARACTERISTICS (T_A = −40 to 85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Operating Current, V_{DD} = 10 V, V_{SS} = 0 V, 1 MHz Crystal		I_{DD}	–	–	10	mA
Input Capacitance		C_{in}	–	5.0	7.5	pF
Mode Control Logic Levels						
V_{LS}	TTL Mode	–	V_{SS}	–	V_{DD} − 4.0	V
	CMOS Mode	V_{IH}	V_{DD} − 0.5	–	V_{DD}	
Clock Select (CS)	State 1, 4.0 MHz	V_{IH}	V_{DD} − 0.5	–	V_{DD}	V
	State 2, 3.684 MHz	V_{IM}	(V_{DD} − V_{SS})/2 − 0.5	–	(V_{DD} − V_{SS})/2 + 0.5	
	State 3, 1.0 MHz	V_{IL}	V_{SS}	–	V_{SS} + 0.5	
O/Ā TTL Logic Levels (V_{DD} = 5 V, V_{SS} = −5 V, V_{LS} = 0 V)						
Input Current	"1" level	I_{IH}	–	–	+0.3	μA
	"0" Level	I_{IL}	−0.3	–	–	
Input Voltage	"1" level	V_{IH}	V_{LS} + 2.0	–	–	V
	"0" level	V_{IL}	–	–	V_{LS} + 0.8	
ST, C1, O/Ā CMOS Logic Levels (V_{LS} = V_{DD}, V_{SS} = 0 V)						
Input Current	"1" level	I_{IH}	–	–	+0.3	μA
	"0" level	I_{IL}	−0.3	–	–	
Input Voltage	"1" level, V_{DD} = 10 V	V_{IH}	7.5	5.75	–	V
	"0" level, V_{DD} = 10 V	V_{IL}	–	4.25	3.0	
CO Output Characteristics (V_{DD} = 10, V_{SS} = 0 V)						
TTL Output Voltage (TTL Mode)	"1" level, I_O = 8 mA	V_{OH}	2.4	–	–	V
	"0" level, I_O = 2.5 mA	V_{OL}	–	–	0.8	
CMOS Output Current	V_{DD} = 10 V, V_{OH} = 9.5 V	I_{OH}	−1.3	−2.25	–	mA
	V_{DD} = 10 V, V_{OL} = 0.5 V	I_{OL}	1.1	2.25	–	

ANALOG ELECTRICAL CHARACTERISTICS (V_{DD} = 10 V, V_{AG} = 5 V, V_{SS} = 0 V, T_A = 0 to 70°)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Input Current (V_{AG})	I_I	−50	–	+50	μA
DC Input Current (TxI, RxI)	I_I	−10	–	+10	μA
AC Input Impedance (TxI, RxI)	Z_{in}	0.2	1.0	–	MΩ
Input Voltage Range (TxI, RxI)	V_{in}	V_{SS} + 1.5	–	V_{DD} − 1.5	V

OP-AMP CHARACTERISTICS (V_{DD} = 5 to 10 V, V_{AG} = V_{DD}/2, V_{SS} = 0 V, T_A = 0 to 70°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (AO)	I_{IO}	−50	–	+50	mV
Open Loop Gain (R_L = 10 kΩ)	A_{OL}	–	45	–	dB
Input Bias Current (A+, A−)	I_{IB}	–	±0.1	–	μA
Output Noise (900 Ω)	P_N	–	−3	–	dBrnC
Slew Rate	S_R	–	2	–	V/μs
Output Voltage Swing (R_L = 600 Ω to V_{AG})	–	1.5 V	–	V_{DD} − 1.5 V	V

DIGITAL SWITCHING CHARACTERISTICS (V_{DD} = 5 V, V_{SS} = 0 V, T_A = 25°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Rise and Fall Times	C1, O/A, ST	t_r, t_f	–	–	4	μs
Input Pulse Width	(TTL Mode) O/A	t_w	200	–	–	ns
	(CMOS Mode) C1, O/A, ST	t_w	125	–	–	
Clock Frequency (Driven by External Clock) (C1 Pin)	(CMOS Mode)	f_c	–	1.0	4.0	MHz
Crystal Frequency	C1, C2	f_x	1.0	–	4.0	MHz

LOW-BAND FILTER CHARACTERISTICS (V_{DD} = 10 V, V_{AG} = V_{DD}/2, V_{SS} = 0 V, T_A = 0 to 70°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Full Scale Input Voltage (+3 dBm0)		V_{FS}	2.13	–	–	V_{p-p}
Gain at 1080 Hz, 0 dBm0		A_r	9.0	10.0	11.0	dB
Idle Noise, Input = V_{AG}, 900 Ω load		P_N	–	– 70	– 64	dBmp
Dynamic Range (Full Scale Output/Idle Noise)		DR	72	78	–	dB
Total Harmonic Distortion		THD	–	1.0	–	%
Power Supply Rejection Ratio		PSRR	–	20	–	dB
Pass-Band Ripple	980 Hz to 1180 Hz	–	–	–	2	dBp-p
Pass-band Response, Ref. 980 Hz, 0 dBm0	1180 Hz	–	– 1.5	–	1.5	dB
Rejection (Ref. 1080 Hz)	1650 Hz to 1850 Hz	–	– 55	–	–	dB
Differential Group Delay	980 Hz to 1180 Hz	–	–	–	600	μs

HIGH-BAND FILTER CHARACTERISTICS (V_{DD} = 10 V, V_{AG} = V_{DD}/2, V_{SS} = 0 V, T_A = 0 to 70°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Full Scale Input Voltage (+3 dBm0)		V_{FS}	2.13	–	–	V_{p-p}
Gain at 1750 Hz, 0 dBm0		A_r	9.0	10.0	11.0	dB
Idle Noise, Input = V_{AG}, 900 Ω load		P_N	–	– 70	– 64	dBmp
Dynamic Range (Full Scale Output/Idle Noise)		DR	72	78	–	dB
Total Harmonic Distortion		THD	–	1.0	–	%
Power Supply Rejection Ratio		PSRR	–	20	–	dB
Pass-Band Ripple	1650 Hz to 1850 Hz	–	–	–	2	dBp-p
Pass-band Response, Ref. 1650 Hz, 0 dBm0	1850 Hz	–	– 1.5	–	1.5	dB
Rejection (Ref. 1750 Hz)	980 Hz to 1180 Hz	–	– 55	–	–	dB
Differential Group Delay	1650 Hz to 1850 Hz	–	–	–	600	μs

V_{ref} CHARACTERISTICS (V_{DD} = 5 to 15 V, V_{ref} = V_{DD}/2, V_{SS} = 0 V, T_A = 0 to 70°C)

Characteristic		Symbol	Min	Typ	Max	Unit
V_{ref} Output Voltage	I_O = ± 5 mA	V_{ref}	– 250	± 75	+ 250	mV

3

PIN DESCRIPTIONS

V_{DD} (PIN 18) – Positive power supply.

V_{SS} (PIN 9) – Negative power supply.

V_{AG} (PIN 1) – Analog ground. In single supply applications, V_{AG} is driven from V_{ref}.

V_{ref} (PIN 5) – This pin provides an output DC voltage at approximately $(V_{DD}-V_{SS})/2$ for use as an external analog ground in single supply applications. In symmetric dual power supply applications, V_{ref} is not used.

V_{LS}, LOGIC SHIFT VOLTAGE (PIN 10) – This pin determines the input/output logic level compatibility of O/$\overline{A}$ and CO. When the voltage on this pin is greater than $V_{DD}-0.5$ V and less than V_{DD}, these digital inputs and outputs are CMOS compatible. When the voltage on this pin is less than $V_{DD}-4$ V and greater than V_{SS}, these digital inputs and outputs are TTL compatible, and V_{LS} is connected to digital ground.

C1, C2, CLOCK 1, CLOCK 2 (PIN 7, PIN 8) – These pins connect to an internal crystal oscillator. In operation, a parallel resonant crystal is connected from C1 to C2 as well as a 10 MΩ resistor in parallel with the crystal and 20 pF capacitors from C1 and C2 to V_{SS}. Crystal frequencies of 1.0, 3.6864, or 4.0 MHz may be used. Alternatively, an external CMOS level signal at the crystal frequency may be applied to C1 in lieu of the crystal, capacitors, and resistor. The inverted clock signal will appear at C2 and will be a CMOS output from V_{SS} to V_{DD}.

Clk Sel, CLOCK SELECT (PIN 6) – This pin is a three-state selector used to select one of the three crystal/clock options. When at V_{DD}, V_{AG}, or V_{SS}, this pin selects the 4.0, 3.6864, or 1.0 MHz crystal/clock option, respectively, for C1 and C2.

Clock Select Pin 6	Clock Frequency *	Clock Output Pin 11
V_{DD}	4.0 MHz	1.0 MHz
V_{AG}	3.6864 MHz	N/A
V_{SS}	1.0 MHz	1.0 MHz

*Use either an external clock to drive C1 Pin 7 or external crystal across C1 and C2 Pins 7 and 8

CO, CLOCK OUT (PIN 11) – This provides a 1.0 MHz output clock signal when either the 1.0 or 4.0 MHz clock is selected and is typically used to drive the clock input to a MC14412 or MC6860 modem. The clock output is not usable when the 3.6864 MHz option is used. The logic family compatibility (CMOS or TTL) of this output is determined by V_{LS}.

O/$\overline{A}$, ORIGINATE, ANSWER (PIN 12) – The mode of the device, originate or answer, is selected with this pin. In the originate mode, selected with a logic "1", the low band band-pass filter is switched into the transmit path and the high band band-pass filter is switched into the receive path. In the answer mode, the filters switch position. The input levels of this pin are determined by V_{LS}.

TxI, TRANSMIT INPUT (PIN 3) – TxI is the input to the transmit band-pass filter which is the low band filter in the originate mode and the high band filter in the answer mode. In the self test mode, this input is routed to the appropriate band-pass filter input so as to pass the modulated data to the demodulator.

TxO, TRANSMIT OUTPUT (PIN 2) – This pin is the output of the Tx output amplifier and typically drives the modulated data into the duplexer or hybrid circuit (see ST pin).

RxI, RECEIVE INPUT (PIN 13) – RxI is the input to the receive band-pass filter which is the high band filter in the originate mode and the low band filter in the answer mode. In the self test mode, this input is disabled.

RxO, RECEIVE OUTPUT (PIN 14) – The output of the receive band-pass filter, whether low band or high band, is provided at RxO. Typically, this signal is capacitively coupled to the input of the external carrier detector and limiter. The AC coupling capacitor is required because of the variable DC offset of the receive filter.

ST, SELF TEST (PIN 4) – A "1" on ST puts the device into a self test mode which routes the modulated carrier from TxI, through the appropriate filter,and out RxO back to the receive carrier input of the modem. TxO remains at V_{AG} during a self test operation. This pin is a standard CMOS input regardless of the state of V_{LS}.

A+ (PIN 17) – This is the noninverting input to the spare operational amplifier.

A– (PIN 15) – This is the inverting input to the spare operational amplifier.

AO (PIN 16) – This is the output of the spare operational amplifier.

FUNCTIONAL DESCRIPTION

This device is capable of four basic analog configurations determined by the state of O/$\overline{A}$ and ST. The normal (non-self test) and self test modes in both the answer and originate modes will be discussed.

In the normal originate mode, O/$\overline{A}$ is a "1" and self test, ST, is a "0". When in this mode, the Tx carrier from the modem is input on TxI and routed through the low band band-pass filter. The filter output is switched to the input of the Tx op-amp which typically drives the Tx carrier off chip into a duplexer circuit which could be implemented with the spare operational amplifier. The output of the duplexer drives RxI which is switched to the input of the high band band-pass filter. The filter output is available at RxO which is typically the input to a limiter and carrier detector.

The normal answer mode is established by a "0" on both O/$\overline{A}$ and ST. This mode is identical to the normal originate mode with one exception: the band-pass filters swap positions, i.e., the high band band-pass filter is switched into the transmit path, and the low band band-pass filter is switched into the receive path.

When used with the MC14412 in the self test mode, the device will function as follows. A "1" on the self test pin of both devices enables the self test mode. The modem switches its demodulator to its modulator frequency and demodulates its own modulated carrier. The modem filter switches the transmit carrier of the modem from TxI through the low band filter and out the RxO pin to the limiter when in the originate mode. When the system is in the answer mode, the modulated signal is instead routed through the high-band filter. TxO will remain at mid-supply (V_{AG}) during self test operations.

FIGURE 1 – TEST CIRCUIT

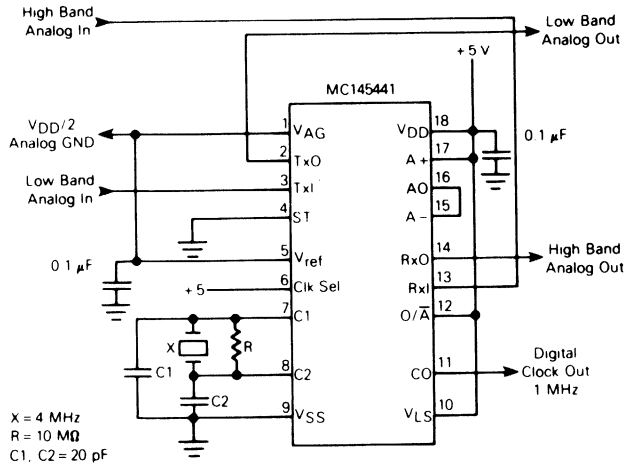


FIGURE 2 – MC145441 FREQUENCY RESPONSE

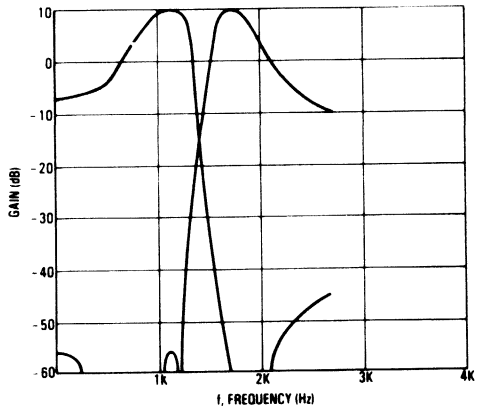
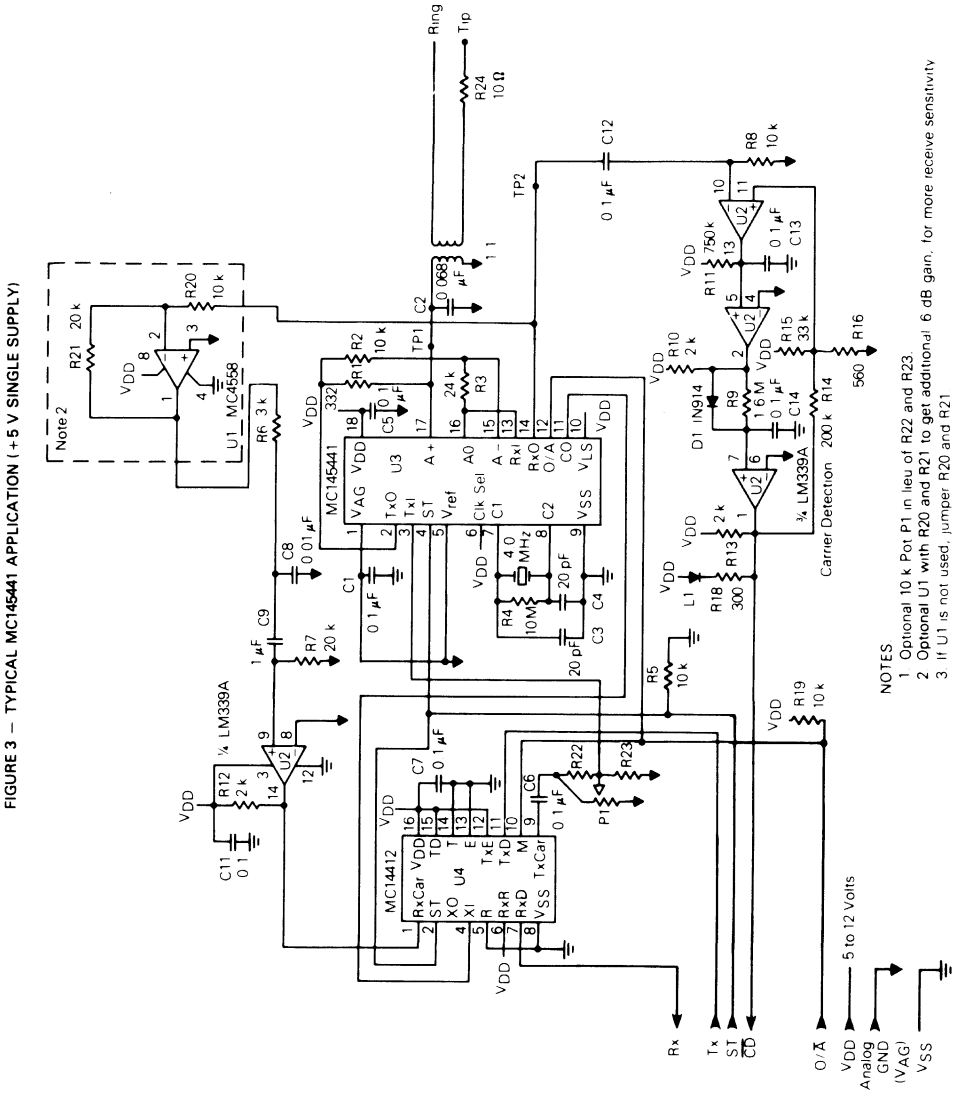


FIGURE 3 – TYPICAL MC145441 APPLICATION (+5 V SINGLE SUPPLY)



MC145442
MC145443

MOTOROLA

Advance Information

Single Chip 300 Baud Modem

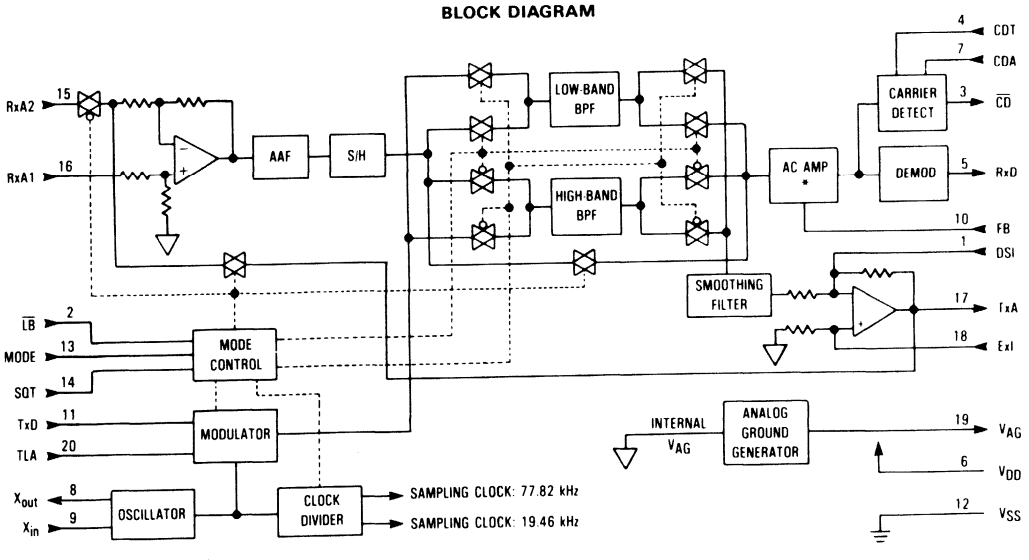
P SUFFIX
PLASTIC
CASE 738

DW SUFFIX
SOIC
CASE 751D

The MC145442 and MC145443 silicon-gate CMOS single-chip low-speed modems contain a complete frequency shift keying (FSK) modulator, demodulator, and filter. These devices are compatible with CCITT V.21 (MC145442) and Bell 103 (MC145443) specifications. Both devices provide full-duplex or half-duplex 300 baud data communicaton over a pair of telephone lines. They also include a carrier detect circuit for the demodulator section and a duplexer circuit for direct operation on a telephone line through a simple transformer.

- MC145442 Compatible with CCITT V.21
- MC145443 Compatible with Bell 103
- Low-Band and High-Band Bandpass Filters On-Chip
- Simplex, Half-Duplex, and Full-Duplex Operation
- Originate and Answer Mode
- Analog Loopback Configuration for Self Test
- Hybrid Network Function On-Chip
- Carrier Detect Circuit On-Chip
- Adjustable Transmit Level and $\overline{CD}$ Delay Timing
- On-Chip Crystal Oscillator (3.579 MHz)
- Single +5 Volt Power Supply Operation
- Internal Mid-Supply Generator
- Power-Down Mode
- Pin Compatible with MM74HC943
- Capable of Driving −9 dBm into a 600-Ohm Load

BLOCK DIAGRAM



*Refer to the FB pin description.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ADI1269

3

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0.5 to 7.0	V
DC Input Voltage	V_{in}	−0.5 to V_{DD} + 0.5	V
DC Output Voltage	V_{out}	−0.5 to V_{DD} + 0.5	V
Clamp Diode Current, per Pin	I_{IK}, I_{OK}	± 20	mA
DC Output Current, per Pin	I_{out}	± 28	mA
Power Dissipation	PD	500	mW
Operating Temperature Range	T_A	−40 to 85	°C
Storage Temperature Range	T_{stg}	−65 to 150	°C

This device contains circuitry to protect against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused outputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{DD}	4.5	5.5	V
DC Input or Output Voltage	V_{in}, V_{out}	0	V_{DD}	V
Input Rise or Fall Time	t_r, t_f	–	500	ns
Crystal Frequency*	$f_{crystal}$	3.2	5.0	MHz

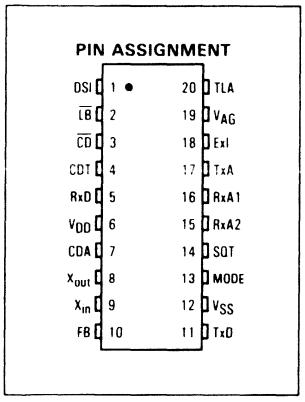
*Changing the crystal frequency from 3.579 MHz will change the output frequencies. The change in output frequency will be proportional to the change in crystal frequency.

DC ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0 V ± 10%, T_A = −40 to 85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
High-Level Input Voltage	$\overline{LB}$	V_{IH}	V_{DD} − 0.8	–	–	V
	X_{in}, TxD, Mode, SQT		3.15	–	–	
Low-Level Input Voltage	$\overline{LB}$	V_{IL}	–	–	0.8	V
	X_{in}, TxD, Mode, SQT		–	–	1.1	
High-Level Output Voltage		V_{OH}				V
I_{OH} = 20 μA	$\overline{CD}$, RxD		V_{DD} − 0.1	–	–	
I_{OH} = 2 mA	$\overline{CD}$, RxD		3.7	–	–	
I_{OH} = 20 μA	X_{out}		–	V_{DD} − 0.05	–	
Low-Level Output Voltage		V_{OL}				V
I_{OL} = 20 μA	$\overline{CD}$, RxD		–	–	0.1	
I_{OL} = 2 mA	$\overline{CD}$, RxD		–	–	0.4	
I_{OL} = 20 μA	X_{out}		–	0.05	–	
Input Current	$\overline{LB}$, TxD, Mode, SQT	I_{in}	–	–	± 1.0	μA
	RxA1, RxA2		–	10	± 12	
	X_{in}		–	–	± 10	
Quiesent Supply Current X_{in} or $f_{crystal}$ = 3.579 MHz		I_{DD}	–	7	10	mA
Power-Down Supply Current			–	200	300	μA
Input Capacitance	X_{in}	C_{in}	–	10	–	pF
	All Other Inputs		–	–	10	
V_{AG} Output Voltage (I_O = ± 10 μA)		V_{AG}	2.4	2.5	2.6	V
CDA Output Voltage (I_O = ± 10 μA)		V_{CDA}	1.1	1.2	1.3	V
Line Driver Feedback Resistor		R_f	10	20	30	kΩ

AC ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0 V ± 10%, T_A = −40 to 85°C, Crystal Frequency = 3.579 MHz ± 0.1%; See Figure 1)

Characteristic		Min	Typ	Max	Unit
TRANSMITTER					
Power Output on TxA RL = 1.2 kΩ, R_{TLA} = ∞ RL = 1.2 kΩ, R_{TLA} = 5.5 kΩ		 −13 −10	 −12 −9	 −11 −8	dBm
Second Harmonic Power RL = 1.2 kΩ		—	−56	—	dBm
RECEIVE FILTER AND HYBRID					
Hybrid Input Impedance RxA1, RxA2		40	50	—	kΩ
FB Output Impedance		—	16	—	kΩ
Adjacent Channel Rejection		−48	—	—	dBm
DEMODULATOR					
Receive Carrier Amplitude		−48	—	−12	dBm
Dynamic Range		—	36	—	dB
Bit Jitter (S/N = 30 dB, Input = −38 dBm, Bit Rate = 300 baud)		—	100	—	μs
Bit Bias		—	5	—	%
Carrier Detect Threshold (CDA = 1.2 V or CDA grounded through a 0.1 μF capacitor)	On to Off Off to On	— —	−44 −47	— —	dBm



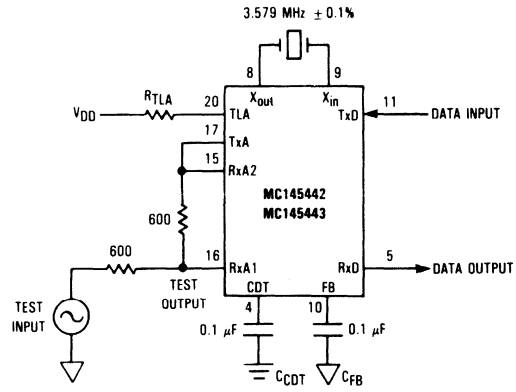


Figure 1. AC Characteristics Evaluation Circuit

PIN DESCRIPTIONS

V_{DD} – POSITIVE POWER SUPPLY (PIN 6)

This pin is normally tied to 5.0 V.

V_{SS} – NEGATIVE POWER SUPPLY (PIN 12)

This pin is normally tied to 0 V.

V_{AG} – ANALOG GROUND (PIN 19)

Analog ground is internally biased to ($V_{DD} - V_{SS}$)/2. This pin must be decoupled by a capacitor from V_{AG} to V_{SS} and a capacitor from V_{AG} to V_{DD}. Analog ground is the common bias line used in the switched capacitor filters, limiter, and slicer in the demodulation circuitry.

TLA – TRANSMIT LEVEL ADJUST (PIN 20)

This pin is used to adjust the transmit level. Transmit level adjustment range is typically from −12 dBm to −9 dBm. (See Applications Information.)

TxD – TRANSMIT DATA (PIN 11)

Binary information is input to the transmit data pin. Data entered for transmission is modulated using FSK techniques. A logic high input level represents a mark and a logic low represents a space. (See Table 1.)

Table 1. Bell 103 and CCITT V.21 Frequency Characteristics

Bell 103 (MC145443)				
Data	Originate Mode		Answer Mode	
	Transmit	Receive	Transmit	Receive
Space	1070 Hz	2025 Hz	2025 Hz	1070 Hz
Mark	1270 Hz	2225 Hz	2225 Hz	1270 Hz
CCITT V.21 (MC145442)				
Data	Originate Mode		Answer Mode	
	Transmit	Receive	Transmit	Receive
Space	1180 Hz	1850 Hz	1850 Hz	1180 Hz
Mark	980 Hz	1650 Hz	1650 Hz	980 Hz

NOTE: Actual frequencies may be ±5 Hz assuming a 3.579545 MHz crystal is used.

3

TxA—TRANSMIT CARRIER (PIN 17)

This is the output of the line driver amplifier. The transmit carrier is the digitally synthesized sine wave output of the modulator derived from a crystal oscillator reference. When a 3.579 MHz crystal is used the frequency outputs shown in Table 1 apply. (See Applications Information.)

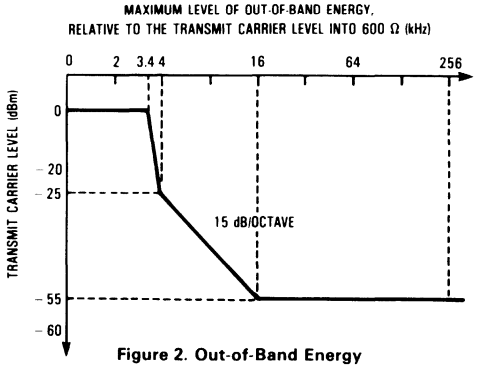


Figure 2. Out-of-Band Energy

ExI—EXTERNAL INPUT (PIN 18)

The external input is the noninverting input to the line driver. It is provided to combine an auxiliary audio signal or speech signal to the phone line using the line driver. This pin should be connected to V_{AG} if not used. The average level must be the same as V_{AG} to maintain proper operation. (See Applications Information.)

DSI—DRIVER SUMMING INPUT (PIN 1)

The driver summing input may be used to connect an external signal, such as a DTMF dialer, to the phone line. A series resistor, R_{DSI}, is needed to define the voltage gain A_V (see Applications Information and Figure 6). When applying a signal to the DSI pin, the modulator should be squelched by bringing SQT (pin 14) to a logic high level. The voltage gain, A_V, is calculated by the formula $A_V = -R_f/R_{DSI}$ (where $R_f \approx 20\ k\Omega$). For example, a 20 kΩ resistor for R_{DSI} will provide unity gain ($A_V = -20\ k\Omega/20\ k\Omega = -1$). This pin MUST be left OPEN if not used.

RxD—RECEIVE DATA (PIN 5)

The receive data output pin presents the digital binary data resulting from the demodulation of the receive carrier. If no carrier is present, $\overline{CD}$ high, the receive data output (RxD) is clamped high.

RxA2, RxA1—RECEIVE CARRIER (PINS 15, 16)

The receive carrier is the FSK input to the demodulator through the receive band-pass filter. RxA1 is the noninverting input and RxA2 is the inverting input of the receive hybrid (duplexer) operational amplifier.

$\overline{LB}$—ANALOG LOOPBACK (PIN 2)

When a high level is applied to this pin (SQT must be low), the analog loopback test is enabled. The analog loopback test connects the TxA pin to the RxA2 pin and the RxA1 to analog ground. In loopback, the demodulator frequencies are switched to the modulation frequencies for the selected mode. (See Tables 1 and 2 and Figures 4c and 4d.)

When $\overline{LB}$ is connected to analog ground (V_{AG}), the modulator generates an echo cancellation tone of 2100 Hz for MC145442 CCITT V.21 and 2225 Hz for MC145443 Bell 103 systems. For normal operation, this pin should be at a logic low level (V_{SS}).

The power-down mode is enabled when both $\overline{LB}$ and SQT are connected to a logic high level. (See Table 2.)

Table 2. Functional Table

MODE Pin 13	SQT Pin 14	$\overline{LB}$ Pin 2	Operating Mode
1	0	0	Originate Mode
0	0	0	Answer Mode
X	0	V_{AG} ($V_{DD}/2$)	Echo Tone
X	0	1	Analog Loopback
X	1	0	Squelch Mode
X	1	V_{AG} ($V_{DD}/2$)	Squelch Mode
X	1	1	Power Down

MODE—MODE (PIN 13)

This input selects the pair of transmit and receive frequencies used during modulation and demodulation. When a logic high level is placed on this input, originate (Bell) or channel 1 (CCITT) is selected. When a low level is placed on this input, answer (Bell) or channel 2 (CCITT) is selected. (See Tables 1 and 2 and Figure 4.)

CDT—CARRIER DETECT TIMING (PIN 4)

A capacitor on this pin to V_{SS} sets the amount of time the carrier must be present before $\overline{CD}$ goes low. (See Applications Information for the capacitor values.)

$\overline{CD}$ – CARRIER DETECT OUTPUT (PIN 3)

This output is used to indicate when a carrier has been sensed by the carrier detect circuit. This output goes to a logic low level when a valid signal above the minimum threshold level (defined by CDA pin 7) is maintained on the input to the hybrid circuit longer than the response time (defined by CDT pin 4). This pin is held at the logic low level until the signal falls below the maximum threshold level for longer than the turn off time. (See Applications Information and Figure 5.)

CDA – CARRIER DETECT ADJUST (PIN 7)

An external voltage may be applied to this pin to adjust the carrier detect threshold. The threshold hysteresis is internally fixed at 3 dB. (See Applications Information.)

X_{out}, X_{in} – CRYSTAL OSCILLATOR (PINS 8, 9)

A crystal reference oscillator is formed when a 3.579 MHz crystal is connected between these two pins. X_{out} (pin 8) is the output of the oscillator circuit, and X_{in} (pin 9) is the input to the oscillator circuit. When using an external clock, apply the clock to the X_{in} (pin 9) pin and leave X_{out} (pin 8) open. An internal 10 mΩ resistor and internal capacitors, typically 10 pF on X_{in} and 16 pF on X_{out}, allow the crystal to be connected without any other external components. Printed circuit board layout should keep external stray capacitance to a minimum.

FB – FILTER BIAS (PIN 10)

This is the negative input to the ac amplifier. In normal operation, this pin is connected to analog ground through a 0.1 μF bypass capacitor in order to cancel the input offset voltage of the limiter. It has a nominal input impedance of 16 kΩ. (See Figure 3.)

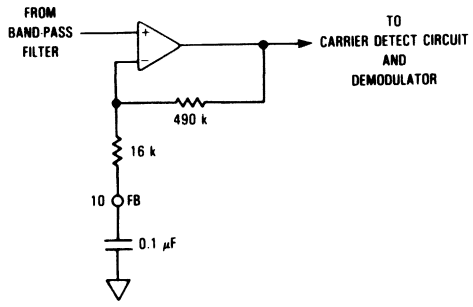


Figure 3. AC Amplifier Circuit

SQT – TRANSMIT SQUELCH (PIN 14)

When this input pin is at a logic high level, the modulator is disabled. The line driver remains active if $\overline{LB}$ is at a logic low level. (See Table 2.)

When both $\overline{LB}$ and SQT are connected to a logic high level, see Table 2, the entire chip is in a power down state and all circuitry except the crystal oscillator is disabled. Total power supply current decreases from 10 mA (maximum) to 300 μA (maximum).

GENERAL DESCRIPTION

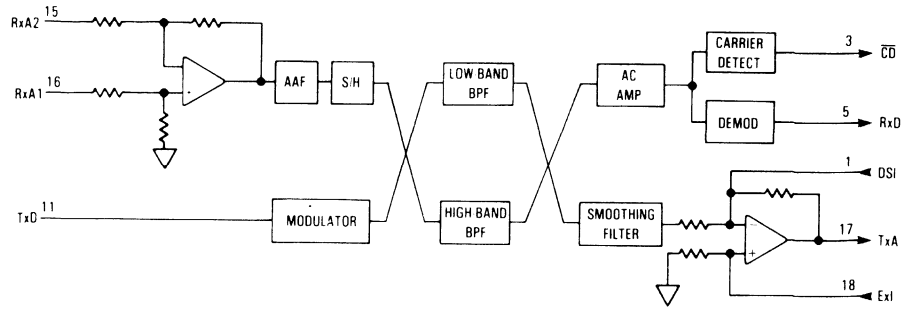
The MC145442 and MC145443 are full-duplex low-speed modems. They provide a 300 baud FSK signal for bidirectional data transmission over the telephone network. They can be operated in one of four basic configurations as determined by the state of MODE (pin 13) and $\overline{LB}$ (pin 2). The normal (non-loopback) and self test (loopback) modes in both answer and originate modes will be discussed.

For an originate or channel 1 mode, a logic high level is placed on MODE (pin 13) and a logic low level is placed on $\overline{LB}$ (pin 2). In this mode, transmit data is input on TxD, where it is converted to a FSK signal and routed through a low-band band-pass filter. The filtered output signal is then buffered by the Tx op-amp line driver, which is capable of driving −9 dBm onto a 600 Ω line. The receive signal is connected through a hybrid duplexer circuit on pins 15 and 16, RxA2 and RxA1. The signal then passes through the anti-aliasing filter, the sample-and-hold circuit, is switched into the high-band band-pass filter, and then switched into the ac amplifier circuit. The output of the ac amplifier circuit is routed to the demodulator circuit and demodulated. The resulting digital data is then output through RxD (pin 5). The carrier detect circuit receives its signal from the output of the ac amplifier circuit and goes low when the incoming signal is detected. (See Figure 4a.)

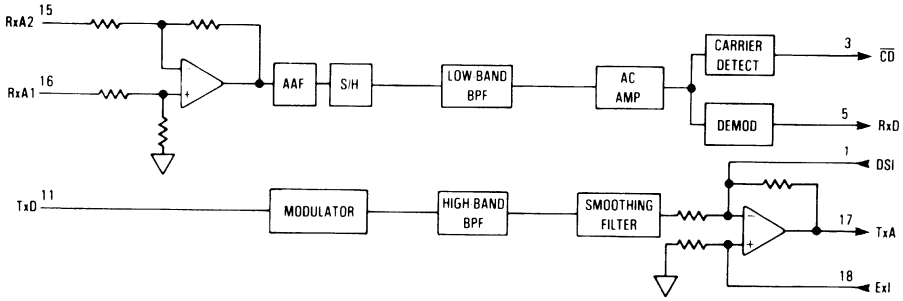
In the answer or channel 2 mode, a logic low level is placed on MODE (pin 13) and on $\overline{LB}$ (pin 2). In this mode, the data follows the same path except the FSK signal is routed to the high-band band-pass filter and the sample-and-hold signal is routed through the low-band band-pass filter. (See Figure 4b.)

In the analog loopback originate or channel 1 mode, a logic high level is placed on MODE (pin 13) and on $\overline{LB}$ (pin 2). This mode is used for a self check of the modulator, demodulator, and low-band pass-band filter circuit. The modulator side is configured exactly like the originate mode above except the line driver output (TxA pin 17) is switched to the negative input of the hybrid op-amp. The RxA2 input pin is open in this mode and the noninverting input of the hybrid circuit is connected to V_{AG}. The sample-and-hold output bypasses the filter so that the demodulator receives the modulated Tx data (see Figure 4c). This test checks all internal device components except the high-band band-pass filter which can be checked in the answer or channel 2 mode loopback test.

In the analog loopback answer or channel 2 mode, a logic low level is placed on MODE (pin 13) and a logic high level on $\overline{LB}$ (pin 2). This mode is used for a self check of the modulator, demodulator, and high-band pass-band filter circuit. This configuration is exactly like the originate loopback mode above, except the signal is routed through the high-band pass-band filter. (See Figure 4d.)

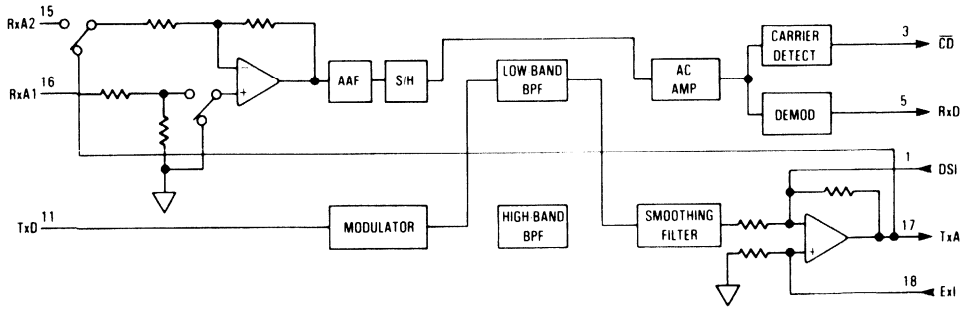


(a) ORIGINATE/CHANNEL 1 MODE (MODE = HIGH, $\overline{LB}$ = LOW)

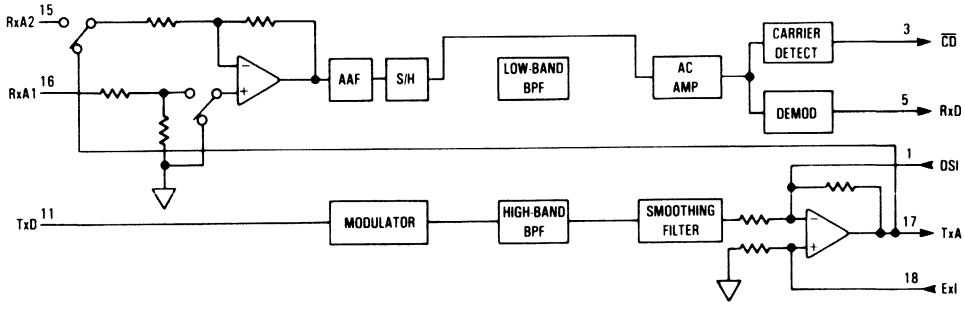


(b) ANSWER/CHANNEL 2 MODE (MODE = LOW, $\overline{LB}$ = LOW)

Figure 4. Basic Operating Modes



(c) ORIGINATE/CHANNEL 1 MODE AND ANALOG LOOPBACK STATE (MODE = HIGH, $\overline{LB}$ = HIGH)



(d) ANSWER/CHANNEL 2 MODE AND ANALOG LOOPBACK STATE (MODE = LOW, $\overline{LB}$ = HIGH)

Figure 4. Basic Operating Modes

APPLICATIONS INFORMATION

CARRIER DETECT TIMING ADJUSTMENT

The value of a capacitor, C_{CDT} at CDT (pin 4) determines how long a received modem signal must be present above the minimum threshold level before $\overline{CD}$ (pin 3) goes low. The C_{CDT} capacitor also determines how long the $\overline{CD}$ pin stays low after the received modem signal goes below the minimum threshold. The $\overline{CD}$ pin is used to distinguish a strong modem signal from random noise. The following equations show the relationship between t_{CDL}, the time in seconds required for $\overline{CD}$ to go low; t_{CDH}, the time in seconds required for $\overline{CD}$ to go high; and C_{CDT}, the capacitor value in μF.

Valid signal to $\overline{CD}$ response time: $t_{CDL} \approx 6.4 \times C_{CDT}$

Invalid signal to $\overline{CD}$ off time: $t_{CDH} \approx 0.54 \times C_{CDT}$

Example: $t_{CDL} \approx 6.4 \times 0.1\ \mu F \approx 0.64$ seconds

$t_{CDH} \approx 0.54 \times 0.1\ \mu F \approx 0.054$ seconds

CARRIER DETECT THRESHOLD ADJUSTMENT

The carrier detect threshold is set by internal resistors to activate $\overline{CD}$ with a typical −44 dBm (into 600 Ω) signal and deactivate $\overline{CD}$ with a typical −47 dBm signal applied to the input of the hybrid circuit. The carrier detect threshold level can be adjusted by applying an external voltage on CDA (pin 7). The following equations may be used to find the CDA voltage required for a given threshold voltage. (V_{on} and V_{off} are in volts RMS.)

$$V_{CDA} = 244 \times V_{on}$$

$$V_{CDA} = 345 \times V_{off}$$

Example (internally set)

$V_{on} = 4.9$ mV ≈ −44 dBm: $V_{CDA} = 244 \times 4.9$ mV = 1.2 V

$V_{off} = 3.5$ mV ≈ −47 dBm: $V_{CDA} = 345 \times 3.5$ mV = 1.2 V

Example (externally set):

$V_{on} = 7.7$ mV ≈ −40 dBm: $V_{CDA} = 244 \times 7.7$ mV = 1.9 V

$V_{off} = 5.4$ mV ≈ −43 dBm: $V_{CDA} = 345 \times 5.4$ mV = 1.9 V

The CDA pin has an approximate Thevenin equivalent voltage of 1.2 V and an output impedance of 100 kΩ. When using the internal 1.2 volt reference a 0.1 μF capacitor should be connected between this pin and V_{SS}. (See Figure 5.)

TRANSMIT LEVEL ADJUSTMENT

The power output at TxA (pin 17) is determined by the value of resistor R_{TLA} that is connected between TLA (pin 20) to V_{DD} (pin 6). Table 3 shows the R_{TLA} values and the corresponding power output for a 600 Ω load. The voltage at TxA is twice the value of that at ring and tip because TxA feeds the signal through a 600 Ω resistor R_{Tx} to a 600 Ω line transformer. (See Figure 7.) When choosing resistor R_{TLA}, keep in mind that −9 dBm is the maximum output level allowed from a modem onto the telephone line (in the U.S.). In addition, keep in mind that maximizing the power output from the modem optimizes the signal-to-noise ratio, improving accurate data transmission.

Table 3. Transmit Level Adjust

Output Transmit Level (Typical into 600 Ω)	R_{TLA}
−12 dBm	∞
−11 dBm	19.8 kΩ
−10 dBm	9.2 kΩ
−9 dBm	5.5 kΩ

THE LINE DRIVER

The line driver is a power amplifier used for driving the telephone line. Both the inverting and noninverting input to the line driver are available for transmitting externally generated tones.

ExI (pin 18) is the noninverting input to the line driver and gives a fixed gain of 2 (R_i = 50 kΩ). The average signal level must be the same as V_{AG} to maintain proper operation. This pin should be connected to V_{AG} if not used.

The driver summing input (DSI, pin 1) may be used to connect an external signal, such as a DTMF dialer, to the phone line. When applying a signal to the DSI pin, the modulator should be squelched by bringing SQT (pin 14) to a logic high level. DSI MUST be left OPEN if not used.

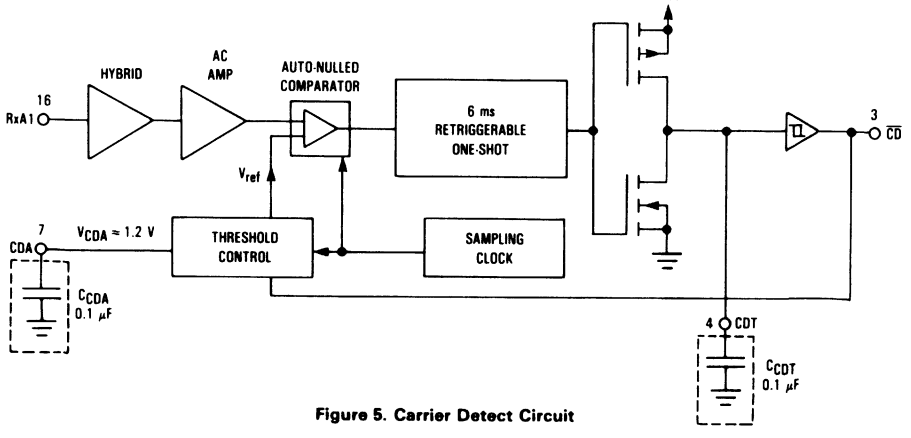


Figure 5. Carrier Detect Circuit

In addition, the DSI pin is the inverting side of the line driver and allows adjustable gain with a series resistor R_{DSI}. (See Figure 6.) The voltage gain, A_V, is determined by the equation:

$$A_V = -\frac{R_f}{R_{DSI}}$$

where $R_f \approx 20\ k\Omega$.

Example: A resistor value of 20 kΩ for R_{DSI} will provide unity gain.

$$A_V = -(20\ k\Omega / 20\ k\Omega) = -1$$

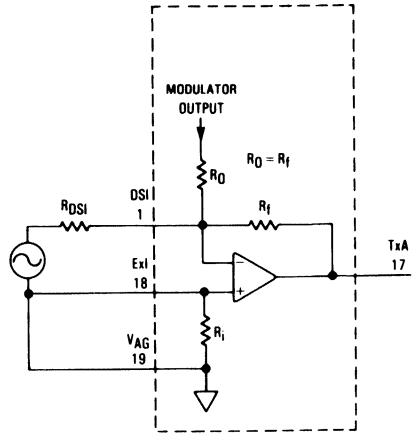
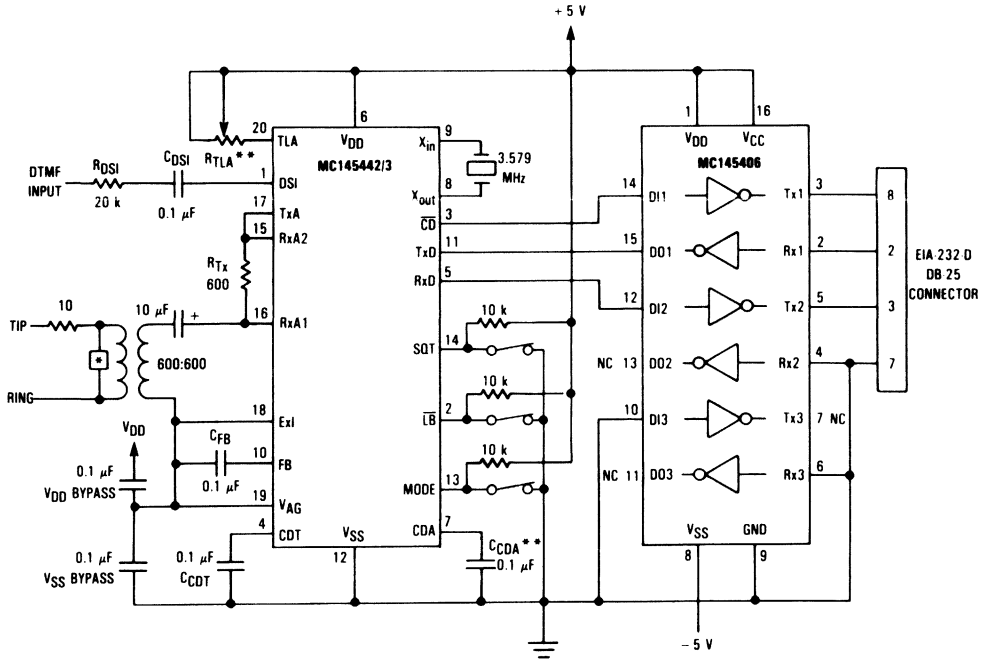


Figure 6. Line Driver Using the DSI Input



*Line protection circuit
**Refer to the applications information for values of C_{CDA} and R_{TLA}

Figure 7. Typical MC145442/MC145443 Applications Circuit

MOTOROLA

MC145445

CMOS

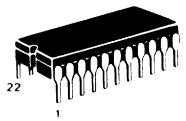
300 BAUD FSK MODEM

3

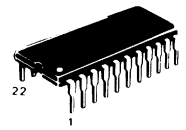
0–300 BAUD FSK MODEM

The MC145445 is a silicon-gate CMOS frequency shift keying (FSK) modem intended for use in Bell 103/113 and CCITT V.21 applications. Features of the device include:

- Bell 103/113 Answer and Originate Compatible, 0-300 Baud
- CCITT V.21 Modes 1 and 2 Compatible, 0-300 Baud
- Eight Selectable $\overline{RTS}$ to $\overline{CTS}$ Delay Options
- Answer-Back Tone Generator (U.S. and CCITT Tones)
- Carrier Detect Input
- TTL Compatible
- 22 Pin Package
- Compatible to the MC145440 Bell 103 or MC145441 CCITT V.21 Modem Filter

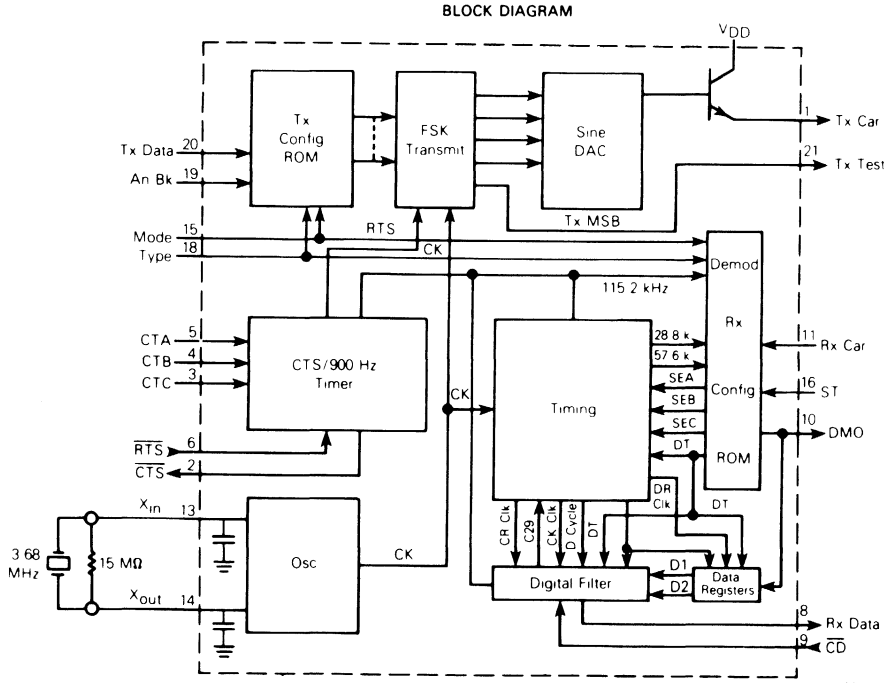


L SUFFIX
CERAMIC PACKAGE
CASE 736



P SUFFIX
PLASTIC PACKAGE
CASE 708

MC145445 300 BAUD FSK MODEM BLOCK DIAGRAM



DS9888

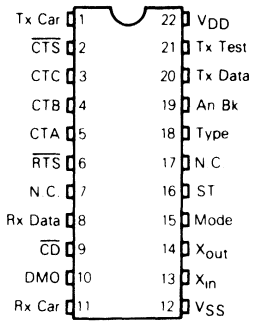
ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	10	V
Input Voltages, All Inputs	V_{in}	V_{SS} – 0.5 to V_{DD} + 0.5	V
DC Current Drain per Pin Pin 3-6, 9, 15, 16, 18, 19, 20 Pins 2, 8	I_{out}	 10 35	mA
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	$V_{DD} - V_{SS}$	4.5	5.0	6.5	V

PIN ASSIGNMENTS



DC ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0 V ±5%, V_{SS} = 0, 0°C ≤ T_A ≤ 70°C)

Characteristics	Symbol	Min	Typ	Max	Unit
Input High Voltage	V_{IH}	–	–	–	V
Pins 3-6, 9, 15, 16, 18, 19, 20	–	2.8	–	–	
Pin 13, 11	–	4.0	–	–	
Input Low Voltage	V_{IL}	–	–	–	V
Pin 3-6, 9, 15, 16, 18, 19, 20	–	–	–	0.5	
Pin 13, 11	–	–	–	0.6	
Input Current	I_{in}	–	–	–	μA
All Inputs (V_{IL} 0 V)	–	–	–	– 5.0	
All Inputs Except Pins 11, 13, (V_{IH} > 2.8 V) (Note 1)	–	–	–	500	
Output High Current (V_{OH} = 2.4 V)	I_{OH}	–	–	–	mA
Pins 2, 8 (Test Load A)	–	0.75	–	–	
Pins 10, 21 (Test Load B)	–	0.75	–	–	
Output Low Current (V_{OL} = 0.4 V)	I_{OL}	–	–	–	mA
Pins 2, 8 (Test Load A)	–	1.2	–	–	
Pins 10, 21 (Test Load B)	–	0.6	–	–	
Operating Current	I_{DD}	–	2.5	6	mA
Input Capacitance	C_{in}	–	–	–	pF
All Except Pin 13	–	–	–	12	
Pin 13 (X_{in})	–	–	8	–	
Output Capacitance	C_{out}	–	–	–	pF
All Except Pin 14	–	–	–	12	
Pin 14 (X_{out})	–	–	13	–	
Transmit Audio Signal Level (Pin 1 R_L = 10 kΩ (Note 2)	–	0.428	0.5	0.578	Vp-p
Total Harmonic Distortion (2nd to 14th) (Note 2)	THD	–	– 50	– 40	dB

AC ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0 V ±5%, V_{SS} = 0, 0°C ≤ T_A ≤ 70°C)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Rise Time (Test Load A) (Pins 2, 8)	t_r	–	20	100	ns
Output Rise Time (Test Load B) (Pins 10, 14, 21)	t_r	–	20	100	ns
Output Fall Time (Test Load A) (Pins 2, 8)	t_f	–	20	100	ns
Output Fall Time (Test Load B) (Pins 10, 14, 21)	t_f	–	20	100	ns
Input Rise and Fall Times (Except Pin 13)	t_r, t_f	–	–	1000	μs
Delay From $\overline{RTS}$ to $\overline{CTS}$	t_d	–	1	–	μs

NOTES:

1. Active pull-up devices are used on these inputs to allow interfacing to TTL devices. The I_{in} specified is a transitional load (not steady state) which is drawn when the input is brought up to 2.8 V until the internal pull-up device has raised the signal to the V_{DD} level.
2. Measured in any mode using HP-3555B dB meter (or equivalent) with 3 kHz flat filtering.

PIN DESCRIPTIONS

V_{DD}, POSITIVE POWER SUPPLY (PIN 22)
This is nominally 5.0 V.

V_{SS}, NEGATIVE POWER SUPPLY (PIN 12)
This is usually 0 volts.

Tx Car, TRANSMIT CARRIER (PIN 1)
The transmit carrier output is a 16 step digitally-synthesized sine wave with an amplitude of 0.1 V_{DD} (p-p) (± 10%) and offset by a dc bias of 0.5 V_{DD} (± 10%). The output load should be 10 kilohms or greater.

$\overline{CTS}$, CLEAR TO SEND (PIN 2)
The clear to send output goes low in response to a high-to-low translation of $\overline{RTS}$ following a selected delay (see CTA, CTB, CTC pin description). This output goes high immediately after loss of $\overline{RTS}$. During the time following activation of $\overline{RTS}$ and before the activation of $\overline{CTS}$, Tx Data should be held in the mark condition.

CTA, CLEAR TO SEND SELECT A (PIN 5)
CTB, CLEAR TO SEND SELECT B (PIN 4)
CTC, CLEAR TO SEND SELECT C (PIN 3)

For delay times for clear to send delay select inputs, see Table 1.

$\overline{RTS}$, REQUEST TO SEND (PIN 6)
The request to send input controls data transmission from the modulator. A low level enables the modulator output and a high level will disable the modulator. See Figure 1.

N.C., NO CONNECTION (PINS 7 AND 17)
These pins are not bonded internally. They should be left open in normal operation.

Rx Data, RECEIVE DATA (PIN 8)
The receive data output is the serial data output from the demodulator. Rx Data is clamped high when $\overline{CD}$ is not active.

$\overline{CD}$, CARRIER DETECT (PIN 9)
When carrier detect input is high (1), the Rx Data output will be clamped to a high state. When carrier detect is low (0), Rx Data output demodulates the Rx carrier input signal.

DMO, DEMODULATOR OUTPUT (PIN 10)
The demodulator output is the output of the differential delay detector. It is used for production testing of the demodulator. In normal operation, this pin should be left open.

Rx Car, RECEIVER CARRIER (PIN 11)
The receiver carrier input is the FSK input to the demodulator. This signal should be the hard-limited output of the receive filter, nominally 50%.

X_{in}, OSCILLATOR INPUT (PIN 13)
X_{out}, OSCILLATOR OUTPUT (PIN 14)
X_{in} should be driven from either an AT-cut crystal or a digital signal source at 3.6864 MHz ±0.01%. When driven by a crystal, a 15 megohm resisitor should be connected from X_{in} to X_{out} in parallel with the crystal.

MODE (PIN 15)
The mode pin selects the pair of frequencies used during modulation and demodulation. A "0" on this pin selects answer mode when Bell type is selected or channel 2 when CCITT type is selected. A "1" on this pin selects originate mode when Bell type is selected or channel 1 when CCITT type is selected.

ST, SELF TEST (PIN 16)
When a high level is placed on this pin, the demodulator is switched to the modulator frequencies (as determined by Mode and Type pins). The modulator should be looped back through the receive filter to the demodulator for self test (echo back). Loopback can be done using a hardwire scheme, or automatically using the internal loopback feature of the filter, such as found on the MC145440/41.

TYPE (PIN 18)
This pin is used to select between Bell 103/113 type operation and CCITT V.21 operation. When the type input pin is a "1", Bell operation is selected. When the type input pin is a "0", the CCITT standard is selected.

An Bk, ANSWER BACK (PIN 19)
The answer back input causes the answer back tone to be transmitted. The answer back tone is 2025 Hz for the Bell mode and 2100 Hz for the CCITT modes. When a high level is placed on the An Bk input pin, the Tx Car pin will output an answer back tone and $\overline{CTS}$ will go to a high state, regardless of the state of $\overline{RTS}$ (see Figure 1).

Tx Data, TRANSMIT DATA (PIN 20)
The transmit data input is the serial input to the modulator. A high level causes a mark frequency to be transmitted, a low level causes a space frequency to be transmitted.

Tx Test, TRANSMIT TEST (PIN 21)
The transmit test output is a square wave representation of the modulator transmit frequency. It is used for test purposes and should be left open in normal operation.

FIGURE 1 – An Bk AND $\overline{RTS}$-$\overline{CTS}$ TIMING

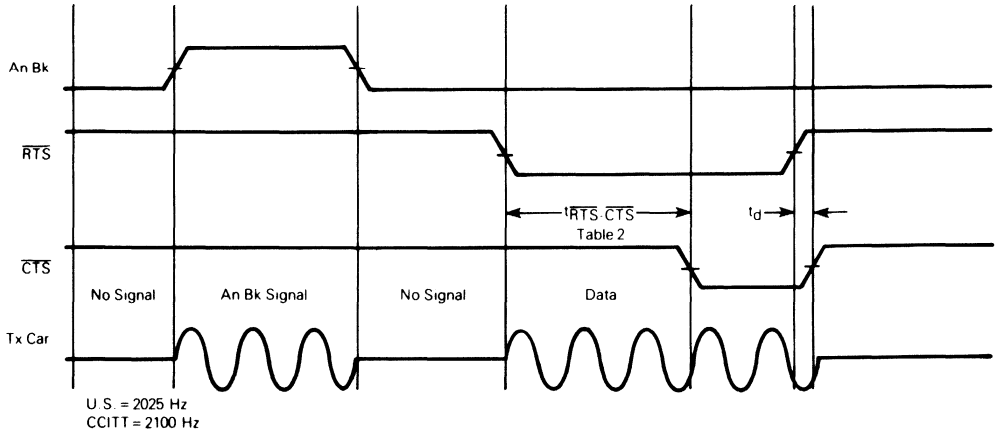


TABLE 1 – $\overline{RTS}$-$\overline{CTS}$ DELAY TIMES

CTC	CTB	CTA	Delay*
0	0	0	0 ms
0	0	1	26.7 ms
0	1	0	40.0 ms
0	1	1	60.0 ms
1	0	0	133.3 ms
1	0	1	213.3 ms
1	1	0	266.7 ms
1	1	1	426.6 ms

*All delays are ±1.7 ms

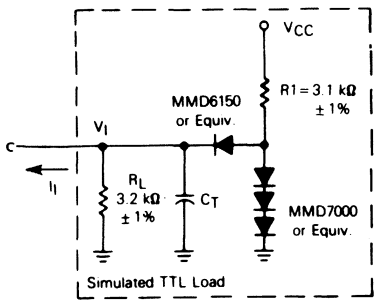
TABLE 2 – OPERATING MODES

Type	Mode	Transmit Data	Transmit Frequency Spec	Transmit Frequency Actual	Application
0	0	0	1850	1850.6	CCITT V.21
		1	1650	1650.13	0-300 Baud, Channel 2
0	1	0	1180	1180.03	CCITT V.21
		1	980	979.9	0-300 Baud, Channel 1
1	0	0	2025	2025.5	Bell 103
		1	2225	2226.09	0-300 Baud, Answer Mode
1	1	0	1070	1069.76	Bell 103
		1	1270	1270.3	0-300 Baud, Originate Mode

Data = 0 = Space
= 1 = Mark

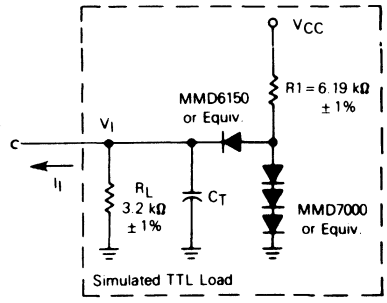
Crystal Frequency = 3.6864 MHz

FIGURE 2 – OUTPUT TEST LOAD A



C_T = 20 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

FIGURE 3 – OUTPUT TEST LOAD B



C_T = 20 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

3

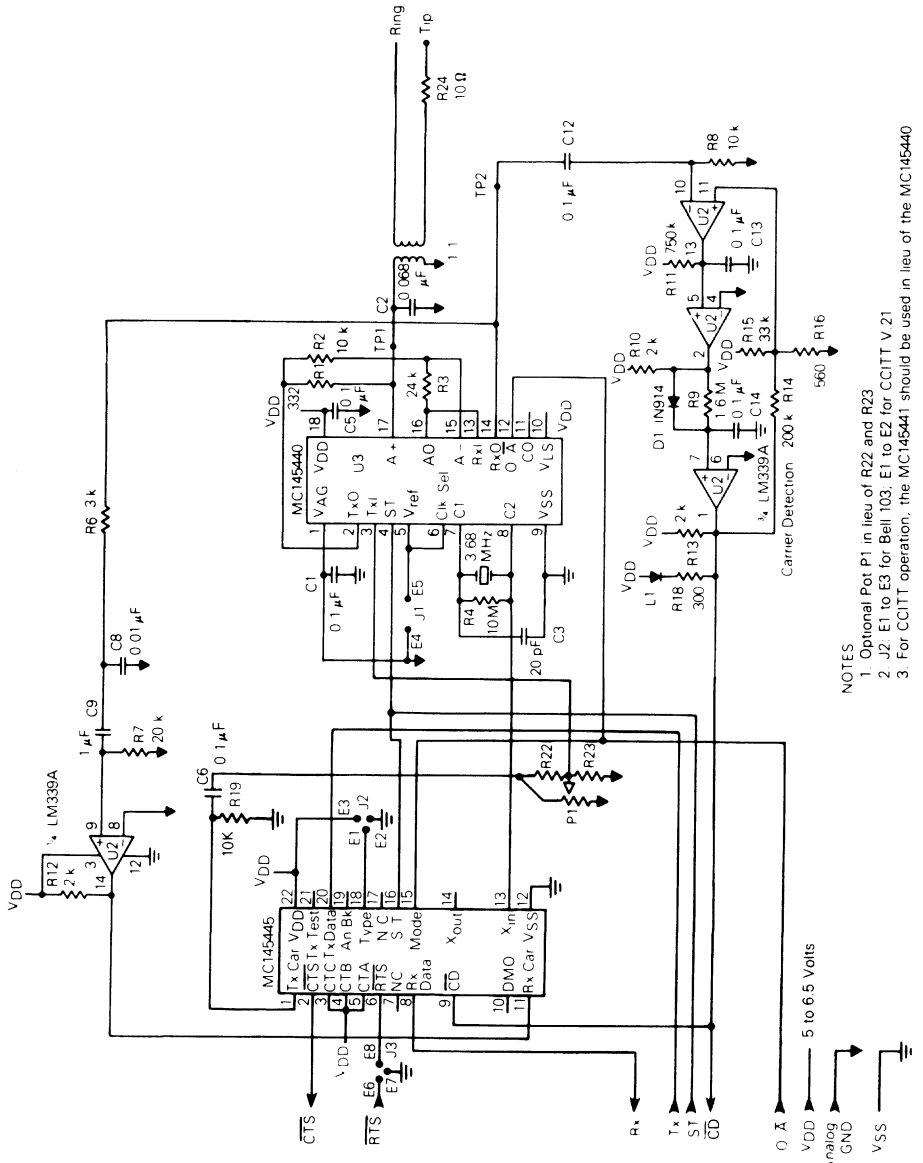


FIGURE 4 — TYPICAL BELL 103/113 ORIGINATE/ANSWER MODEM

MOTOROLA

MC145450

Advance Information

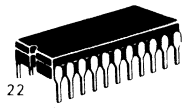
1200 BAUD FSK MODEM

The MC145450 is a silicon-gate CMOS frequency shift keying (FSK) modem intended for use in Bell 202 and CCITT V.23 applications. Features of the device include

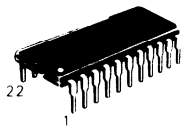
- Bell 202 Compatible 0 to 1800 Baud Main Channel
- 0 to 150 Baud Reverse Channel
- CCITT V.23 Mode 2 Compatible 0 to 1800 Main Channel
- CCITT V.23 0 to 75 Baud Compatible Reverse Channel
- TTL Compatible
- Eight Selectable $\overline{RTS}$-$\overline{CTS}$ Delay Options
- Soft Turn-Off Capability
- Answer Back Tone Generator (US and CCITT Tones)
- Carrier Detect Input
- 22 Pin Package

CMOS

1200 BAUD FSK MODEM



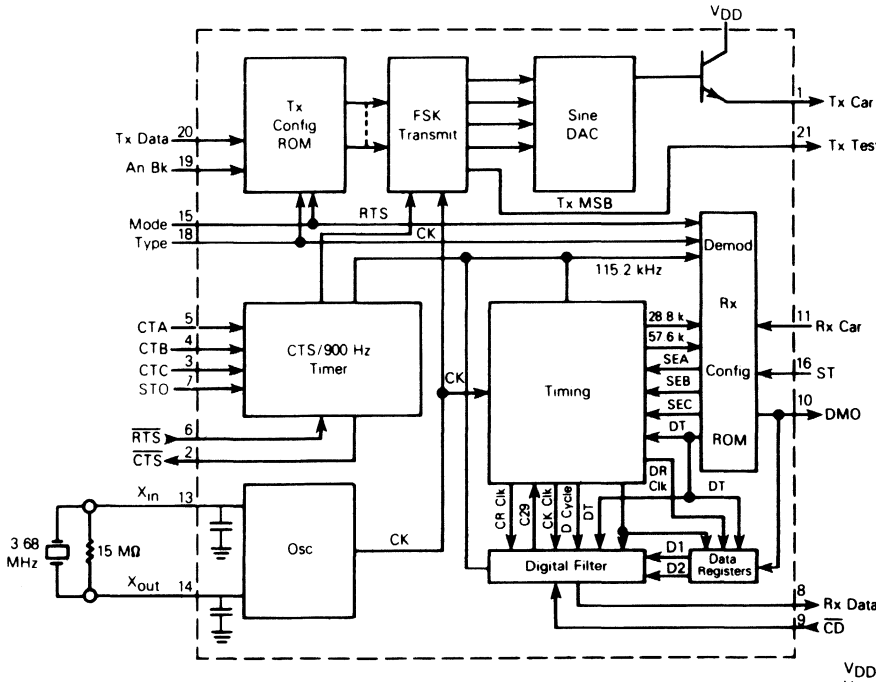
L SUFFIX
CERAMIC PACKAGE
CASE 736



P SUFFIX
PLASTIC PACKAGE
CASE 708

3

MC145450 1200 BAUD FSK MODEM
BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

ADI967R1

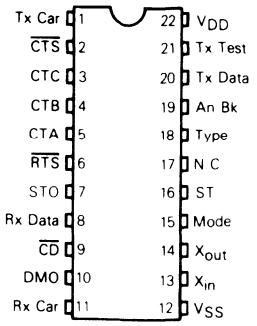
ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	10	V
Input Voltages, All Inputs	V_{in}	$V_{SS}-0.5$ to $V_{DD}+0.5$	V
DC Current Drain per Pin Pin 3-6, 9, 15, 16, 18, 19, 20 Pins 2, 8	I_{out}	 10 35	mA
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	$V_{DD}-V_{SS}$	4.5	5.0	6.5	V

PIN ASSIGNMENTS



3

DC ELECTRICAL CHARACTERISTICS ($V_{DD}=5.0$ V ±5%, $V_{SS}=0$, $T_A=0$ to 70°C)

Characteristics	Symbol	Min	Typ	Max	Unit
Input High Voltage	V_{IH}				V
Pins 3-7, 9, 15, 16, 18, 19, 20	–	2.8	–	–	
Pin 13, 11	–	4.0	–	–	
Input Low Voltage	V_{IL}				V
Pins 3-7, 9, 15, 16, 18, 19, 20		–	–	0.5	
Pin 13, 11		–	–	0.6	
Input Current	I_{in}				μA
All Inputs (V_{IL} 0 V)		–	–	−5.0	
All Inputs Except Pins 11, 13, ($V_{IH}>2.8$ V) (Note 1)		–	–	600	
Output High Current ($V_{OH}=2.4$ V)	I_{OH}				mA
Pins 2, 8 (Test Load A)		0.75	–	–	
Pins 10, 21 (Test Load B)		0.75	–	–	
Output Low Current ($V_{OL}=0.4$ V)	I_{OL}				mA
Pins 2, 8 (Test Load A)		1.2	–	–	
Pins 10, 21 (Test Load B)		0.6	–	–	
Operating Current	I_{DD}	–	2.5	6	mA
Input Capacitance	C_{in}				pF
All Except Pin 13		–	–	12	
Pin 13 (X_{in})		–	8	–	
Output Capacitance	C_{out}				pF
All Except Pin 14		–	–	12	
Pin 14 (X_{out})		–	13	–	
Transmit Audio Signal Level (Pin 1 $R_L=10$ kΩ (Note 2)	–	0.428	0.5	0.578	Vp-p
Total Harmonic Distortion (2nd to 14th) (Note 2)	THD	–	−50	−40	dB

AC ELECTRICAL CHARACTERISTICS ($V_{DD}=5.0$ V ±5%, $V_{SS}=0$, $T_A=0$ to 70°C)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Rise Time (Test Load A) (Pins 2, 8)	t_r	–	20	100	ns
Output Rise Time (Test Load B) (Pins 10, 14, 21)	t_r	–	20	100	ns
Output Fall Time (Test Load A) (Pins 2, 8)	t_f	–	20	100	ns
Output Fall Time (Test Load B) (Pins 10, 14, 21)	t_f	–	20	100	ns
Input Rise and Fall Times (Except Pin 13)	t_r, t_f	–	–	1000	μs
Delay From $\overline{RTS}$ to $\overline{CTS}$ STO = Low	$t_{d(low)}$	–	1	–	μs
Delay From $\overline{RTS}$ to $\overline{CTS}$ STO = High	$t_{d(high)}$	18.3	–	21.7	ms

NOTES:

1. Active pull-up devices are used on these inputs to allow interfacing to TTL devices. The I_{in} specified is a transitional load (not steady state) which is drawn when the input is brought up to 2.8 V until the internal pull-up device has raised the signal to the V_{DD} level.
2. Measured in any mode using HP-3555B dB meter (or equivalent) with 3 kHz flat filtering.

PIN DESCRIPTIONS

V_{DD}, POSITIVE POWER SUPPLY (PIN 22)
This is nominally 5.0 V.

V_{SS}, NEGATIVE POWER SUPPLY (PIN 12)
This is usually 0 volts.

Tx Car, TRANSMIT CARRIER (PIN 1)
The transmit carrier output is a 16 step digitally-synthesized sine wave with an amplitude of 0.1 V_{DD} (p-p) (± 10%) and offset by a dc bias of 0.5 V_{DD} (± 10%). The output load should be 10 kilohms or greater.

$\overline{CTS}$, CLEAR TO SEND (PIN 2)
The clear to send output goes low in response to a high-to-low translation of $\overline{RTS}$ following a selected delay (see CTA, CTB, CTC pin description). This output goes high immediately after loss of $\overline{RTS}$. During the time following activation of $\overline{RTS}$ and before the activation of $\overline{CTS}$, Tx Data should be held in the mark condition.

CTA, CLEAR TO SEND SELECT A (PIN 5)
CTB, CLEAR TO SEND SELECT B (PIN 4)
CTC, CLEAR TO SEND SELECT C (PIN 3)

For delay times for clear to send delay select inputs, see Table 1.

$\overline{RTS}$, REQUEST TO SEND (PIN 6)
The request to send input controls data transmission from the modulator. A low level enables the modulator output and a high level will disable the modulator. See Figure 1.

STO, SOFT TURN OFF INPUT (PIN 7)
Activation of STO causes a 900 Hz tone to be transmitted and $\overline{CTS}$ to remain active for 20 ms following the loss of $\overline{RTS}$. See Figure 5.

Rx Data, RECEIVE DATA (PIN 8)
The receive data output is the serial data output from the demodulator. Rx Data is clamped high when $\overline{CD}$ is not active.

$\overline{CD}$, CARRIER DETECT (PIN 9)
When carrier detect input is high (1), the Rx Data output will be clamped to a high state. When carrier detect is low (0), Rx Data output demodulates the Rx carrier input signal.

DMO, DEMODULATOR OUTPUT (PIN 10)
The demodulator output is the output of the differential delay detector. It is used for production testing of the demodulator. In normal operation, this pin should be left open.

Rx Car, RECEIVER CARRIER (PIN 11)
The receiver carrier input is the FSK input to the demodulator. This signal should be the hard-limited output of the receive filter, nominally 50%.

X_{in}, OSCILLATOR INPUT (PIN 13)
X_{out}, OSCILLATOR OUTPUT (PIN 14)
X_{in} should be driven from either an AT-cut crystal or a digital signal source at 3.6864 MHz ±0.01%. When driven by a crystal, a 15 megohm resistor should be connected from X_{in} to X_{out} in parallel with the crystal.

MODE (PIN 15)
The mode pin selects the pair of frequencies used during modulation and demodulation. A "0" on this pin selects forward channel operation, i.e. high-speed transmit and low-speed receive. A "1" on this pin selects reverse channel operation, i.e. low-speed transmit and high-speed receive.

ST, SELF TEST (PIN 16)
When a high level is placed on this pin, the demodulator is switched to the modulator frequencies and baud rate (as determined by Mode and Type pins). The modulator should be looped back through the receive filter to the demodulator for self test (echo back).

N.C. NO CONNECTION (PIN 17)
This pin is not bonded internally and should be left open in normal operation.

TYPE (PIN 18)
This pin is used to select Bell 202 type operation and CCITT V.23 operation. When the type input pin is a "1", Bell operation is selected. When the type input pin is a "0", the CCITT standard is selected.

An Bk, ANSWER BACK (PIN 19)
The answer back input causes the answer back tone to be transmitted. The answer back tone is 2025 Hz for the Bell mode and 2100 Hz for the CCITT modes. When a high level is placed on the An Bk input pin, the Tx Car pin will output an answer back tone and $\overline{CTS}$ will go to a high state, regardless of the state of $\overline{RTS}$ (see Figure 1).

Tx Data, TRANSMIT DATA (PIN 20)
The transmit data input is the serial input to the modulator. A high level causes a mark frequency to be transmitted, a low level causes a space frequency to be transmitted.

Tx Test, TRANSMIT TEST (PIN 21)
The transmit test output is a square wave representation of the modulator transmit frequency. It is used for test purposes and should be left open in normal operation.

FIGURE 1 – An Bk AND $\overline{RTS}$-$\overline{CTS}$ TIMING

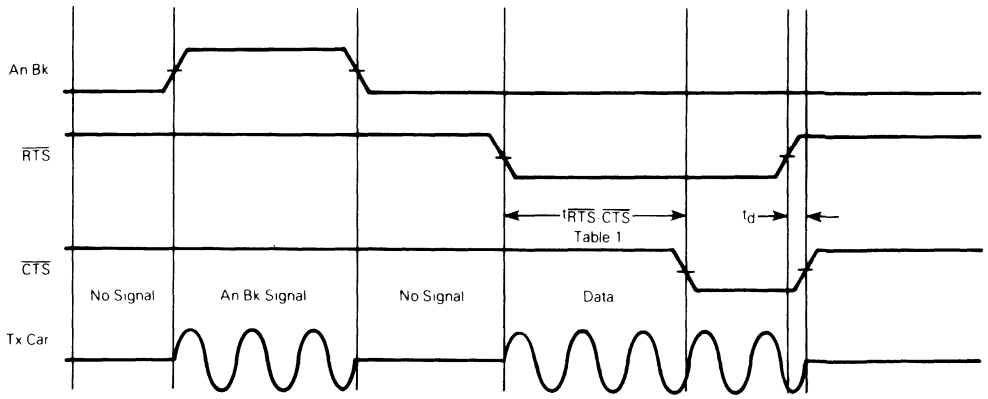


TABLE 1 – $\overline{RTS}$-$\overline{CTS}$ DELAY TIMES

CTC	CTB	CTA	Delay*
0	0	0	0 ms
0	0	1	26.7 ms
0	1	0	40.0 ms
0	1	1	60.0 ms
1	0	0	133.3 ms
1	0	1	213.3 ms
1	1	0	266.7 ms
1	1	1	426.6 ms

*All delays are ± 1.7 ms.

TABLE 2 – OPERATING MODES

Type	Mode	Transmit Data	Transmit Frequency Spec	Transmit Frequency Actual	Answer Back Tone	Application
0	0	0	2100	2099.32	2100	CCITT V.23 75 Baud Receive 1200 Baud Transmit
		1	1300	1299.86		Forward Channel
0	1	0	450	450	2100	CCITT V.23 1200 Baud Receive 75 Baud Transmit
		1	390	390.5		Reverse Channel
1	0	0	2200	2199.52	2025	U.S. 150 Baud Receive 1200 Baud Transmit (Bell 202)
		1	1200	1200		Forward Channel
1	1	0	510	509.73	390	U.S. 1200 Baud Receive (Bell 202) 150 Baud Transmit
		1	390	390.5		Reverse Channel

Data = 0 = Space
= 1 = Mark

* Crystal Frequency = 3.6864 MHz

FIGURE 2 – STO TIMING

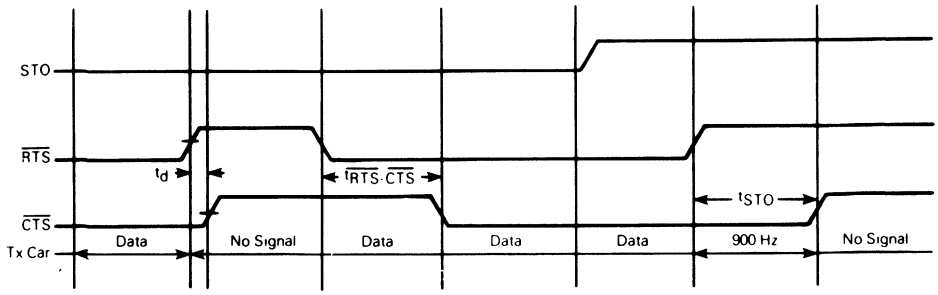
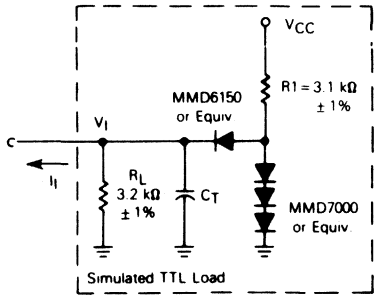
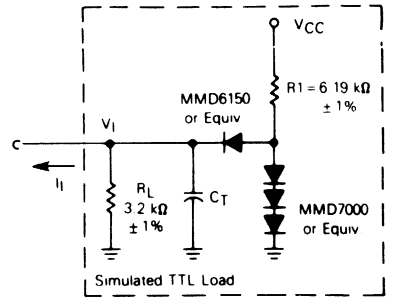


FIGURE 3 – OUTPUT TEST LOAD A



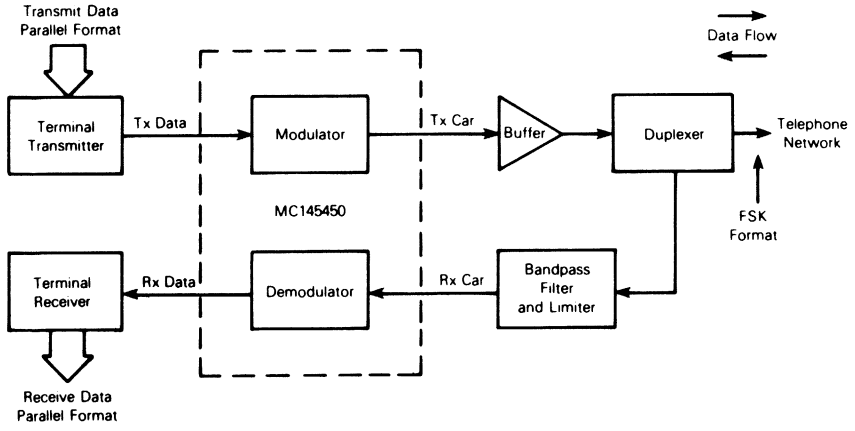
C_T = 20 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

FIGURE 4 – OUTPUT TEST LOAD B



C_T = 20 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

FIGURE 5 – TYPICAL MEDIUM-SPEED MODEM APPLICATION



3

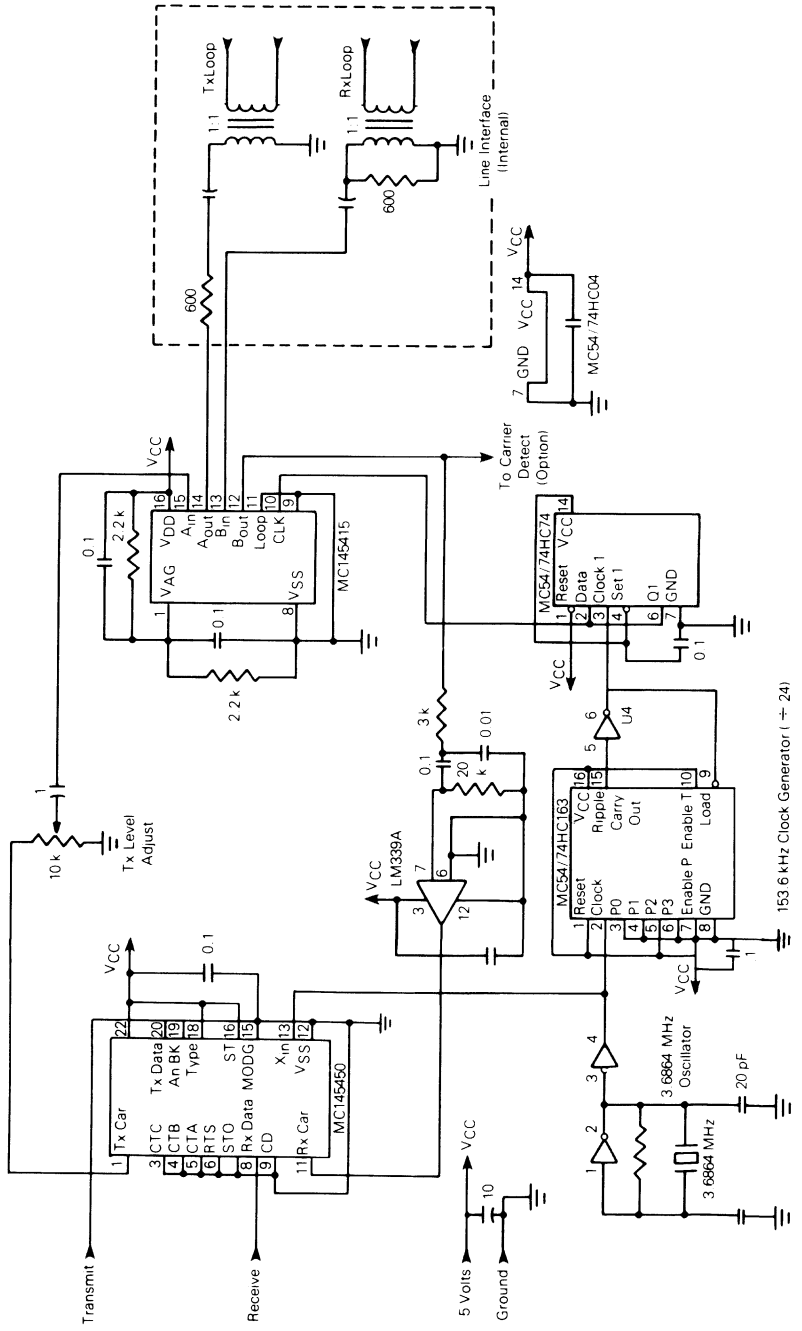


FIGURE 6 – TYPICAL 1200 BAUD 4 WIRE MODEM APPLICATION

MOTOROLA

MC145472

Product Preview

ISDN U REFERENCE POINT TRANSCEIVER

The MC145472 is a transceiver which provides an interface between the Interchip Digital Link (IDL) and a twisted wire pair. Two 64 kbps data channels (B) and one 16 kbps signalling channel (D) are provided to the MC145472 by the IDL bus. The MC145472 reformats the channels and transmits the data on a twisted wire pair in accordance with the American National Standard. The receiver portion of the MC145472 separates the channels and provides them to the IDL bus. This transaction occurs in both directions simultaneously, i.e. full duplex. A Serial Control Port is provided to efficiently control the MC145472. This is a common feature of the Motorola family of ISDN devices.

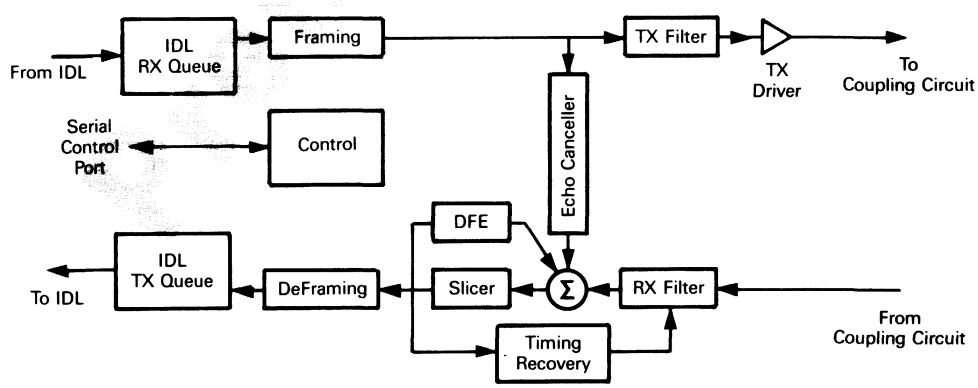
- A single chip 2B1Q, Echo Cancelling, Adaptivly Equalized Transceiver
- Conforms to the American National Draft Standard for ISDN Basic Access Interface for Application at the Network side of the NT, Layer 1 Specification.
- Customer data (2B+D) provided to/from the Industrial standard Interchip Digital Link (IDL)
- Control, Status, and Extended Maintenance functions provided via the Serial Control Port
- On Chip conformance with Activation/Deactivation as specified in the American National Draft Standard.
- Low power consumption when in the deactivated state
- Basic Maintenance functions provided on chip
- Extended maintenance functions provided via the Serial Control Port
- Pin selectable NT/LT mode of operation
- On chip transmit driver
- Low Power CMOS

ISDN U REFERENCE POINT TRANSCEIVER

TBA

3

BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MOTOROLA

MC145474

Product Preview

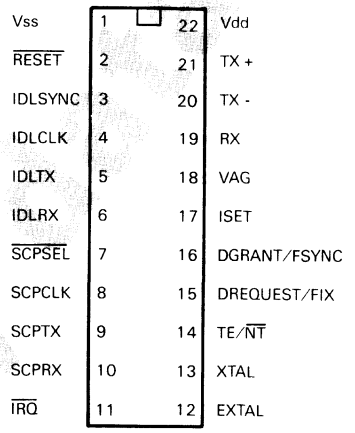
ISDN S/T INTERFACE TRANSCEIVER

The MC145474 ISDN S/T transceiver provides an economic VLSI layer one interface for use in network termination and terminal equipment applications. The MC145474 conforms to the CCITT I.430 recommendations and provides the modulation/line drive, demodulation/line receive functions required of the interface. In addition the MC145474 provides the activation/deactivation, error monitoring, framing, bit and octet timing. The MC145474 also provides the control signals for the interface to layer two devices, multiframing capability and maintenance signaling channels. The MC145474 features the IDL digital interface for the exchange of B and D channel information between ISDN components and systems. The MC145474 provides an industry standard serial control port to program the operation of the transceiver.

FEATURES

- Conforms to CCITT I.430 Recommendations
- Features the Interchip Digital Link (IDL)
- Pin Selectable Terminal or Network Operating Modes
- Industry Standard Microprocessor Serial Control Port
- Supports 1:1 Transformers for Transmit and Receive
- Extended Range Operation
- Supports Multiframing S & Q Channels
- Optional B Channel Idle, Exchange, or Invert
- Supports full range of Loopbacks
- Low Power CMOS Operation
- Supports Low Power Wake-Up Mode
- Supports Crystal or Clock Input

PIN ASSIGNMENTS



OVERVIEW

TRANSCEIVER MODES OF OPERATION

The MC145474 ISDN S/T transceivers operate in one of two pin selectable modes of operation, the network terminating (NT) mode, and the terminal (TE) mode of operation. The transceivers operate on a four wire circuit with one pair of wires dedicated to each direction of transmission. The line rate of transmission is 192k bit/s (192k symbol/s). The data bits are encoded in the one bit per baud, 100% pulse width, Alternate Mark Inversion (AMI)* format. The 192k bit/s data streams carry two B channels of data at 64k bit/s each, and one D channel for signaling and data, at 16k bit/s. The additional bits in the 192k bit/s stream of information are used to maintain proper operation of the data link at the physical level. The range of the MC145474 (S/T) Transceiver is 2 Km over 26 AWG cable (approximately 24 dB of insertion loss).

The transceivers are capable of point to point, as well as point to multipoint operation. Point to point operation implies that only one transmitter and one receiver are active at any one time in each direction of transmission. Point to multipoint operation implies that more than one TE, may be active simultaneously. The basic wiring configuration for both modes of operation is illustrated in Fig. 2/I.430. The wiring of the transmit sections of each TE device must be matched in polarity in the multipoint configuration.

In addition to the modulation/line drive, and demodulation/line receive functions involved with the data transmission, the MC145474 S/T transceiver provides the activation/deactivation, error monitoring, framing, bit and octet timing required of the interface. The S/T transceiver also features: Link Access Protocol D channel (LAPD) interface controls, multiframing, and maintenance signaling channels. A serial control port is provided to gain access to the control registers within the S/T transceiver, which govern the overall operation of the device. Figs. #2 and #3 provide functional block diagrams of the MC145474 S/T transceiver in the NT and TE modes of operation.

INTERCHIP DIGITAL LINK

The MC145474 S/T transceiver will feature the Interchip Digital Link (IDL) for the exchange of digital information between ISDN components and systems. The IDL interface will be featured on all Motorola components in the ISDN family of components in order to insure system compatibility in differing applications and partitionings of the ISDN network components. The IDL interface itself operates in one of two modes (master and slave). In the slave mode the IDL interface receives data clock, and frame synchronization information (typically from the network). In the master mode the IDL interface supplies the data clock, and frame synchronization. In both modes there are separate I/O lines for transmit and receive data. In total, each IDL port is a four wire interface consisting of a frame sync signal which is periodic at an 8 kHz rate, a continuous data clock signal, a transmit data output, and a receive data input.

*Zeros cause the line to Mark

D CHANNEL CONTROL

The TE mode S/T transceivers provide two control lines for the control of the D channel. These lines are used to indicate the beginning and ending of layer 2 frames, D channel collisions, and when the D channel may be used by layer 2 devices. The priority CLASS is selected by a control bit within the serial control port (SCP).

LOOPBACKS

Each transceiver has the capability of looping data back to the source that originated the data. These loopbacks also exercise a substantial portion of each transceiver's internal functional blocks. The combination of loopbacks provides the capability of testing the transmission loop or the data path prior to the loop. Typical loopback configurations allow data received by the demodulator circuit to be buffered and modulated back to the source of that data. Data received via the IDL interface also has the capability of being buffered and then returned to the output side of the IDL interface. Each loopback function may operate in a transparent, or non-transparent manner.

MULTIFRAMING, S and Q CHANNELS

The MC145474 S/T transceivers provide means for the establishment of a multiframe between the NT and TE transceivers. The multiframe format establishes an S channel from the NT to the TE and a Q channel from the TE to the NT. The S and Q channels may be used to establish a layer 1 signaling capability for maintenance of the S/T loop.

SERIAL CONTROL PORT

The MC145474 S/T transceivers provide a four wire serial port to program the operation of the transceiver, receive status, and data from the transceivers. The operation of the S/T transceiver is controlled by setting and clearing the bits of the control registers within the S/T transceiver. The serial control port is directly compatible with the Motorola Serial Peripheral Interface (SPI) and the NSC MicroWire Plus (TM) industry standard microprocessor serial interfaces. The Serial Control Port (SCP) gives the MC145474 S/T transceiver an architecture which is economic for LT, NT, TE and TA applications.

FIGURE 2 - TE MODE FUNCTIONAL BLOCK DIAGRAM

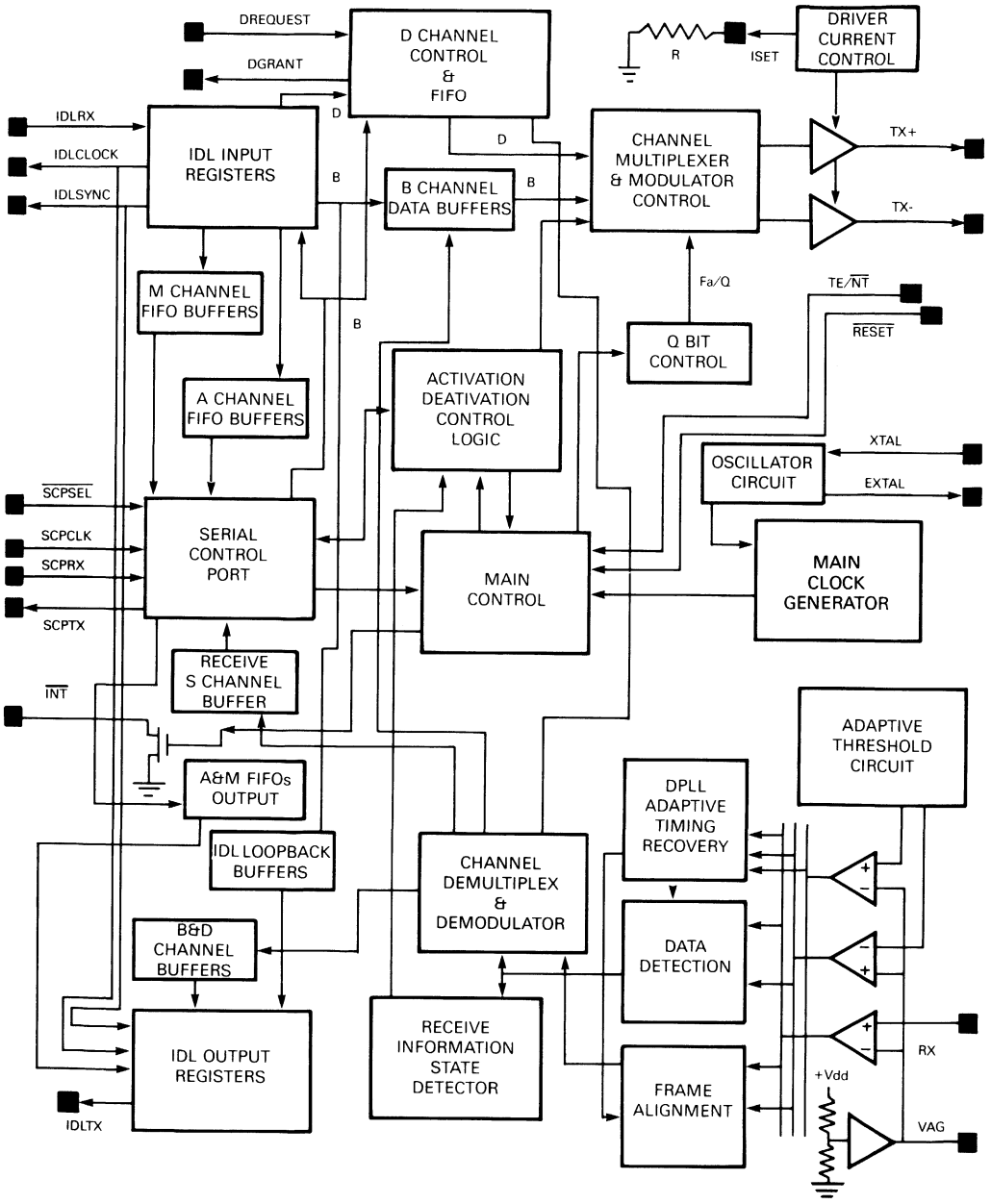
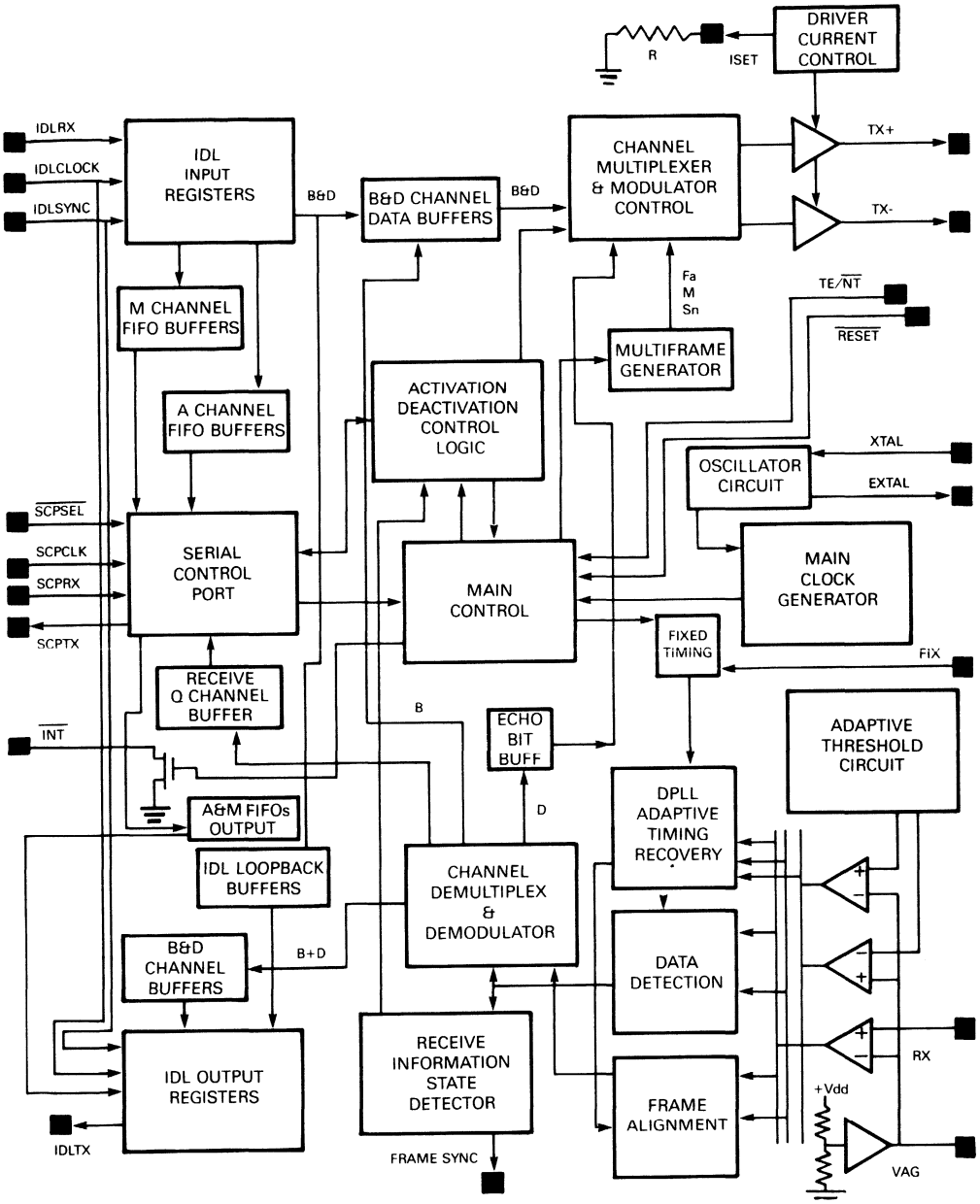


FIGURE 3 - NT MODE FUNCTIONAL BLOCK DIAGRAM



MOTOROLA

MC145488

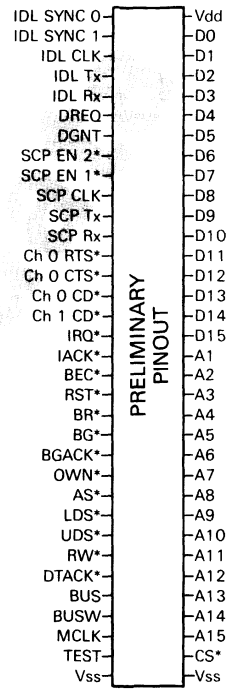
Product Preview

DUAL DATA LINK CONTROLLER (DDLC)

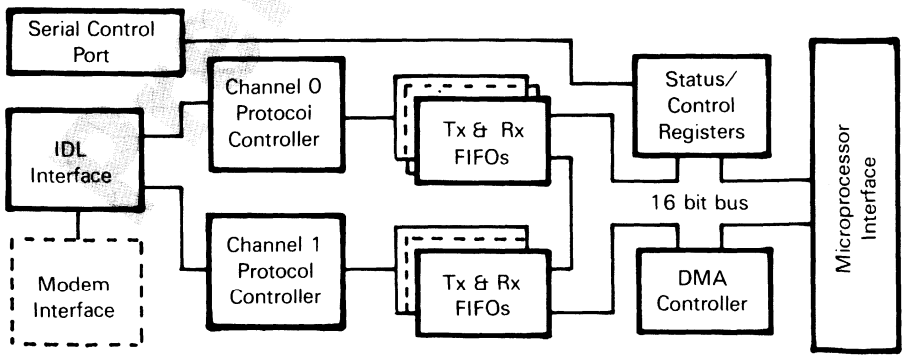
The MC145488 is a two-channel ISDN LAP-D controller with on-chip DMA controllers. It is intended for ISDN terminal and switch applications where one or two channels of data will use HDLC type protocols. The DDLC is ideally suited for use with the MC145474 S/T Transceiver. The Inter-chip Digital Interface easily connects the chips together providing a powerful Layer One/Layer Two ISDN solution. A Serial Control Port is provided to efficiently control the MC145474 or other ISDN family devices. The DDLC is compatible with the 68000 asynchronous bus and other popular bus structures.

- Two Independent Full-Duplex Bit-Oriented Protocol Controllers
- Four DMA Channels
  - 64k byte Address Range with Expansion Control
- Two Buffer Descriptors for Receiver Channel 0
- 68000 Bus Compatible
  - 16 or 8-Bit Data Bus
- Bit-Level HDLC Processing including:
  - Flag Generation/Detection
  - Abort Generation/Detection
  - Zero Insertion/Deletion
  - CRC-CCITT Generation/Checking
  - Residue Bit Handler
- Frame Address Comparison
- Interrupt Vector Generator
- IDL Interface to MC145474 ISDN S/T Transceiver
- Serial Control Port for ISDN Family Device Control
- Flexible Serial Interface with Modem Control Signals
- Compatible with V.110 and I.460
- Compatible with DMI Specification 3.1
- Low Power CMOS with Automatic Power-Down

PIN ASSIGNMENT



BLOCK DIAGRAM



SECTION 1
OVERVIEW

1.1 DDLC OVERVIEW

The MC145488 Dual Data Link Controller (DDLC) is a high-performance CMOS two-channel protocol controller with on-chip DMA. Each channel has a full-duplex transceiver with independent protocol controllers to handle the bit-level tasks of HDLC-type bit-oriented protocols including LAP-B and LAP-D. Each channel has dedicated DMA controllers for transmit and receive. A transparent mode is provided which bypasses the protocol circuitry so that data may be directly DMAed between the host processor's memory and the serial interface. The microprocessor interface is configurable to 68000-based structures or other popular buses.

The serial data interface has two modes: IDL/SCP and modem. In the IDL/SCP mode for ISDN applications, the IDL bus is supported with access control lines to the D-channel included. Two communication channels can be active; both B-channels or the D-channel and either B-channel. A Serial Control Port (SCP) is provided so systems may be constructed using a serial control mechanism to simplify wiring. In the modem mode each transceiver channel has its own separate transmit and receive clock inputs along with modem control lines (RTS, CTS and CD).

The DDLC has an automatic power-down feature that reduces power consumption when the chip is idle. When both transceiver channels are idle and the CS* or IACK* pins are inactive, the DDLC enters the low power state. When the CS* or IACK* pins are activated for a register read/write or vector acquisition, the chip enters the normal power state for the duration of the access and for any time required for internal processing.

Two internal loopback functions and a test mode are available. The loopbacks are controlled by the host for on-line maintenance. The test mode is pin activated and provides access to the internal state machines.

1.2 HDLC OVERVIEW

HDLC (High-Level Data Link Control) and its descendents, LAP-B (Link Access Protocol-Balanced) and LAP-D (Link Access Protocol for the D-channel), are bit-oriented synchronous protocols which are finding increased usage in data communication systems. LAP-B and LAP-D share the basic format of HDLC but differ in certain aspects of the software implementations.

TheDDLC in the HDLC mode transmits and receives data in a format called a frame. All frames start with an opening flag and end with a closing flag. Between the flags, a frame contains an address field, control field, information field and a Cyclic Redundancy Check field (CRC).

Flag - The flag is the unique binary pattern (01111110). It provides the frame boundary and a reference for the position of each field of the frame. The DDLC transmitter generates a flag pattern internally and the opening flag and closing flags are appended to a frame automatically. Two successive frames can share one flag for a closing flag of the first frame and for the opening flag of the next frame. The receiver searches for a flag on a bit-by-bit basis and recognizes a flag at any time. The receiver establishes the frame synchronization with every flag. The flags mark the frame boundary and reference for each field but they are not transferred to the receive FIFOs.

Address Field - The 8 or 16 bits following the opening flag comprise the address field. The address field is used to distinguish between the various devices in a network. Devices receiving frames not addressed to them may discard and ignore the frames. The DDLC has address recognition circuitry included which relieves the host from this task.

Control Field - The 8 or 16 bits following the address field are the control field. Commands and responses between the devices in a network are exchanged in this field.

Information Field - This field follows the control field and precedes the CRC field. The information field contains the "data" to be transferred but is not always necessarily contained in every frame. The information field is not necessarily an integral number of octets in length. The DDLC receives non-octet frames as octets and LSB-justifies the extra "orphan" bits at the end of the field. The number of orphan bits is indicated in a residue register.

Cyclic Redundancy Check Field - The 16 bits preceding the closing flag are the CRC field. The polynomial $x^{16} + x^{12} + x^5 + 1$ is used both for the transmitter and receiver. Both the transmitter and receiver polynomial registers are initialized to all 'ones' prior to calculation of the CRC. The transmitter calculates the CRC on all bits of the frame except for the flags and transmits the complement of the resulting remainder as the CRC field. The receiver performs the similar computation on all bits except for the flags and compares the result to FOB8 (hex). When the result matches FOB8, the frame is accepted and the buffer is closed. CRC generation and checking are automatically performed by the DDLC. The CRC field is not transferred to the buffer in memory. If desired, frames with CRC errors can be discarded automatically. All CRC errors are logged in a counter.

FIGURE 1.1 HDLC FRAME FORMAT

8 bits	8 or 16 bits	8 or 16 bits	n octets	16 bits	8 bits
FLAG	ADDRESS	CONTROL	INFORMATION	CRC	FLAG

Zero Insertion and Deletion - Zero insertion and deletion which allow the content of the frame to be transparent is automatically performed by the DDLC. A binary 'zero' is inserted by the transmitter after any succession of five 'ones' within a frame (between flags). The receiver deletes a binary 'zero' that follows successive five consecutive 'ones' within a frame.

Abort - The function of prematurely terminating a data link is called an 'abort'. The transmitter aborts a frame by sending eight consecutive 'ones' when a system fault such as a FIFO underrun is detected. The reception of at least seven consecutive 'ones' is interpreted as an abort by the receiver. The receiver responds to an abort by clearing the FIFO, clearing the buffer in memory. It then begins searching for a new frame.

Idle and Interframe Time Fill - When the transmitter is in an 'out of frame' condition (the transmitter is not transmitting a frame), it is in an idle state. Either a series of continuous flags (time fill) or a mark idle (consecutive 'ones' on a bit-by-bit basis) may be selected. When a receiver receives 15 or more consecutive 'ones', an interrupt is queued indicating the status to the host.

SECTION 2
BLOCK DIAGRAM DESCRIPTION

3

This section will describe the internal blocks of the DDLC. The blocks include a serial interface with two modes of operation, two protocol controllers which handle the bit-level aspects of HDLC-like protocols and four FIFOs which buffer the data. A four-channel DMA controller and a microprocessor interface block connecting the DDLC to the host system along with a Serial Control Port which provides serial communication to devices in ISDN applications are also included. The following paragraphs will describe the operation of the internal blocks.

2.1 SERIAL INTERFACE

The DDLC serial interface has two modes of operation: the IDL/SCP mode and the modem mode. This section will describe the operation of these modes.

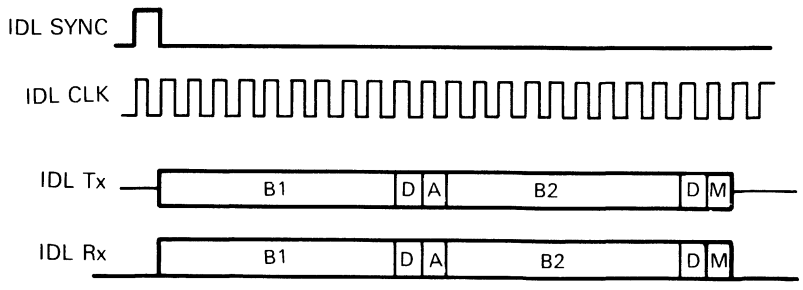
2.1.1 Interchip Digital Link (IDL) Interface

The IDL Interface is a full-duplex four wire serial interface used to interconnect various devices on an ISDN board level system. The IDL is used to distribute the several channels of information on the ISDN Basic Access Interface (S/T bus) that has been processed by the MC145474 S/T Transceiver to the various devices on a board level ISDN product. Data on five independent channels is transferred in 20-bit frames every 125 µs providing 160k bps bandwith. Two 64k bps B-channels and one 16k bps D-channel along with two 8k bps auxiliary channels are passed on the IDL Interface. The DDLC is an IDL slave which is clocked by the bus master. The following diagram indicates the relationship of the four IDL signals.

IDL CLK is an input which receives a continuous signal at 2.56 MHz from the IDL bus master. For ISDN terminal applications, the MC145474 S/T Transceiver is the IDL bus master which provides this clock. In other systems, frequencies such as 1.536 MHz or 2.048 MHz are useable. IDL Tx is an output which is active only on assigned bits in the frames. For all other bit times, it is high-impedance. IDL Rx is an input which accepts bits only on assigned timeslots. IDL SYNC is an input which accepts a positive pulse one clock period wide. This signal indicates that the 20 clock periods following the pulse contain the IDL frame. This pulse occurs every 125 µs so that 8000 frames per second are exchanged between the bus master and the slaves. The DDLC has two IDL SYNC pins (IDL SYNC 0 and IDL SYNC 1), one for each channel, so that the two channels are not restricted to operating on the same IDL frame. For terminal applications where there is only one IDL bus master, both SYNC pins will be connected together. IDL SYNC 0 is used for Channel 0 and IDL SYNC 1 is used for channel 1.

The 20-bit frames are broken into five bit-fields. The first eight bits contain data on the 64k bps B1-channel. The 9th bit contains one bit of the D-channel. The 10th bit is an auxiliary bit which is not used by the DDLC. Bits 11 - 18 contain the 64k bps B2-channel. The 19th bit is the second bit of the D-channel and the 20th bit is another auxiliary bit which is not used by the DDLC. When the DDLC operates on the D-channel, it uses bit 9 and bit 19 of the IDL frame. The two bits cannot be separated. The D-channel is a 16k bps channel which is used for communication between an ISDN terminal and the network. Channel 1 of the DDLC is primarily intended for use with the IDL D-channel and directly supports

FIGURE 2.1.1.1 - IDL BUS SIGNALS



the D-channel contention algorithm of the MC145474 S/T Transceiver. The DDLC has the capability of handling data on either B-channel and the D-channel or on both of the B-channels simultaneously.

When the DDLC is operating on the D-channel with the companion MC145474 S/T Transceiver, Channel 1 with the DREQ and DGNT lines must be used to comply with the D-channel contention algorithm. When the DDLC has a data frame to transmit, it asserts DREQ (DREQ high). The S/T transceiver monitors the S/T Interface for activity on the D-channel and indicates when the channel is free by asserting DGNT (DGNT high). When DREQ is high, the DDLC samples the DGNT pin on the falling edge of IDL CLK while IDL SYNC 1 is high. Transmission from the DDLC begins in the IDL D-bit time slots when the DREQ and DGNT are both active. If a D-channel collision is detected on the S/T Interface by the S/T transceiver, DGNT is negated (DGNT low). When a collision is detected, the colliding device is expected to immediately stop transmitting and re-transmit the frame at a later time when the D-channel is again free. If a collision is detected, the DDLC automatically aborts the frame in progress and prepares to retransmit the entire frame when the D-channel is again free. This is done without interrupting the host.

Normally, all eight bits of an ISDN B-channel are grouped into one 64k bps bearer channel. However, a B-channel may be thought of as composed of eight 8k bps channels. CCITT specification I.460 outlines a technique where the individual bits in a B-channel are accessed and treated as individual channels. The DDLC has the capability of meeting the requirements of I.460 as it can access the individual bits in the B-channels for multiplexer or other non-ISDN applications. A bit mask register is provided for Channel 0 and Channel 1 to select the individual bits in the 8-bit field that are active. The B-channel Bit Mask Registers are programmed with 'ones' in the positions where the bits are active and 'zeros' where the bits are ignored. Note that the least significant bit is transmitted first. For example: if bits 2 and 3 are to be used in a particular application, the coding in the Bit Mask Register would be 0000 1100. The receiver will ignore all bits in bit positions other than b2 and b3. The transmitter will transmit only on these two bit positions. On all other positions it will be high-impedance. The Bit Mask feature is only useable on the B-channels when the IDL interface is used. In the D-channel or modem mode, the Bit Mask registers are disabled.

2.1.2 Serial Control Port (SCP)

The DDLC has a Serial Control Port which is used to program external devices through a serial mechanism. The SCP is a four wire full-duplex communication system which exchanges 8-bit bursts of data with SCP slave devices. The DDLC is an SCP master which generates the Enable and Clock signals. The following paragraphs describe the operation of the SCP.

SCP EN 1 and SCP EN 2 are outputs which enable SCP slave devices. When low, the Enable signals indicate that the slaves are selected and should expect a data burst. SCP CLK is an output which provides the shift clock for the data. The clock is normally low until a burst of data is transmitted. Then the clock is active for eight pulses. SCP Rx is the input which accepts data from the slave devices. This pin is sampled on the falling edges of SCP CLK. SCP Tx is an output which provides data to the slave devices. New data bits are presented on the rising edges of SCP CLK.

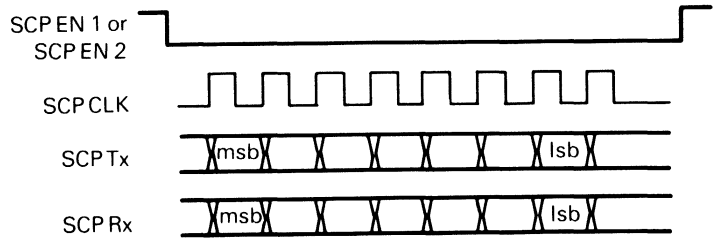
When a message is to be sent to a slave device, the information is placed in the SCP Tx/Rx Register bits b0 – b7. Then Enable 1 or Enable 2 (bits b8 or b9) in the SCP Status/Control Register are set to a logic one depending on the application. This activates the selected Enable pin to a logic low. The host then activates the Transmit bit (bit b10) and the SCP controller generates eight clock pulses on the SCP CLK pin and shifts the data on the eight rising edges. Data is shifted most significant bit first. The slave transmitter, at the same time, shifts its data (if any is ready) to the DDLC SCP Rx pin on the rising SCP CLK edges. The DDLC samples the SCP Rx pin on the falling SCP CLK edges and replaces the transmitted data with the received data in the Tx/Rx Register on a bit by bit. After the eight shifts have occurred, the Transmit bit (bit b10) in the SCP Status/Control Register is cleared indicating that the exchange was completed. An interrupt is also queued at that time. The host then resets the Enable 1 or Enable 2 (bit b8 or b9) which causes the Enable pin to return to a logic high.

The user can select an appropriate baud rate for the application. Bits b12 and b13 in the SCP Status/Control Register select a tap on a divider chain. The SCP CLK signal is derived from the MCLK through this chain.

2.1.3 Modem Interface

If the SCP and IDL interfaces are not needed for a particular application, an alternate serial interface is provided in the DDLC. When the Modem Enable Bit in the

FIGURE 2.1.2.1 - SCP PIN FUNCTIONS



Master Status/Control Register is set to a logic one, the IDL and SCP interfaces are disabled and a modem interface is substituted. This section will describe the operation of the modem mode. In this discussion references will be made to pin names which are generic names associated with the seven modem pins on each channel. The actual pin names indicate the channel with which they are associated: e.g. Ch 0 TxD.

A general purpose serial interface is provided in the DDLC where the two independent full-duplex data channels may be controlled. Each channel has seven pins associated with it. There are transmit and receive clock inputs (Tx CLK and Rx CLK), transmit and receive data pins (TxD and RxD) and modem control lines (RTS*, CTS* and CD*). The transmit and receive clocks are all independent of each other and may be asynchronous to the microprocessor system clock (MCLK). These clocks may have a frequency of up to 2.56 MHz, but it must be noted that the data throughput of the DDLC is limited by the microprocessor bus bandwidth available to the DDLC.

Data bits from the TxD pins are presented on the falling edges of the associated TxCLK. Data bits on the RxD pins are sampled on the rising edges of the associated RxCLK. The modem control lines are used to control the flow of data. Request-to-Send (RTS*) is an active low output which indicates that the DDLC has data to transmit. Clear-to-Send (CTS*) is an input which indicates that the DDLC has permission to transmit. Bit b8 in the associated Transmit Status/Control Register indicates the current state of this pin. In the HDLC mode, if CTS* goes inactive (high) while a frame is being transmitted, the DDLC immediately aborts the frame and prepares to retransmit the aborted frame when CTS* again goes active. In the transparent mode when CTS* goes inactive, the DDLC simply stops transmitting and resumes where it left off when CTS* is again active. Carrier Detect (CD*) is an input which indicates that the data on the RXD pin is valid. Bit b0 of the associated Receive Status Register indicates the current state of this pin. An interrupt is queued when this pin changes state.

Note: DGNT and CTS* are dual function pins associated with Channel 1. When the D-channel mode is selected, the pin becomes DGNT which is an active high signal. In the non D-channel mode or the modem mode, the pin becomes CTS*, an active low signal. In either case, the internal bit in the Channel 1 Transmit Status/Control Register indicates that the pin is active with a logic one.

2.2 PROTOCOL CONTROLLERS

Two identical bit-level protocol controllers are provided which perform HDLC framing and deframing. Additionally, the receivers have the capability of address screening along with detection and logging of CRC errors. This section will describe these blocks.

2.2.1 Transmitters

Each channel's transmitter is designed to need as little intervention from the host processor as possible. To transmit a frame of data, the host merely informs the DDLC of the starting address of the data frame in memory and the length of the frame in bytes. The DDLC then transmits an opening flag and the data from memory. When the transmitter detects that the end of the frame has been reached, a CRC field and a closing flag are appended. Zeros are automatically inserted in the data to prevent it from imitating a flag or abort character. The transmitter will generate an abort character if the FIFO underruns. The transmitters remain in the idle state when Transmit Enable (bit b0 of the Transmit Status/Control Register) is at logic zero. While in this state, ones are transmitted in selected bit periods. During interframe periods, the DDLC has the capability of transmitting continuous flags (7E hex) or continuous marks (FF hex) as selected by bit b2 of the Transmit Status/Control Register. For network-level fault isolation, the transmitters have the capability of generating faulty CRCs (bit b3 of the Transmit Status/Control Register). The transmitters also continuously monitor the DGNT or CTS* pins and indicate the current state of the pins with Transmit Status/Control Register bit b8.

The transmitters have two methods of indicating to the transceiver or modem that they have data ready to transmit. In the normal mode, Request-to-Send is active (RTS* low) as long as the Transmit Enable bit is set. During interframe periods, either flags or marks are transmitted. Transmission actually begins when Clear-to-Send (CTS* low) is active. If CTS* goes inactive while a frame is in transmission, the frame is aborted and the DMA pointers are reset so that the frame can be retransmitted without interrupting the host. For ISDN D-channel applications, Channel 1 of the DDLC requests the D-channel from the MC145474 S/T Transceiver by activating D-channel Request (DREQ pin high) and begins transmitting when the S/T Transceiver indicates that the D-channel is clear by activating D-channel Grant (DGNT high). DREQ remains active until the closing flag has been transmitted. If the S/T transceiver detects a collision on the D-channel, it aborts the colliding frame and indicates to the DDLC that the frame was aborted by negating DGNT (low). The DDLC stops transmitting, resets the DMA pointers and retransmits the data frame when DGNT goes active (high) indicating that the D-channel is again clear.

There are several sources of interrupts in the transmitters. The Transmit Frame Complete Interrupt indicates that the closing flag of a frame has been transmitted. The DMA Complete Interrupt indicates that the DMA controller has transferred the last byte of data to the FIFO. If the FIFO underruns, the FIFO Underrun interrupt will be queued. If, while a DMA transfer is in progress, a bus error or address error is detected, the Bus Error or Address Error Interrupt will be queued.

The transmitters have a transparent mode where the HDLC formatters are disabled and data is directly transmitted from memory. In this mode, transmission continues as long as CTS* is active (low). If CTS* goes inactive, transmission stops and resumes where it left off as soon as CTS* again goes active.

2.2.2 Receivers

The receivers provide the complementary functions to those provided by the transmitters. The receiver is reset and idle until the Receive Enable bit is set. In the HDLC mode, the receiver begins searching for a flag character. When it is found, the selected address field of the frame is checked against two user programmable addresses and a hardwired address (FF hex). Either the first or second octet following the opening flag may be checked for an address match as selected by the LAP-B/LAP-D Mode Select bit (b5) in the Receive Control Register. If a match is found, the DDLC passes the frame of data to the allocated buffer in memory. If no address match is found

the DDLC resets the DMA pointers and searches for a new frame. If address comparison is not desired, it may be disabled and all data frames may be passed to memory. Zeros inserted by the transmitter are removed from the data before placing the bytes in memory.

At the end of the frame, the CRC field is checked and if found to be correct, the DDLC queues an interrupt indicating that a good data frame has been received and is in memory. If the CRC is found to be in error, the DDLC resets the buffer pointers to the start of the buffer and searches for a new frame. This in essence clears the buffer and discards the frame in error. In certain instances, frames with CRC errors will be of interest. A control bit is provided so that frames with CRC errors can be passed to memory. A CRC error flag in the Receive Status/Control Register indicates that the frame is in error. All CRC errors are logged in the CRC Error Registers.

The receivers have the capability of detecting and reacting to aborted frames. If an abort is detected (7 to 15 consecutive ones with no inserted zeros), the DMA controller suspends activity on that channel and resets the buffer descriptor pointers so that the buffer may be reused on the next frame. The FIFO is cleared and the receiver searches for another frame's opening flag.

The receivers have the capability of operating in non-octet aligned systems. The residue bit count indicating the number of orphan data bits at the end of the information field is placed in the three most significant bits of the associated Receive Frame Length Register.

There are five sources of interrupts from the receivers. Receive DMA Complete indicates that a good frame was received and has been placed in memory. The Receive Idle interrupt indicates that 15 or more consecutive 'ones' were received. Another interrupt is generated when the CD* pin changes state. This is the CD Interrupt. These interrupts are considered normal operation interrupts. Two other interrupts, related to fault conditions are the FIFO Overrun Interrupt and the Buffer Overrun Interrupt. When a FIFO overrun is detected, bit b8 of the Receive Status Register is set and DMA activity on that channel is suspended. If a received frame is too large for the buffer in memory, the Buffer Overrun bit (b9 or b10) is set, DMA activity on that channel is suspended and the Buffer Overrun Interrupt is queued.

In the transparent mode, the DDLC passes the received data directly to memory. No HDLC de-framing is used.

2.3 FIRST-IN, FIRST-OUT BUFFERS (FIFOs)

The protocol blocks of the DDLC are asynchronous to the MPU blocks so a buffer mechanism is required to synchronize the two sections. Four FIFOs, one for each receiver and transmitter channel provide the synchronization. They also buffer the data so DMA requests are minimized. This section will describe the FIFOs.

2.3.1 Receive FIFOs

Each receiver has a FIFO which interfaces it to the DMA controller. The FIFO is an 8-bit by 4-byte buffer which can be read and written simultaneously. Serial bytes are produced by the receiver and converted to parallel. As each byte is formed, it is pushed into the FIFO. A counter in the FIFO controller keeps track of the occupancy of the buffer and requests that the DMA controller place a word of data (16-bits) in memory when there are two or more bytes in the FIFO. If the FIFO overruns because the DMA controller did not service a request, an interrupt is queued. When a receiver is operating at 64k bps, DMA requests from that channel will occur at approximately 250 µs intervals.

A Tag bit which moves through the FIFO with the data is provided which indicates that the byte associated with the Tag is the last byte of a data frame. When the DMA controller detects the Tag, it closes the buffer in memory and queues an interrupt.

2.3.2 Transmit FIFOs

Each transmitter has a FIFO which interfaces it to the DMA controller. The FIFO is identical to the receive FIFO except that the data flows in the opposite direction. When the host has a message to send, the DMA controller will fill the transmit FIFO and attempt to keep it full. A counter in the FIFO controller keeps track of the occupancy of the buffer and requests that the DMA controller load a word of data (16-bits) when the FIFO empties to two or less bytes. If the FIFO underruns because the DMA controller did not service a request, an interrupt is queued and the current frame in transmission is aborted. A Tag bit scheme similar to that used in the receivers is implemented in the transmit FIFOs.

2.4 DMA CONTROLLER

In order to relieve the host from critically timed data transfers to or from the protocol controllers, the DDLC provides four DMA channels, one for each transmitter and receiver. This section will describe the operation of the DMA controller and the various buffer descriptor registers.

2.4.1 DMA Operation

When the DMA controller detects a service request from one of the FIFOs, it in turn requests ownership of the system bus from the host. When ownership is granted, the DMA controller assumes ownership and transfers data either to or from memory. Transfers are 16 bits or 8 bits depending on the bus width and the type of request. In a 16-bit system, all transfers will be word-wide. If however, the number of bytes in a frame is odd, the last byte will be read or written as a byte. In 8-bit systems, all transfers will be 8 bits but two transfers will be made for every DMA request.

The DDLC will attempt to service all pending DMA requests with one bus arbitration cycle. For example, if Receive Channel 0 and Transmit Channel 1 have requests pending, when the DDLC assumes ownership of the bus, both requests will be serviced before bus ownership is relinquished. The servicing mechanism does not prioritize requests. All requests are serviced in the order: Receive Channel 0, Receive Channel 1, Transmit Channel 0 and Transmit Channel 1. If Receive Channel 0 and Transmit Channel 1 have pending requests, and while Receive Channel 0 is being serviced, Receive Channel 1 generates a request. Receive Channel 1 will be serviced before Transmit Channel 1. The DMA controller will relinquish bus ownership only when all requests have been serviced. This characteristic must be noted when using the DDLC at high serial data rates. When high speed data is transferred, the DDLC can consume excessive bus bandwidth and generate interrupts quickly.

It is impossible to precisely predict what the DDLC's bus occupancy will be, but worst case with both

channels operating full-duplex at 64k bps and an 8 MHz MCLK, approximately 2% of the host's bus bandwidth will be consumed by the DDLC.

2.4.2 Buffer Descriptors

As previously stated, the DDLC has four DMA channels. Pointer registers and counters are required so that the DMA controller knows where to place data in, or fetch data from memory. The two transmit channels buffer descriptors are identical, but the two receive channels have different applications and thus different buffer descriptor structures.

2.4.2.1 Receive Buffer Descriptors

The Receive Buffer Descriptors have a 16-bit Buffer Start Address Register, a 12-bit Buffer Length Register, a 12-bit Frame Length Register and a 3-bit Residue Register. The 16-bit Start Address Register provides 64k byte address range. The Buffer Start Address Register contains the address of the first word of the data buffer which will accept a data frame. The 12-bit Buffer Length Register indicates the length of the buffer. Buffers of up to 4096 bytes may be built. The DMA controller will never place data outside of the boundaries set-up by these two registers. If a received frame is larger than a buffer, the Buffer Overrun interrupt will be queued and further activity on that buffer will be halted. The receiver will immediately enter the flag search state to look for a new frame. The fault condition will be indicated by the Buf X Ovrn or Buf Y Ovrn bits (b9 or b10 of the Receive Status Register).

Once a data frame has been completely received, the number of bytes received is indicated in the Frame Length Register. The number in this register is valid only when the Receive DMA Complete bit (b1 in the Receive Status Register) is set to one. If non-octet aligned frames are received, the number of orphan bits (valid bits) in the last byte is indicated in the three most significant bits of the associated Receive Frame Length Register. For octet-aligned systems, the residue count will be zero.

Channel 0 is intended for higher speed applications than Channel 1, so a pair of buffer descriptors is provided for this channel. These may be used alternately so that while one buffer is filling, another buffer is ready in-waiting. If back-to-back data frames are received, after the first buffer has been closed, the second is immediately ready for the next frame. There must be at least one buffer ready to accept data. If both descriptors are prepared, the X Buffer will be filled first then the Y Buffer. If no buffers are ready and the receive FIFO overruns, a FIFO Overrun interrupt will be queued indicating the overrun.

Two Buffer Ready bits (Buf X Rdy and Buf Y Rdy, bits b1 and b2 of the Receive Status/Control Register) are provided which allow the DMA controller to operate on that buffer. DMA activity on a receive channel will begin when there is data in the FIFO and a buffer ready bit is set. As the buffer fills, the byte count increments. When the last byte has been placed in memory and the CRC has been checked OK, the selected buffer ready bit (Buf X Rdy or Buf Y Rdy) is cleared halting future DMA activity on that buffer.

There is one buffer descriptor for Channel 1. Since this channel is intended for operation at 16k bps, one descriptor is sufficient. At 16k bps, if back-to-back frames are received, the host has approximately 1000 µs to prepare another buffer before the FIFO overruns.

A semaphore bit, the Buffer Active Bit, (Buf X Active and Buf Y Active for Channel 0) is provided in the Receive Status Register for each buffer indicating that DMA controller is active on that buffer. If a buffer is active, the host should not modify the buffer descriptor, as the data may be placed in an unintended location. The current DMA address pointer is calculated by adding the byte count to the Buffer Starting Address. If the start address is modified, the DMA controller will place the next received byte n-bytes from the modified starting address where 'n' is the current contents of the byte count register.

2.4.2.2 Transmit Buffer Descriptors

When the host has a frame of data to transmit, it informs the DMA controller where the data resides in memory. A 16-bit register, the Transmit Buffer Start Address Register is used to point to the first word of the transmitted frame. The 16-bit address registers provide 64k byte address range. The host programs the address of the first word to be transmitted into this register. The length of the data frame must also be given to the DMA controller so a 12-bit register, the Transmit Buffer Length Register, is used to indicate the length of the frame in bytes. Frames of up to 4096 bytes may be transmitted. An internal counter keeps track of the number of bytes transferred to the FIFO. When its count equals the number in the Buffer Length Register, an End-of-Frame Tag is generated and loaded into the FIFO along with the last byte and further DMA activity on that channel is suspended. The host prepares another frame by setting up another buffer descriptor and setting the Buffer Ready bit high.

The Transmission Active bit (b12 in the Transmit Status/Control Register) is a semaphore which indicates that the DMA controller is actively working on a data frame. Once the DMA controller has transferred the last byte of a frame to the FIFO, this bit is reset. The host should not modify a buffer descriptor if its associated semaphore bit is active or undesired data may be transmitted.

Two interrupts related to the semaphore are produced. One is the DMA Complete interrupt which indicates that the last byte of data has been transferred to the transmit FIFO. For applications where back-to-back frames are desired, this interrupt should be unmasked. At 64k bps, the host has approximately 625 µs before the transmitter enters the interframe time-fill state, so a new buffer descriptor should be set up in that time if back-to-back frames are desired to be transmitted.

2.5 MICROPROCESSOR INTERFACE

The microprocessor block interfaces the internal 16-bit bus to the host's 8 or 16 bit bus. All timing conversion and buffering is also performed. This block has three modes of operation: system slave, system master and interrupt generator. This section will describe the operation of these three modes.

2.5.1 System Slave Mode

When the DDLC is in this mode, it appears as memory to the host processor. The host can read or write to the registers in the DDLC. This mode is entered when the CS* pin is activated. Internal address decoding circuitry is selected and the desired register is placed on the internal bus for access by the host. Either 16 bit or 8 bit tran-

sactions may be made as selected by the BUSW (bus width) pin. In certain systems the DDLC may appear to be a slow memory device, so a bus wait feature is supported to request that wait states be inserted For a 68000 system, one wait state is used for each access.

2.5.2 System Master Mode

During DMA operation the DDLC becomes a system master and controls the system bus. When one of the internal FIFOs requests a DMA transfer, the DDDLC negotiates with the system host for ownership of the bus. After successful negotiation, all pending DMA requests are serviced then the bus is relinquished. The DDLC has the capability of reading and writing data from or to memory. Either 16 bit or 8 bit data is transferred depending on the setting of the BUSW pin. If the memory system is slow, the DDLC inserts wait states until the memory completes the access. The DDLC has the capability of recovering from system faults such as address or bus errors. If one of these faults are detected, the DDLC will disable the particular DMA channel which encountered the fault and queue an interrupt indicating the fault. Other DMA channels requesting service will be serviced as soon as the fault signal is removed. The pointers in the DMA register which had the fault remain where they were when the fault was detected, so the host may investigate the problem.

2.5.3 Interrupt Operation

The DDLC has 24 interrupt sources to inform the host of its status. One group of interrupts is normal operation interrupts. These inform the host that a particular task was completed and that further tasks are desired. Another group is bit handler faults which inform the host that a DDLC channel had a fault from which it cannot recover without assitance from the host. The last group of interrupts is the system faults. These include bus errors and address errors. When a DMA channel encounters one of these errors, it stops operation on the affected channel and informs the host that the channel had been disabled. All interrupts are maskable. In the case of the system faults, all channels' interrupts are enabled or masked as a group.

The interrupts are presented to the host as a vector number in an Interrupt Acknowledge cycle. The interrupts are encoded into four bits so the DDLC's vector space consumes 16 out of 256 locations. For applications not using vectored interrupts, the vector number is accessable in the Master Status/Control Register.

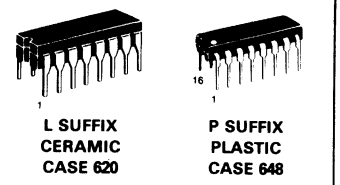
The interrupts are queued internally and a priority mechanism is used to ensure that the most important interrupt is serviced first.

MOTOROLA

MC145500
MC145501
MC145502
MC145503
MC145505

Advance Information

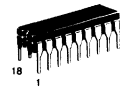
PCM Codec/Filter Mono-Circuit



L SUFFIX
CERAMIC
CASE 620

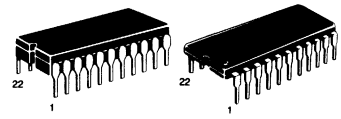
P SUFFIX
PLASTIC
CASE 648

MC145500/03/05



L SUFFIX
CERAMIC
CASE 726

MC145501



L SUFFIX
CERAMIC
CASE 736

P SUFFIX
PLASTIC
CASE 708

MC145502

DW SUFFIX
SO
CASE 751
MC145503
MC145505

FN SUFFIX
CHIP CARRIER
CASE 776
MC145502

The MC145500, MC145501, MC145502, MC145503, and MC145505 are all per channel PCM codec/filter mono-circuits. These devices perform the voice digitization and reconstruction as well as the band limiting and smoothing required for PCM systems. The MC145500 and MC145503 are general purpose devices that are offered in a 16-pin package. They are designed to operate in both synchronous and asynchronous applications and contain an on chip precision reference voltage. The MC145501 is offered in an 18-pin package and adds the capability of selecting from three peak overload voltages (2.5, 3.15, and 3.78 V). The MC145505 is a synchronous device offered in a 16-pin DIP and wide body SOIC package intended for instrument use. The MC145502 is the full-featured device which presents all of the options of the chip. This device is packaged in a 22-pin DIP and a 28-pin chip carrier package and contains all the features of the MC145500 and MC145501 plus several more. Most of these features can be made available in a lower pin count package tailored to a specific user's application. Contact the factory for further details.

These devices are pin-for-pin replacements for Motorola's first generation of MC14400/01/02/03/05 PCM mono-circuits and upwardly compatible with the MC14404/06/07 codecs and other industry standard codecs. They also maintain compatibility with Motorola's family of TSACs and MC3419 SLIC products.

The MC145500 family of PCM codec/filter mono-circuits utilizes CMOS due to its reliable low-power performance and proven capability for complex analog/digital VLSI functions.

MC145500
- 16-Pin Package
- Transmit Bandpass and Receive Low-Pass Filters on Chip
- Pin Selectable Mu/A Law Companding with Corresponding Data Format
- On Chip Precision Reference Voltage (3.15 V)
- Power Dissipation of 50 mW, Power Down of 0.1 mW at ±5 Volts
- Automatic Prescaler Accepts 128 kHz, 1.536, 1.544, 2.048, and 2.56 MHz for Internal Sequencing

MC145501—All of the Above Plus:
- 18-Pin Package
- Selectable Peak Overload Voltages (2.5, 3.15, 3.78 Volts)
- Access to the Inverting Input of the Txl Input Operational Amplifier

MC145502—All of the Above Plus:
- 22-Pin Package
- Variable Data Clock Rates (64 kHz to 4.1 MHz)
- Complete Access to the Three Terminal Transmit Input Operational Amplifier
- An External Precision Reference May Be Used

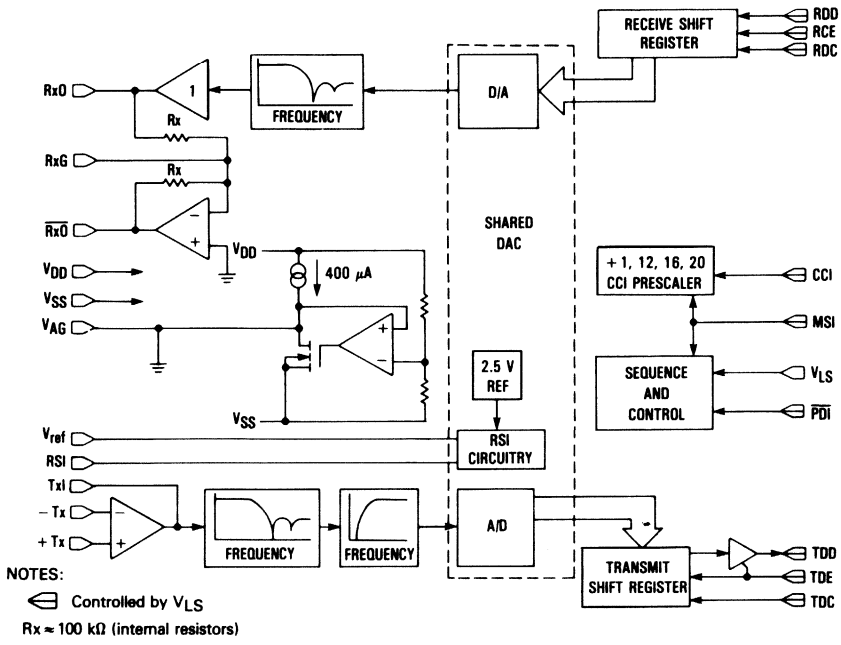
MC145503—All the Above Features of the MC145500 Plus:
- 16-Pin Package
- Complete Access to the Three Terminal Transmit Input Operational Amplifier

MC145505—Same as MC145503 Except:
- 16-Pin Package
- Common 6 kHz to 4.1 MHz Transmit/Receive Data Clock

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ADI 1287

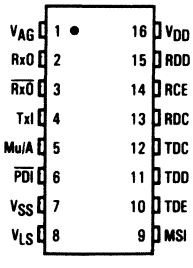
MC145500/01/02/03/05 PCM CODEC/FILTER MONO-CIRCUIT BLOCK DIAGRAM



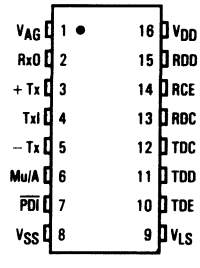
PIN ASSIGNMENT

(Drawings Do Not Reflect Relative Size)

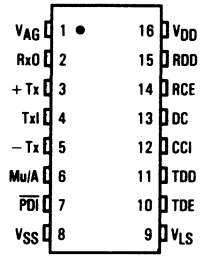
MC145500L



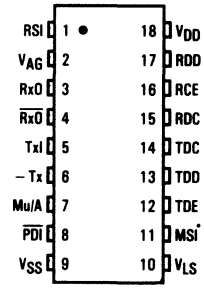
MC145503L,P



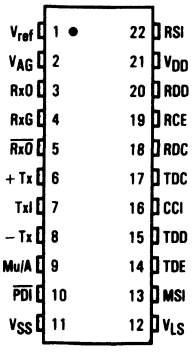
MC145505L,P



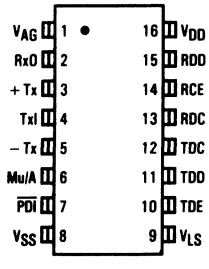
MC145501L



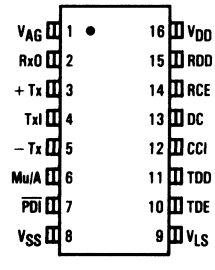
MC145502L,P

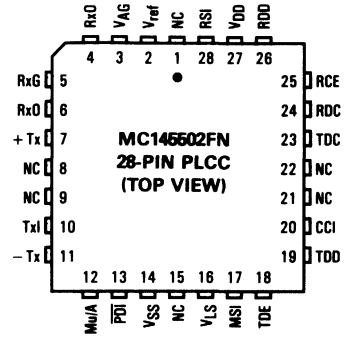


MC145503DW



MC145505DW





MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	$V_{DD} - V_{SS}$	−0.5 to 13	V
Voltage, Any Pin to V_{SS}	V	−0.5 to V_{DD} + 0.5	V
DC Drain Per Pin (Excluding V_{DD}, V_{SS})	I	10	mA
Operating Temperature Range	T_A	− 40 to + 85	°C
Storage Temperature Range	T_{stg}	−85 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = −40 to +85°C)

Characteristic		Min	Typ	Max	Unit
DC Supply Voltage					V
Dual Supplies: $V_{DD} = -V_{SS}$, ($V_{AG} = V_{LS} = 0$ V)		4.75	5.0	6.3	
Single Supply: V_{DD} to V_{SS} (V_{AG} is an Output, $V_{LS} = V_{DD}$ or V_{SS})					
MC145500, MC145501, MC145502, MC145503, MC145505 (Using Internal 3.15 V Reference)		8.5	–	12.6	
MC145501, MC145502 Using Internal 2.5 V Reference		7.0	–	12.6	
MC145501, MC145502 Using internal 3.78 V Reference		9.5	–	12.6	
MC145502 Using External 1.5 V Reference, Referenced to V_{AG}		4.75	–	12.6	
Power Dissipation					mW
CMOS Logic Mode (V_{DD} to V_{SS} = 10 V, $V_{LS} = V_{DD}$)		–	40	70	
TTL Logic Mode (V_{DD} = +5 V, V_{SS} = −5 V, $V_{LS} = V_{AG} = 0$ V)		–	50	90	
Power Down Dissipation		–	0.1	1.0	mW
Frame Rate Transmit and Receive		7.5	8.0	8.5	kHz
Data Rate		–	128	–	kHz
MC145500, MC145501, MC145503		–	1536	–	
Must Use One of These Frequencies ±2%, Relative to MSI Frequency of 8 kHz		–	1544	–	
		–	2048	–	
		–	2560	–	
Data Rate for MC145502, MC145505		64	–	4096	kHz
Full Scale Analog Input and Output Level					V_P
MC145500, MC145503, MC145505		–	3.15	–	
MC145501, MC145502 ($V_{ref} = V_{SS}$)	RSI = V_{DD}	–	3.78	–	
	RSI = V_{SS}	–	3.15	–	
	RSI = V_{AG}	–	2.5	–	
MC145502 Using an External Reference Voltage Applied at V_{ref} Pin	RSI = V_{DD}	–	1.51 × V_{ref}	–	
	RSI = V_{SS}	–	1.26 × V_{ref}	–	
	RSI = V_{AG}	–	V_{ref}	–	

DIGITAL LEVELS (V_{SS} to V_{DD} = 4.75 V to 12.6 V, T_A = −40 to +85°C)

Characteristic		Symbol	Min	Max	Unit
Input Voltage Levels (TDE, TDC, RCE, RDC, RDD, DC, MSI, CCI, PDI)					V
CMOS Mode ($V_{LS} = V_{DD}$, V_{SS} is Digital Ground)	"0"	V_{IL}		0.3 × V_{DD}	
	"1"	V_{IH}	0.7 × V_{DD}		
TTL Mode ($V_{LS} \leq V_{DD} - 4.0$ V, V_{LS} is Digital Ground)	"0"	V_{IL}		V_{LS} + 0.8 V	
	"1"	V_{IH}	V_{LS} + 2.0 V		
Output Current for TDD (Transmit Digital Data)					mA
CMOS Mode ($V_{LS} = V_{DD}$, $V_{SS} = 0$ V and is Digital Ground)					
(V_{DD} = 5 V, V_{out} = 0.4 V)		I_{OL}	4.0		
(V_{DD} = 10 V, V_{out} = 0.5 V)			6.0		
(V_{DD} = 5 V, V_{out} = 4.5 V)		I_{OH}	−4.0		
(V_{DD} = 10 V, V_{out} = 9.5 V)			−6.0		
TTL Mode ($V_{LS} \leq V_{DD} - 4.75$ V, $V_{LS} = 0$ V and is Digital Ground)	V_{OL} = 0.4 V	I_{OL}	1.6		
	V_{OH} = 2.4 V	I_{OH}	−0.2		

ANALOG TRANSMISSION PERFORMANCE

(V_{DD} = +5 V ±5%, V_{SS} = −5 V ±5%, V_{LS} = V_{AG} = 0 V, V_{ref} = RSI = V_{SS} (Internal 3.15 V Reference), 0 dBm0 = 1.546 Vrms = +6 dBm @ 600 Ω, T_A = −40 to +85°C, TDC = RDC = CCI, TDE = RCE = MSI, Unless Otherwise Noted)

Characteristic		End to End		A/D		D/A		Unit
		Min	Max	Min	Max	Min	Max	
Absolute Gain (0 dBm0 @ 1.02 kHz), T_A = 25°C, V_{DD} = 5 V, V_{SS} = 5 V		–	–	−0.30	+0.30	−0.30	+0.30	dB
Absolute Gain Variation With Temperature 0° to +70°C		–	–	–	±0.03	–	±0.03	dB
Absolute Gain Variation With Temperature −40° to +85°C		–	–	–	±0.1	–	±0.1	dB
Absolute Gain Variation With Power Supply (V_{DD} = 5 V, V_{SS} = 5 V, 5%)		–	–	–	±0.02	–	±0.02	dB
Gain vs Level Tone (Relative to −10 dBm0, 1.02 kHz)	+3 to −40 dBm0	−0.4	+0.4	−0.2	+0.2	−0.2	+0.2	dB
	−40 to −50 dBm0	−0.8	+0.8	−0.4	+0.4	−0.4	+0.4	
	−50 to −55 dBm0	−1.6	+1.6	−0.8	+0.8	−0.8	+0.8	
Gain vs Level Pseudo Noise (A-Law Relative to −10 dBm0) CCITT G.714	−10 to −40 dBm0	–	–	−0.25	+0.25	−0.25	+0.25	dB
	−40 to −50 dBm0	–	–	−0.30	+0.30	−0.30	+0.30	
	−50 to −55 dBm0	–	–	−0.45	+0.45	−0.45	+0.45	
Total Distortion—1.02 kHz Tone (C-Message)	0 to −30 dBm0	35	–	35	–	36	–	dBC
	−40 dBm0	29	–	29	–	30	–	
	−45 dBm0	24	–	24	–	25	–	
Total Distortion With Pseudo Noise (A-Law), CCITT G.714	−3 dBm0	27.5	–	28	–	28.5	–	dB
	−6 to −27 dBm0	35	–	35.5	–	36	–	
	−34 dBm0	33.1	–	33.5	–	34.2	–	
	−40 dBm0	28.2	–	28.5	–	30.0	–	
	−55 dBm0	13.2	–	13.5	–	15.0	–	
Idle Channel Noise (For End-End and A/D, See Note 1) (Mu-Law, C-Message Weighted)		–	15	–	15	–	9	dBmC0
(A-Law, Psophometric Weighted)		–	−69	–	−69	–	−78	dBmOp
Frequency Response (Relative to 1.02 kHz @ 0 dBm0)	15 to 60 Hz	–	−23	–	−23	–	0.15	dB
	300 to 3000 Hz	−0.3	+0.3	−0.15	+0.15	−0.15	+0.15	
	3400 Hz	−1.6	0	−0.8	0	−0.8	0	
	4000 Hz	–	−28	–	−14	–	−14	
	≥4600 Hz	–	−60	–	−32	–	−30	
Inband Spurious (1.02 kHz @ 0 dBm0, Transmit and RxO)	300 to 3000 Hz	–	–	–	−43	–	−43	dBm0
Out-of-Band Spurious at RxO (300-3400 Hz @ 0 dBm0 In)								dB
	4600 to 7600 Hz	–	−30	–	–	–	−30	
	7600 to 8400 Hz	–	−40	–	–	–	−40	
	8400 to 100,000 Hz	–	−30	–	–	–	−30	
Idle Channel Noise Selective @ 8 kHz, Input = V_{AG}, 30 Hz Bandwidth		–	−70	–	–	–	−70	dBm0
Absolute Delay @ 1020 Hz (TDC = 2.048 MHz, TDE = 8 kHz)								
Group Delay Referenced to 1020 Hz (TDC = 2048 kHz, TDE = 8 kHz)								
	500 to 600 Hz							
	600 to 800 Hz							
	800 to 1000 Hz							
	1000 to 1600 Hz							
	1600 to 2600 Hz							
	2600 to 2800 Hz							
	2800 to 3000 Hz							
Crosstalk of 1020 Hz @ 0 dBm0 From A/D or D/A (Note 2)		–	–	–	−80	–	−80	dB
Intermodulation Distortion of Two Frequencies of Amplitudes −4 to −21 dBm0 From the Range 300 to 3400 Hz		–	–	–	−41	–	−41	dB

NOTES:
1. Extrapolated from a 1020 Hz @ −50 dBm0 distortion measurement to correct for encoder enhancement.
2. Selectively measured while the A/D is stimulated with 2667 Hz @ −50 dBm0.

ANALOG ELECTRICAL CHARACTERISTICS ($V_{DD} = -V_{SS} = 5$ V to 6 V $\pm 5\%$, $T_A = -40$ to $+85°C$)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current +Tx, −Tx (TxI for MC145500)	I_{in}	–	±0.01	±0.2	μA
AC Input Impedance to V_{AG} (1 kHz) +Tx, −Tx	Z_{in}	5	10	–	MΩ
(TxI for MC145500)		0.1	0.2	–	
Input Capacitance +Tx, −Tx		–	–	10	pF
Input Offset Voltage of TxI Op Amp		–	< ±30	–	mV
Input Common Mode Voltage Range +Tx, −Tx	V_{ICR}	$V_{SS}+1.0$	–	$V_{DD}-2.0$	V
Input Common Mode Rejection Ratio +Tx, −Tx	CMRR	–	70	–	dB
TxI Unity Gain Bandwidth $R_L \geq 10$ kΩ	BW_p	–	1000	–	kHz
TxI Open Loop Gain $R_L \geq 10$ kΩ	A_{VOL}	–	75	–	dB
Equivalent Input Noise (C-Message) Between +Tx and −Tx, at TxI		–	−20	–	dBrnC0
Output Load Capacitance for TxI Op Amp		0	–	100	pF
Output Voltage Range TxI Op Amp, RxO or $\overline{RxO}$	V_{out}				V
$R_L = 10$ k to V_{AG}		$V_{SS}+0.8$	–	$V_{DD}-1.0$	
$R_L = 600$ Ω to V_{AG}		$V_{SS}+1.5$	–	$V_{DD}-1.5$	
Output Current TxI, RxO, $\overline{RxO}$ $V_{SS}+1.5\ V \leq V_{out} \leq V_{DD}-1.5\ V$		±5.5	–	–	mA
Output Impedance RxO, $\overline{RxO}$* 0 to 3.4 kHz	Z_{out}	–	3	–	Ω
Output Load Capacitance for RxO and $\overline{RxO}$*		0	–	200	pF
Output dc Offset Voltage Referenced to V_{AG} Pin RxO				±100	mV
$\overline{RxO}$*		–	–	±150	
Internal Gainsetting Resistors for RxG to RxO and $\overline{RxO}$		62	100	225	kΩ
External Reference Voltage Applied to V_{ref} (Referenced to V_{AG})		0.5	–	$V_{DD}-1.0$	V
V_{ref} Input Current		–	–	20	μA
V_{AG} Output Bias Voltage		–	$0.53\ V_{DD}+$	–	V
		–	$0.47\ V_{SS}$	–	
V_{AG} Output Current Source	I_{VAG}	0.4	–	0.8	mA
Sink		10.0	–	–	
Output Leakage Current During Power Down for the TxI Op Amp, V_{AG}, RxO, and $\overline{RxO}$		–	–	±30	μA
Positive Power Supply Rejection Ratio, Transmit		45	50	–	dBC
0-100 kHz @ 250 mV, C-Message Weighting Receive		55	65	–	
Negative Power Supply Rejection Ratio, Transmit		50	55	–	dBC
0-100 kHz @ 250 mV, C-Message Weighting Receive		50	60	–	

*Assumes that RxG is not connected for gain modifications to $\overline{RxO}$.

MODE CONTROL LOGIC (V_{SS} to V_{DD} = 4.75 V to 12.6 V, T_A = −40 to +85°C)

Characteristic	Min	Typ	Max	Unit
V_{LS} Voltage for TTL Mode (TTL Logic Levels Referenced to V_{LS})	V_{SS}	–	$V_{DD}-4.0$	V
V_{LS} Voltage for CMOS Mode (CMOS Logic Levels of V_{SS} to V_{DD})	$V_{DD}-0.5$	–	V_{DD}	V
Mu/A Select Voltage				V
Mu-Law Mode	$V_{DD}-0.5$	–	V_{DD}	
Sign Magnitude Mode	$V_{AG}-0.5$	–	$V_{AG}+0.5$	
A-Law Mode	V_{SS}	–	$V_{SS}+0.5$	
RSI Voltage for Reference Select Input (MC145501 and MC145502)				V
3.78 V Mode	$V_{DD}-0.5$	–	V_{DD}	
2.5 V Mode	$V_{AG}-0.5$	–	$V_{AG}+0.5$	
3.15 V Mode	V_{SS}	–	$V_{SS}+0.5$	
V_{ref} Voltage for Internal or External Reference (MC145502 only)				V
Internal Reference Mode	V_{SS}	–	$V_{SS}+0.5$	
External Reference Mode	$V_{AG}+0.5$	–	$V_{DD}-1.0$	
Analog Test Mode Selection Frequency, MS = CCI (MC145500, MC145501, MC145502 only) See Pin Description; Test Modes	–	128	–	kHz

SWITCHING CHARACTERISTICS (V_{SS} to V_{DD} = 9.5 V to 12.6 V, T_A = −40 to +85°C, C_L = 150 pF CMOS or TTL Mode)

Characteristic		Symbol	Min	Typ	Max	Unit
Output Rise Time	TDD	t_{TLH}	–	30	80	ns
Output Fall Time		t_{THL}	–	30	80	
Input Rise Time	TDE, TDC, RCE, RDC, DC, MSI, CCI	t_{TLH}	–	–	4	µs
Input Fall Time		t_{THL}	–	–	4	
Pulse Width	TDE Low, TDC, RCE, RDC, DC, MSI, CCI	t_W	100	–	–	ns
Data Clock Pulse Frequency	TDC, RDC, DC	f_{CL}	64	–	4096	kHz
CCI Clock Pulse Frequency (MSI = 8 kHz)		f_{CL1}	–	128	–	kHz
This Pin will Accept One of These Discrete Clock Frequencies and will		f_{CL2}	–	1536	–	
Compensate to Produce Internal Sequencing		f_{CL3}	–	1544	–	
		f_{CL4}	–	2048	–	
		f_{CL5}	–	2560	–	
Propagation Delay Time						ns
TDE Rising to TDD Low Impedance	TTL	t_{P1}	–	90	180	
	CMOS		–	90	150	
TDE Falling to TDD High Impedance	TTL	t_{P2}	–	–	55	
	CMOS		–	–	40	
TDC Rising Edge to TDD Data, During TDE High	TTL	t_{P3}	–	90	180	
	CMOS		–	90	150	
TDE Rising Edge to TDD Data, During TDC High	TTL	t_{P4}	–	90	180	
	CMOS		–	90	150	
TDC Falling Edge to TDE Rising Edge Setup Time		t_{su1}	20	–	–	ns
TDE Rising Edge to TDC Falling Edge Setup Time		t_{su2}	100	–	–	ns
TDE Falling Edge to TDC Rising Edge to Preserve the Next TDD Data		t_{su8}	20	–	–	ns
RDC Falling Edge to RCE Rising Edge Setup Time		t_{su3}	20	–	–	ns
RCE Rising Edge to RDC Falling Edge Setup Time		t_{su4}	100	–	–	ns
RDD Valid to RDC Falling Edge Setup Time		t_{su5}	60	–	–	ns
CCI Falling Edge to MSI Rising Edge Setup Time		t_{su6}	20	–	–	ns
MSI Rising Edge to CCI Falling Edge Setup Time		t_{su7}	100	–	–	ns
RDD Hold Time from RDC Falling Edge		t_h	100	–	–	ns
TDE, TDC, RCE, RDC, RDD, DC, MSI, CCI Input Capacitance			–	–	10	pF
TDE, TDC, RCE, RDC, RDD, DC, MSI, CCI Input Current			–	±0.01	±0.2	µA
TDD Capacitance During High Impedance (TDE Low)			–	12	15	pF
TDD Input Current During High Impedance (TDE Low)			–	±0.1	±10.0	µA

3

DEVICE DESCRIPTIONS

A codec/filter is a device which is used for digitizing and reconstructing the human voice. These devices were developed primarily for the telephone network to facilitate voice switching and transmission. Once the voice is digitized, it may be switched by digital switching methods or transmitted long distance (T1, microwave, satellites, etc.) without degradation. The name codec is an acronym from "coder" for the A/D used to digitize voice, and "decoder" for the D/A used for reconstructing voice. A codec is a single device that does both the A/D and D/A conversions.

To digitize intelligible voice requires a signal to distortion of about 30 dB for a dynamic range of about 40 dB. This may be accomplished with a linear 13-bit A/D and D/A, but will far exceed the required signal to distortion at amplitudes greater than 40 dB below the peak amplitude. This excess performance is at the expense of data per sample. Two methods of data reduction are implemented by compressing the 13-bit linear scheme to companded 8-bit schemes. These companding schemes follow a segmented or "piecewise-linear" curve formatted as sign bit, three chord bits, and four step bits. For a given chord, all 16 of the steps have the same voltage weighting. As the voltage of the analog input increases, the four step bits increment and carry to the three chord bits which increment. With the chord bits increment, the step bits double their voltage weighting. This results in an effective resolution of 6-bits (sign + chord + four step bits) across a 42 dB dynamic range (7 chords above zero, by 6 dB per chord). There are two companding schemes used; Mu-255 Law specifically in North America, and A-Law specifically in Europe. These companding schemes are accepted world wide. The tables show the linear quantization levels to PCM words for the two companding schemes.

In a sampling environment, Nyquist theory says that to properly sample a continuous signal, it must be sampled at a frequency higher than twice the signal's highest frequency component. Voice contains spectral energy above 3 kHz, but its absence is not detrimental to intelligibility. To reduce the digital data rate, which is proportional to the sampling rate, a sample rate of 8 kHz was adopted, consistent with a bandwidth of 3 kHz. This sampling requires a low-pass filter to limit the high frequency energy above 3 kHz from distorting the inband signal. The telephone line is also subject to 50/60 Hz power line coupling which must be attenuated from the signal by a high-pass filter before the A/D converter.

The D/A process reconstructs a staircase version of the desired inband signal which has spectral images of the inband signal modulated about the sample frequency and its harmonics. These spectral images are called aliasing components which need to be attenuated to obtain the desired signal. The low-pass filter used to attenuate these aliasing components is typically called a reconstruction or smoothing filter.

The MC145500 series PCM codec/filters have the codec, both presampling and reconstruction filters, a precision voltage reference on chip, and require no external components. There are five distinct versions of the Motorola MC145500 Series.

MC145500

The MC145500 PCM mono-circuit is intended for standard byte interleaved synchronous and asynchronous applications. The TDC pin on this device is the input to both the TDC and CCI functions in the pin description. Consequently, for MSI = 8 kHz, TDC can be one of five discrete frequencies. These are 128 kHz (40 to 60% duty cycle) 1.536, 1.544, 2.048, or 2.56 MHz. (For other data clock frequencies see MC145502 or MC145505.) The internal reference is set for 3.15 volts peak full scale, and the full scale input level at TxI and output level at RxO is 6.3 volts peak-to-peak. This is the +3 dBm0 level of the PCM codec/filter. All other functions are described in the pin description.

MC145501

The MC145501 PCM codec/filter offers the same features and is for the same application as the MC145500, but offers two additional pins and features. The reference select input allows the full scale level of the device to be set at 2.5 V_P, 3.15 V_P, or 3.78 V_P. The −Tx pin allows for external transmit gain adjust and simplifies the interface to the MC3419 SLIC. Otherwise, it is identical to MC145500.

MC145502

The MC145502 PCM codec/filter is the full feature 22-pin device. It is intended for use in applications requiring maximum flexiblity. The MC145502 contains all the features of the MC145500 and MC145501. The MC145502 is intended for bit interleaved or byte interleaved applications with data clock frequencies which are nonstandard or time varying. One of the five standard frequencies (listed above) is applied to the CCI input, and the data clock inputs can be any frequency between 64 kHz and 4.096 MHz. The V_{ref} pin allows for use of an external shared reference or selection of the internal reference. The RxG pin accommodates gain adjustments for the inverted analog output. All three pins of the input gain-setting operational amplifier are present which provide maximum flexibility for the analog interface.

MC145503

The MC145503 PCM mono-circuit is intended for standard byte interleaved synchronous or asynchronous applications. TDC can be one of five discrete frequencies. These are 128 kHz (40 to 60% duty cycle), 1.536, 1.544, 2.048, or 2.56 MHz. (For other data clock frequencies see MC145502 or MC145505.) The internal reference is set for 3.15 volts peak full scale, and the full scale input level at TxI and output level at RxO is 6.3 volts peak-to-peak. This is the +3 dBm0 level of the PCM codec/filter. The +Tx and −Tx inputs provide maximum flexibility for analog interface. All other functions are described in the pin description.

MC145505

The MC145505 PCM mono-circuit is intended for byte interleaved synchronous applications. The MC145505 has all the features of the MC145503 but internally connects TDC and RDC (see pin description) to the DC pin. One of the five standard frequencies (listed above) should be applied to CCI. The data clock input (DC) can be any frequency between 64 kHz and 4.096 MHz.

PIN DESCRIPTION

DIGITAL

V_{LS}—Logic Level Select Input and TTL Digital Ground

V_{LS} controls the logic levels and digital ground reference for all digital inputs and the digital output. These devices can operate with logic levels from full supply (V_{SS} to V_{DD}) or with TTL logic levels using V_{LS} as digital ground. For $V_{LS}=V_{DD}$, all I/O is full supply (V_{SS} to V_{DD} swing) with CMOS switch points. For $V_{SS}<V_{LS}<(V_{DD}-4$ volts), all inputs and outputs are TTL compatible with V_{LS} being the digital ground. The pins controlled by V_{LS} are inputs MSI, CCI, TDE, TDC, RCE, RDC, RDD, $\overline{PDI}$, and output TDD.

MSI—Master Synchronization Input

MSI is used for determining the sample rate of the transmit side and as a time base for selecting the internal prescale divider for the convert clock input (CCI) pin. The MSI pin should be tied to an 8 kHz clock which may be a frame sync or system sync signal. MSI has no relation to transmit or receive data timing, except for determining the internal transmit strobe as described under the TDE pin description. MSI should be derived from the transmit timing in asynchronous applications. In many applications MSI can be tied to TDE. (MSI is tied internally to TDE in MC145503/05.)

CCI—Convert Clock Input

CCI is designed to accept five discrete clock frequencies. These are 128 kHz, 1.536 MHz, 1.544 MHz, 2.048 MHz, or 2.56 MHz. The frequency at this input is compared with MSI and prescale divided to produce the internal sequencing clock at 128 kHz (or 16 times the sampling rate). The duty cycle of CCI is dictated by the minimum pulse width except for 128 kHz, which is used directly for internal sequencing and must have a 40 to 60% duty cycle. In asynchronous applications, CCI should be derived from transmit timing. (CCI is tied internally to TDC in MC145500/01/03.)

TDC—Transmit Data Clock Input

TDC can be any frequency from 64 kHz to 4.096 MHz, and is often tied to CCI if the data rate is equal to one of the five discrete frequencies. This clock is the shift clock for the transmit shift register and its rising edges produce successive data bits at TDD. TDE should be derived from this clock. (TDC and RDC are tied together internally in the MC145505 and are called DC.)

TDE—Transmit Data Enable Input

TDE serves three major functions. The first TDE rising edge following an MSI rising edge generates the internal transmit strobe which initiates an A/D conversion. The internal transmit strobe also transfers a new PCM data word into the transmit shift register (sign bit first) ready to be output at TDD. The TDE pin is the high impedance control for the transmit digital data (TDD) output. As long as this pin is high, the TDD output stays low impedance. This pin also enables the output shift register for clocking out the 8-bit serial PCM word. The logical AND of the TDE pin with the TDC pin clocks out a new data bit at TDD. TDE should be held high for eight consecutive TDC cycles to clock out a complete PCM word for byte interleaved applications. The transmit shift register feeds back on itself to allow multiple reads of the transmit data. If the PCM word is clocked out once per frame in a byte interleaved system, the MSI pin function is transparent and may be connected to TDE.

The TDE pin may be cycled during a PCM word for bit interleaved applications. TDE controls both the high impedance state of the TDD output and the internal shift clock. TDE must fall before TDC rises (t_{su8}) to ensure integrity of the next data bit. There must be at least two TDC falling edges between the last TDE rising edge of one frame and the first TDE rising edge of the next frame. MSI must be available separate from TDE for bit interleaved applications.

TDD—Transmit Digital Data Output

The output levels at this pin are controlled by the V_{LS} pin. For V_{LS} connected to V_{DD}, the output levels are from V_{SS} to V_{DD}. For a voltage of V_{LS} between $V_{DD}-4$ V and V_{SS}, the output levels are TTL compatible with V_{LS} being the digital ground supply. The TDD pin is three-state output controlled by the TDE pin. The timing of this pin is controlled by TDC and TDE. When in TTL mode, this output may be made high-speed CMOS compatible using a pullup resistor. The data format (Mu-Law, A-Law, or sign magnitude) is controlled by the Mu/A pin.

RDC—Receive Data Clock Input

RDC can be any frequency from 64 kHz to 4.096 MHz. This pin is often tied to the TDC pin for applications that can use a common clock for both transmit and receive data transfers. The receive shift register is controlled by the receive clock enable (RCE) pin to clock data into the receive digital data (RDD) pin on falling RDC edges. These three signals can be asynchronous with all other digital pins. The RDC input is internally tied to the TDC input on the MC145505 and called DC.

RCE—Receive Clock Enable Input

The rising edge of RCE should identify the sign bit of a receive PCM word on RDD. The next falling edge of RDC, after a rising RCE, loads the first bit of the PCM word into the receive register. The next seven falling edges enter the remainder of the PCM word. On the ninth rising edge, the receive PCM word is transferred to the receive buffer register and the A/D sequence is interrupted to commence the decode process. In asynchronous applications with an 8 kHz transmit sample rate, the receive sample rate should be between 7.5 and 8.5 kHz. Two receive PCM words may be decoded and analog summed each transmit frame to allow on chip conferencing. The two PCM words should be clocked in as two single PCM words, a minimum of 31.25 μs apart, with a receive data clock of 512 kHz or faster.

RDD—Receive Digital Data Input

RDD is the receive digital data input. The timing for this pin is controlled by RDC and RCE. The data format is determined by the Mu/A pin.

Mu/A Select

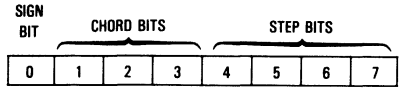
This pin selects the companding law and the data format at TDD and RDD.

Mu/A = V_{DD}; Mu255 Companding D3 Data Format with Zero Code Suppress

Mu/A = V_{AG}; Mu255 Companding with Sign Magnitude Data Format

Mu/A = V_{SS}; A-law Companding with CCITT Data Format Bit Inversions

CODE	SIGN/ MAGNITUDE	Mu-LAW	A-LAW (CCITT)
+ FULL SCALE	1111 1111	1000 0000	1010 1010
+ ZERO	1000 0000	1111 1111	1101 0101
− ZERO	0000 0000	0111 1111	0101 0101
− FULL SCALE	0111 1111	0000 0010	0010 1010



NOTE: Starting from sign magnitude, to change format:

To Mu-Law—
- MSB is unchanged (sign)
- Invert remaining seven bits
- If code is 0000 0000, change to 0000 0010 (for zero code suppression

To A-Law—
- MSB is unchanged (sign)
- Invert odd numbered bits
- Ignore zero code suppression

$\overline{PDI}$—Power Down Input

The power down input disables the bias circuitry and gates off all clock inputs. This puts the V_{AG}, TxI, RxO, $\overline{RxO}$, and TDD outputs into a high impedance state. The power dissipation is reduced to 0.1 mW when $\overline{PDI}$ is a low logic level. The circuit operates normally with $\overline{PDI} = V_{DD}$ or with a logic high as defined by connection at V_{LS}. TDD will not come out of high impedance for two MSI cycles after $\overline{PDI}$ goes high.

DC—Data Clock Input

DC—in the MC145505, TDC and RDC are internally connected to this pin.

ANALOG

V_{AG}—Analog Ground Input/Output Pin

V_{AG} is the analog ground power supply input/output. All analog signals into and out of the device use this as their ground reference. Each version of the MC145500 PCM codec/filter family can provide its own analog ground supply internally. The dc voltage of this internal supply is 6% positive of the midway between V_{DD} and V_{SS}. This supply can sink more than 8 mA but has a current source limited to 400 μA. The output of this supply is internally connected to the analog ground input of the part. The node where this supply and the analog ground are connected is brought out to the V_{AG} pin. In symmetric dual supply systems (±5, ±6, etc.), V_{AG} may be externally tied to the system analog ground supply. When RxO or $\overline{RxO}$ drive low impedance loads tied to V_{AG}, a pullup resistor to V_{DD} will be required to boost the source current capability if V_{AG} is not tied to the supply ground. All analog signals for the part are referenced to V_{AG}, including noise, therefore, decoupling capacitors (0.1 μF) should be used from V_{DD} to V_{AG} and V_{SS} to V_{AG}.

V_{ref}—Positive Voltage Reference Input (MC145502 Only)

The V_{ref} pin allows an external reference voltage to be used for the A/D and D/A conversions. If V_{ref} is tied to V_{SS}, the internal reference is selected. If $V_{ref} > V_{AG}$, then the external mode is selected and the voltage applied to V_{ref} is used for generating the internal converter reference voltage. In either internal or external reference mode, the actual voltage used for conversion is multiplied by the ratio selected by the RSI pin. The RSI pin circuitry is explained under its pin description below. Both the internal and external references are inverted within the PCM codec/filter for negative input voltages such that only one reference is required.

External Mode—In the external reference mode ($V_{ref} > V_{AG}$), a 2.5 volt reference like the MC1403 may be connected from V_{ref} to V_{AG}. A single external reference may be shared by tying together a number of V_{ref} pins and V_{AG} pins from different codec/filters. In special applications, the external reference voltage may be between 0.5 and 5 volts. However, the reference voltage gain selection circuitry associated with RSI must be considered to arrive at the desired codec/filter gain.

Internal Mode—In the internal reference mode ($V_{ref} = V_{SS}$), an internal 2.5 volt reference supplies the reference voltage for the RSI circuitry. The V_{ref} pin is functionally connected to V_{SS} for the MC145500, MC145501, MC145503, and MC145505 pinouts.

RSI—Reference Select Input (MC145501/02 Only)

The RSI input allows the selection of three different overload or full scale A/D and D/A converter reference voltages independent of the internal or external reference mode. The RSI pin is a digital input that senses three different logic states; V_{SS}, V_{AG}, and V_{DD}. For RSI = V_{AG}, the reference voltage is used directly for the converters. The internal reference is 2.5 volts. For RSI = V_{SS}, the reference voltage is multiplied by the ratio of 1.26, which results in an internal converter reference of 3.15 volts. For RSI = V_{DD}, the reference voltage is multiplied by 1.51, which results in an internal converter reference of 3.78 volts. The device requires a minimum of 1.0 volt of headroom between the internal converter reference to V_{DD}. V_{SS} has this same absolute valued minimum, also measured from V_{AG} pin. The various modes of operation are summarized in the table below. The RSI pin is functionally connected to V_{SS} for the MC145500, MC145503, and MC145505 pinouts.

RxO, $\overline{RxO}$—Receive Analog Outputs

These two complimentary outputs are generated from the output of the receive filter. They are equal in magnitude and out of phase. The maximum signal output of each is equal to the maximum peak-to-peak signal described with the reference. If a 3.15 volt reference is used with RSI tied to V_{AG}

and a +3 dBm0 sine wave is decoded, the RxO output will be a 6.3 volt peak-to-peak signal. $\overline{RxO}$ will also have an inverted signal output of 6.3 volt peak-to-peak. External loads may be connected from RxO to $\overline{RxO}$ for a 6 dB push-pull signal gain or from either RxO or $\overline{RxO}$ to V_{AG}. With a 3.15 volt reference each output will drive 600 Ω to +9 dBm. With RSI tied to V_{DD}, each output will drive 900 Ω to +9 dBm.

RxG—Receive Output Gain Adjust (MC145502 Only)

The purpose of the RxG pin is to allow external receive gain adjustment for the $\overline{RxO}$ pin. If RxG is left open, then the output signal at RxO will be inverted and output at $\overline{RxO}$. Thus the push-pull gain to a load from RxO to $\overline{RxO}$ is two times the output level at RxO. If external resistors are applied from RxO to RxG (RI) and from RxG to $\overline{RxO}$ (RG), the gain of $\overline{RxO}$ can be set differently from inverting unity. These resistors should be in the range of 10 kΩ. The RxO output level is unchanged by the resistors and the $\overline{RxO}$ gain is approximately equal to minus RG/RI. The actual gain is determined by taking into account the internal resistors which will be in parallel to these external resistors. The internal resistors have a large tolerance, but they match each other very closely. This matching tends to minimize the affects of their tolerance on external gain configurations. The circuit for RxG and $\overline{RxO}$ is shown in the block diagram.

TxI—Transmit Analog Input

TxI is the input to the transmit filter. It is also the output of the transmit gain amplifiers of the MC145501/02/03/05. The input impedance is greater than 100 k to V_{AG} in the MC145500. The TxI input has an internal gain of 1.0, such that a +3 dBm0 signal at TxI corresponds to the peak converter reference voltage as described in the V_{ref} and RSI pin descriptions. For 3.15 volt reference, the +3 dBm0 input should be 6.3 volts peak-to-peak.

+Tx-Positive Tx Amplifier Input (MC145502/03/05 Only)
−Tx-Negative Tx Amplifier Input (MC145501/02/03/05 Only)

The TxI pin is the input to the transmit band-pass filter. If +Tx or −Tx are available, then there is an internal amplifier preceding the filter whose pins are +Tx, −Tx, and TxI. These pins allow access to the amplifier terminals to tailor the input gain with external resistors. The resistors should be in the range of 10 kΩ. If +Tx is not available, it is internally tied to V_{AG}. If −Tx and +Tx are not available, the TxI is a unity gain high impedance input.

Power Supplies

V_{DD}—Most Positive Supply V_{DD} is typically 5 to 12 volts.

V_{SS}—Most Negative Supply. V_{SS} is typically 10 to 12 volts negative of V_{DD}.

For a ±5 volt dual-supply system, the typical power supply configuration is V_{DD} = +5 V, V_{SS} = −5 V, V_{LS} = 0 V (digital ground accommodating TTL logic levels), and V_{AG} = 0 V being tied to system analog ground.

For single-supply applications, typical power supply configurations include:

V_{DD} = 10 V to 12 V
V_{SS} = 0 V
V_{AG} generates a mid supply voltage for referencing all analog signals.
V_{LS} controls the logic levels. This pin should be connected to V_{DD} for CMOS logic levels from V_{SS} to V_{DD}. This pin should be connected to digital ground for true TTL logic levels referenced to V_{LS}.

Testing Considerations (MC145500/01/02 Only)

An analog test mode is activated by connecting MSI and CCI to 128 kHz. In this mode, the input of the A/D (the output of the Tx filter) is available at the $\overline{PDI}$ pin. This input is direct coupled to the A/D side of the codec. The A/D is a differential design, this results in the gain of this input being effectively attenuated by half. If monitored with a high-impedance buffer, the output of the Tx low-pass filter can also be measured at the $\overline{PDI}$ pin. This test mode allows independent evaluation of the transmit low-pass filter and A/D side of the codec. The transmit and receive channels of these devices are tested with the codec/filter fully functional.

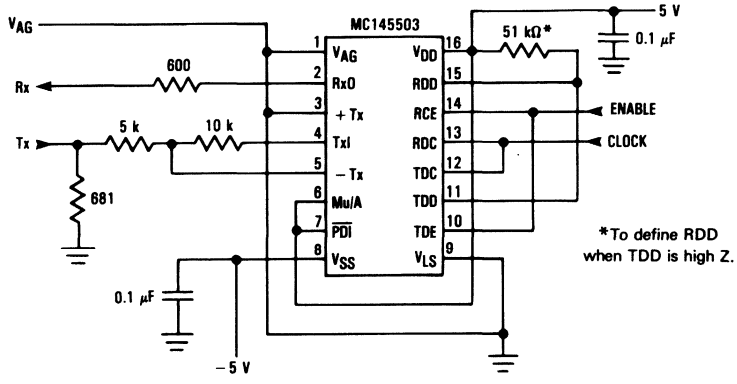


Figure 1. Test Circuit

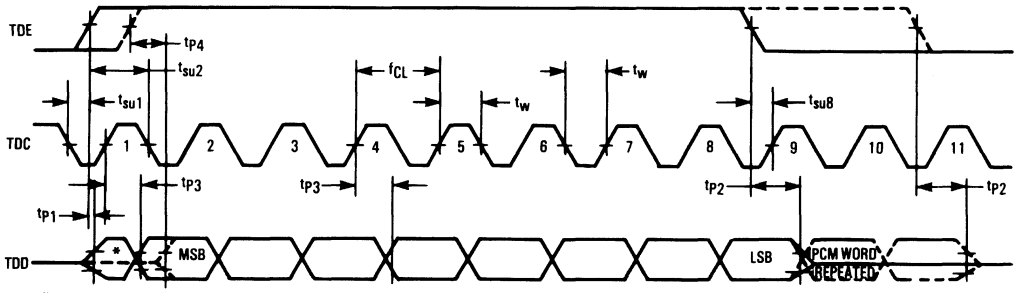
Table 1. Options Available by Pin Selection

RSI* Pin Level	V_{ref}* Pin Level	Peak-to-Peak Overload Voltage (TxI, RxO)
V_{DD}	V_{SS}	7.56 Vpp
V_{DD}	$V_{AG}+V_{EXT}$	$(3.02 \times V_{EXT})$ Vpp
V_{AG}	V_{SS}	5 Vpp
V_{AG}	$V_{AG}+V_{EXT}$	$(2 \times V_{EXT})$ Vpp
V_{SS}	V_{SS}	6.3 Vpp
V_{SS}	$V_{AG}+V_{EXT}$	$(2.52 \times V_{EXT})$Vpp

*On MC145500/03/05, RSI and V_{ref} internally to V_{SS}. On MC145501, V_{ref} tied internally to V_{SS}.

Table 2. Summary of Operation Conditions User Programmed Through Pins V_{DD}, V_{AG}, and V_{SS}

Pin Programmed / Logic Level	Mu/A	RSI Peak Overload Voltage	V_{LS}
V_{DD}	Mu-Law Companding Curve and D3/D4 Digital Formats with Zero Code Suppress	3.78	CMOS Logic Levels
V_{AG}	Mu-Law Companding Curve and Sign Magnitude Data Format	2.50	TTL Levels V_{AG} Up
V_{SS}	A-Law Companding Curve and CCITT Digital Format	3.15	TTL Levels V_{SS} Up



*Data output during this time will vary depending on TDC rate and TDE timing.

Figure 2. Transmit Timing Diagram

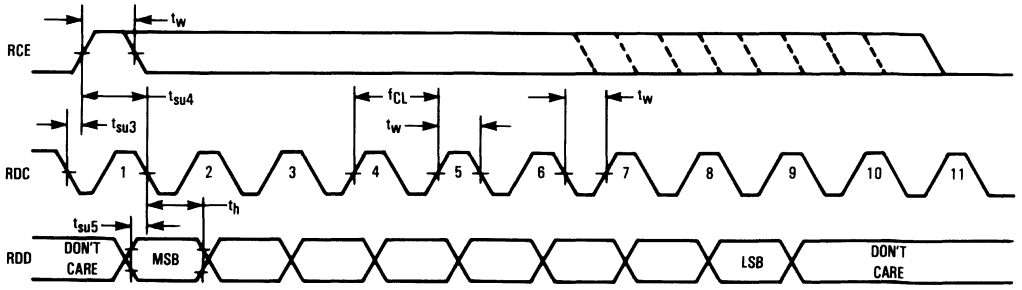


Figure 3. Receive Timing Diagram

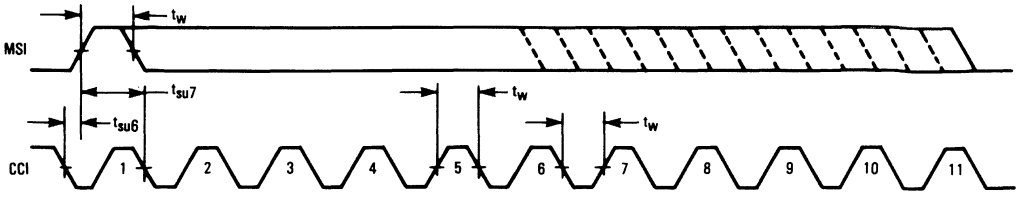


Figure 4. MSI/CCI Timing Diagram

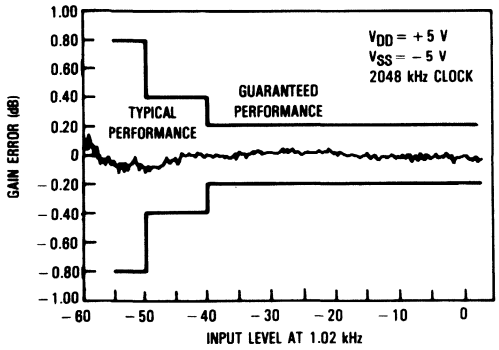


Figure 5. MC145502 Gain vs Level Mu-Law Transmit

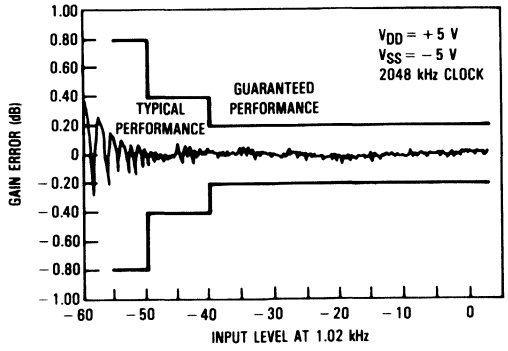


Figure 6. MC145502 Gain vs Level Mu-Law Receive

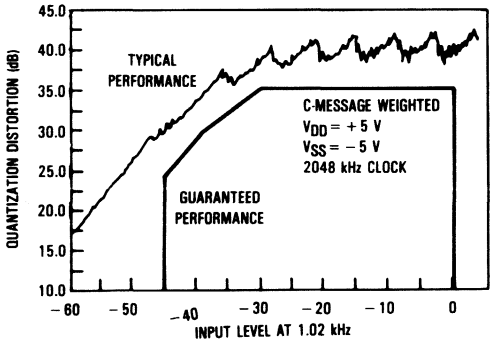


Figure 7. MC145502
Quantization Distortion Mu-Law Transmit

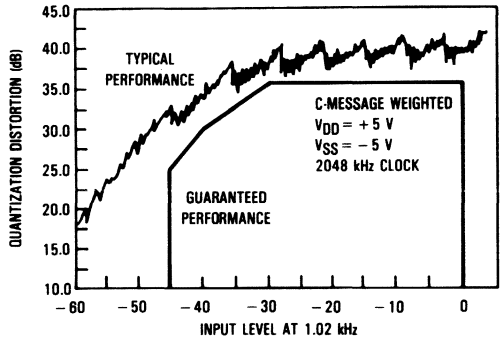


Figure 8. MC145502
Quantization Distortion Mu-Law Receive

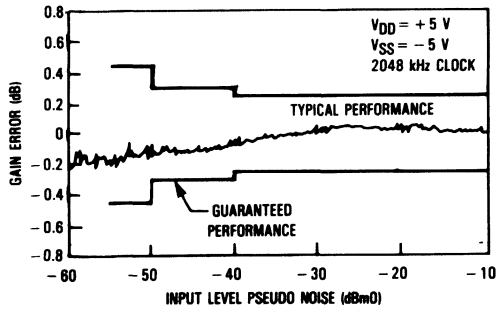


Figure 9. MC145502 Gain vs Level A-Law Transmit

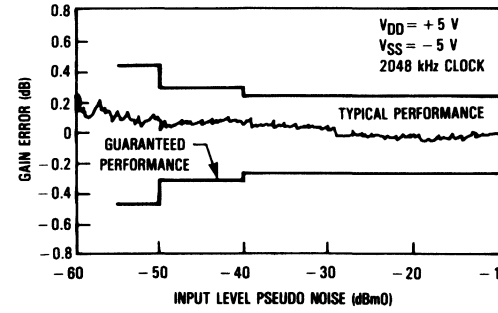


Figure 10. MC145502 Gain vs Level A-Law Receive

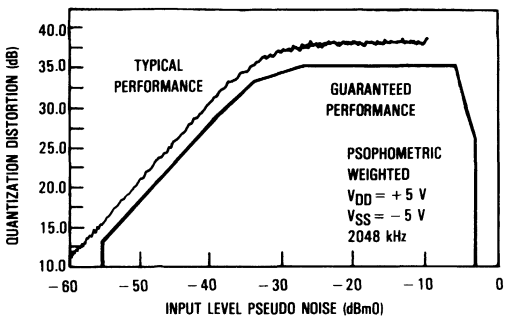


Figure 11. MC145502
Quantization Distortion A-Law Transmit

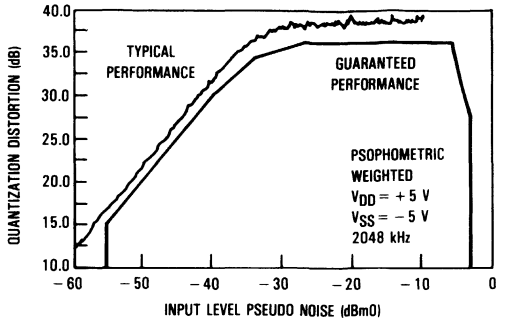


Figure 12. MC145502
Quantization Distortion A-Law Receive

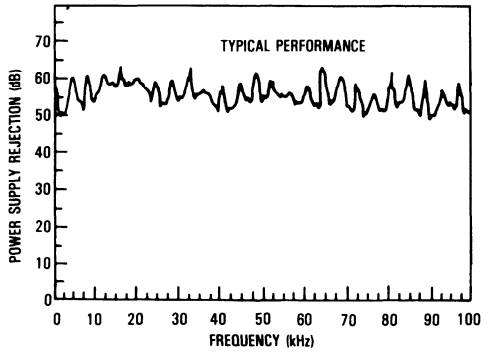


Figure 13. MC145502 Power Supply Rejection Ratio Positive Transmit VAC = 250 mVrms, C-Message Weighted

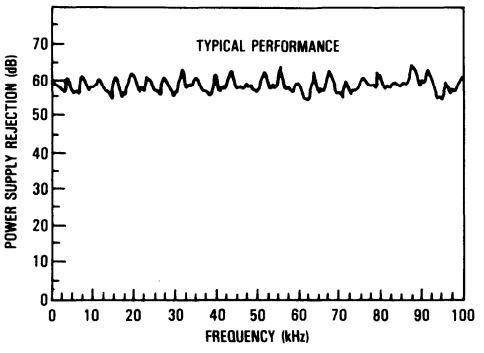


Figure 14. MC145502 Power Supply Rejection Ratio Negative Transmit VAC = 250 mVrms, C-Message Weighted

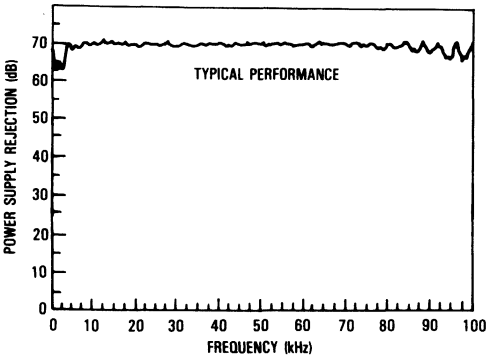


Figure 15. MC145502 Power Supply Rejection Ratio Positive Receive VAC = 250 mVrms, C-Message Weighted

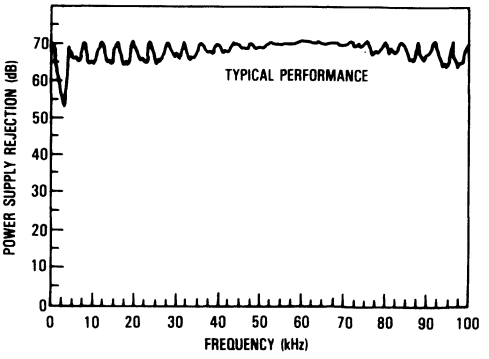


Figure 16. MC145502 Power Supply Rejection Ratio Negative Receive VAC = 250 mVrms, C-Message Weighted

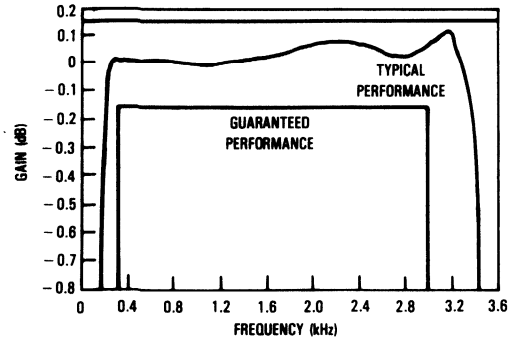


Figure 17. MC145502
Passband Filter Response Transmit

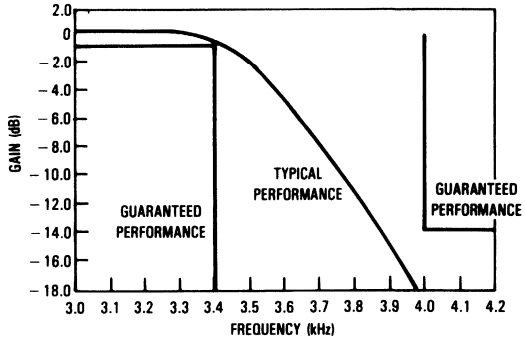


Figure 18. MC145502
Low-Pass Filter Response Transmit

3

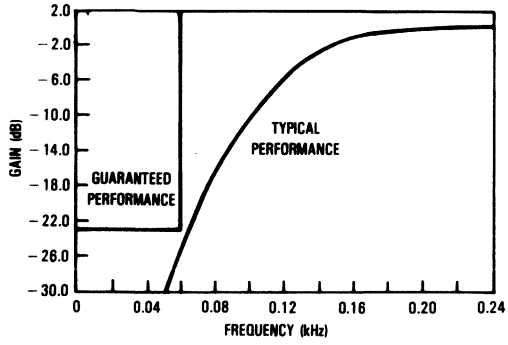


Figure 19. MC145502
High-Pass Filter Response Transmit

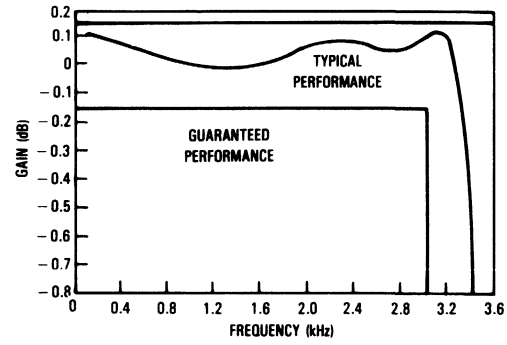


Figure 20. MC145502
Passband Filter Response Receive

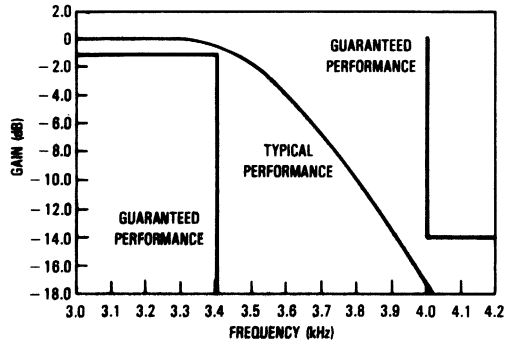


Figure 21. MC145502
Low-Pass Filter Response Receive

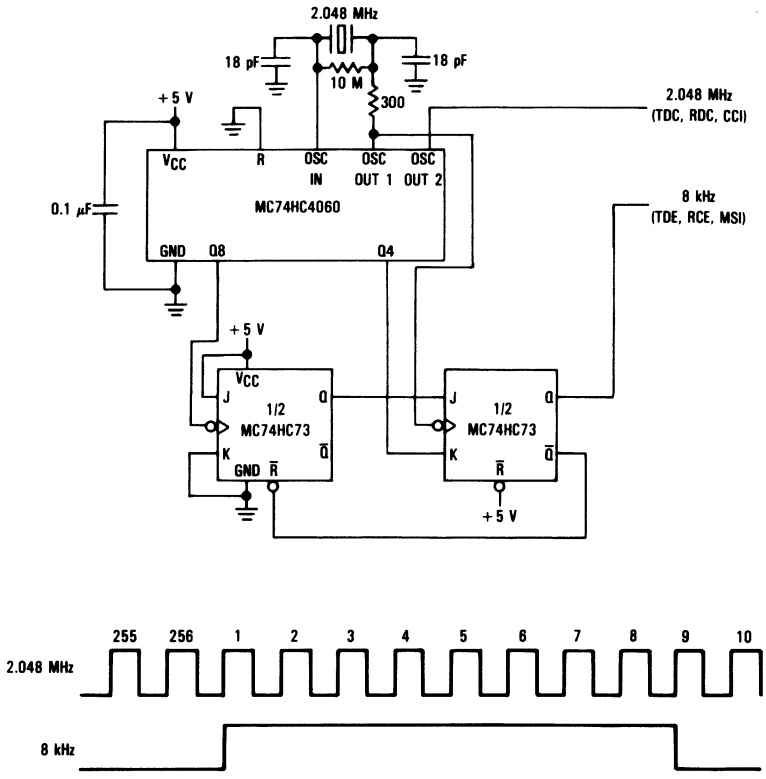
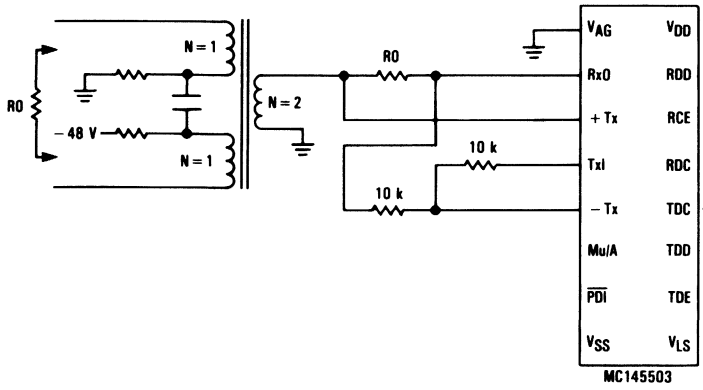
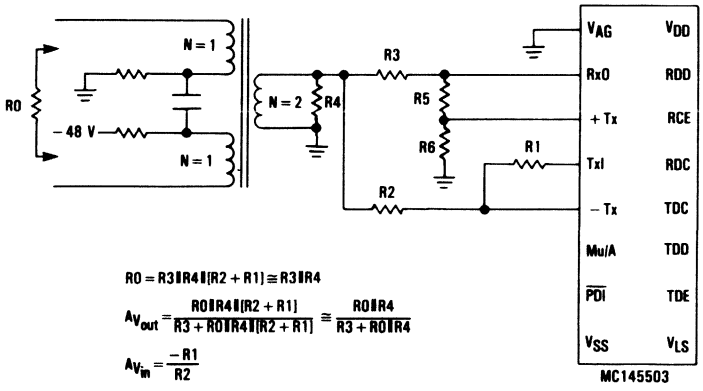


Figure 22. Simple Clock Circuit for Driving MC145500/01/02/03/05 Codec/Filters



(a) SIMPLIFIED TRANSFORMER HYBRID USING MC145503



$$RO = R3 \| R4 \| [R2 + R1] \cong R3 \| R4$$

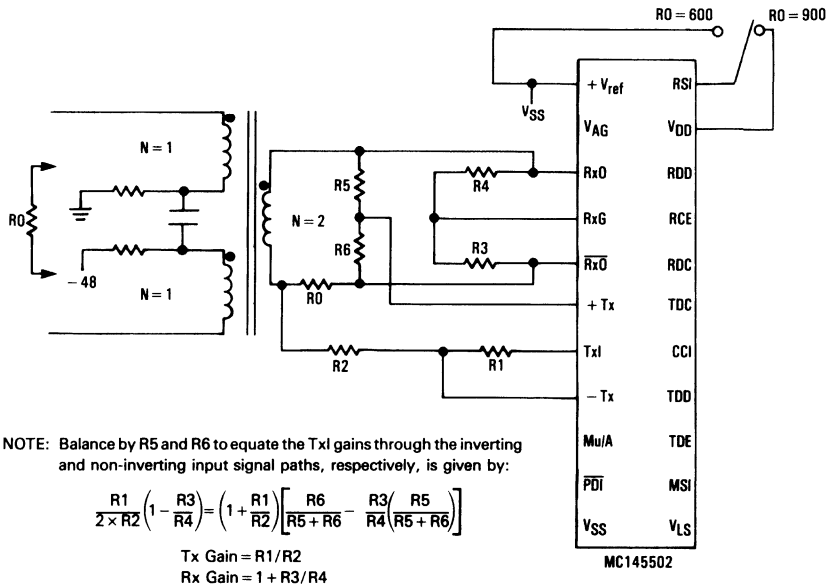
$$A_{V_{out}} = \frac{RO \| R4 \| [R2 + R1]}{R3 + RO \| R4 \| [R2 + R1]} \cong \frac{RO \| R4}{R3 + RO \| R4}$$

$$A_{V_{in}} = \frac{-R1}{R2}$$

NOTE: Hybrid Balance by R5 and R6 to equate the RxO signal gain at TxI through the inverting and non-inverting signal paths.

(b) UNIVERSAL TRANSFORMER HYBRID USING MC145503

Figure 23. Hybrid Interfaces to the MC145503 PCM Codec/Filter Mono-Circuit

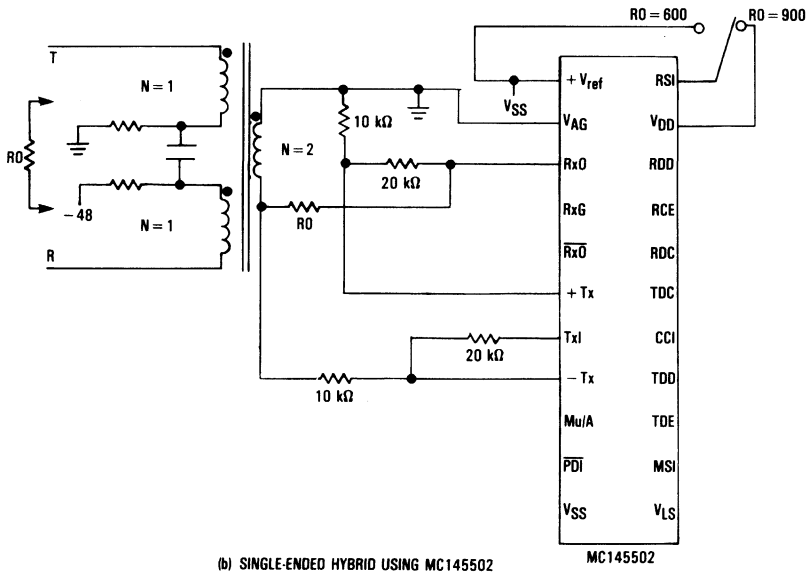


NOTE: Balance by R5 and R6 to equate the TxI gains through the inverting and non-inverting input signal paths, respectively, is given by:

$$\frac{R1}{2 \times R2}\left(1-\frac{R3}{R4}\right)=\left(1+\frac{R1}{R2}\right)\left[\frac{R6}{R5+R6}-\frac{R3}{R4}\left(\frac{R5}{R5+R6}\right)\right]$$

Tx Gain = R1/R2
Rx Gain = 1 + R3/R4
R5, R6 ≅ 10 k
Adjust Rx Gain with R3
Adjust Tx Gain with R1

(a) UNIVERSAL TRANSFORMER HYBRID USING MC145502



(b) SINGLE-ENDED HYBRID USING MC145502

Figure 24. Hybrid Interfaces to the MC145502 PCM Codec/Filter Mono-Circuit

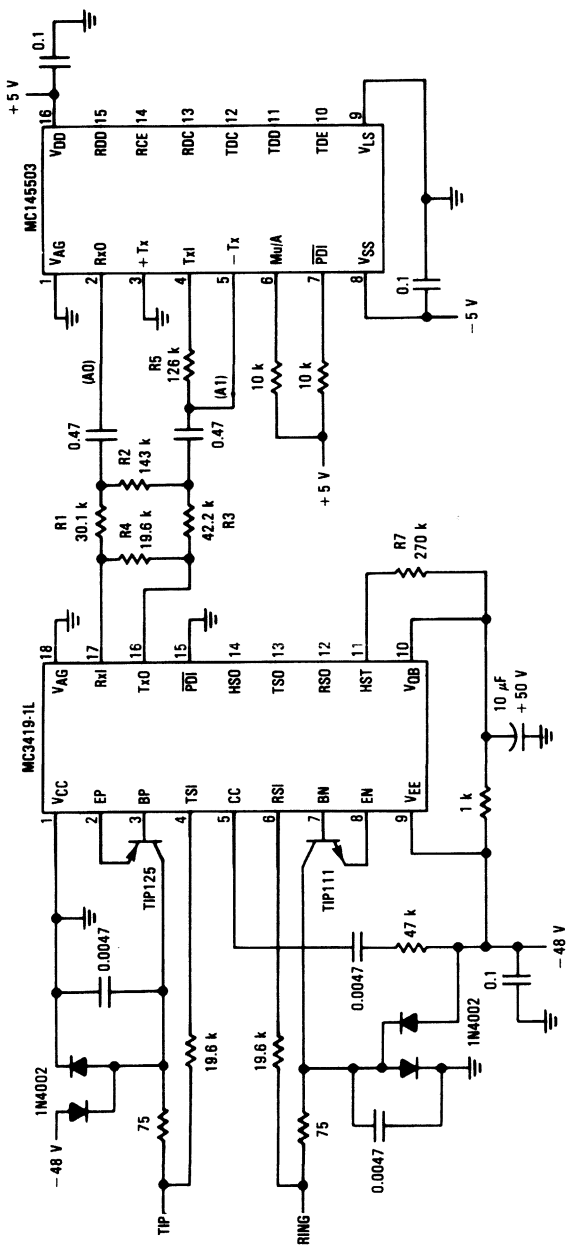
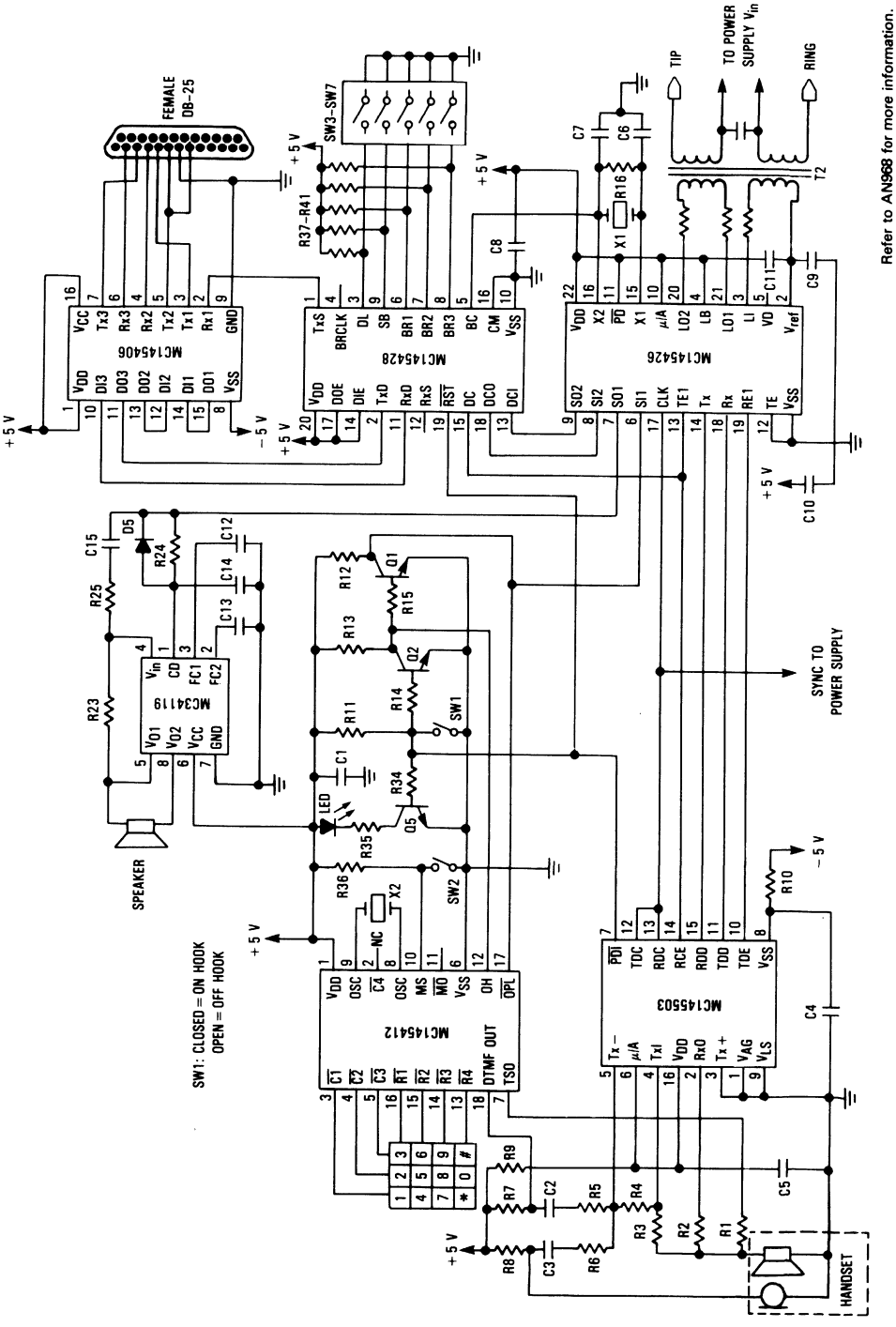


Figure 25. A Complete Single Party Channel Unit Using MC3419 SLIC and MC14403 PCM Mono-Circuit



Refer to AN968 for more information.

Figure 26. Digital Telephone Schematic

Table 3. Mu-Law Encode-Decode Characteristics

Chord Number	Number of Steps	Step Size	Normalized Encode Decision Levels	Digital Code								Normalized Decode Levels
				1	2	3	4	5	6	7	8	
				Sign	Chord	Chord	Chord	Step	Step	Step	Step	
			8159									
8	16	256	7903	1	0	0	0	0	0	0	0	8031
			:					:				:
			4319	1	0	0	0	1	1	1	1	4191
			4063									
7	16	128	:					:				:
			2143	1	0	0	1	1	1	1	1	2079
			2015									
6	16	64	:					:				:
			1055	1	0	1	0	1	1	1	1	1023
			991									
5	16	32	:					:				:
			511	1	0	1	1	1	1	1	1	495
			479									
4	16	16	:					:				:
			239	1	1	0	0	1	1	1	1	231
			223									
3	16	8	:					:				:
			103	1	1	0	1	1	1	1	1	99
			95									
2	16	4	:					:				:
			35	1	1	1	0	1	1	1	1	33
			31									
1	15	2	:					:				:
			3	1	1	1	1	1	1	1	0	2
	1	1	1	1	1	1	1	1	1	1	1	0
			0									

NOTES:
1. Characteristics are symmetrical about analog zero with sign bit = 0 for negative analog values.
2. Digital code includes inversion of all magnitude bits.

Table 4. A-Law Encode-Decode Characteristics

Chord Number	Number of Steps	Step Size	Normalized Encode Decision Levels	Digital Code 1 Sign	2 Chord	3 Chord	4 Chord	5 Step	6 Step	7 Step	8 Step	Normalized Decode Levels
			4096									
7	16	128	3968	1	0	1	0	1	0	1	0	4032
			:				:					:
			2176	1	0	1	0	0	1	0	1	2112
			2048									
6	16	64	:				:					:
			1088	1	0	1	1	0	1	0	1	1056
			1024									
5	16	32	:				:					:
			544	1	0	0	0	0	1	0	1	528
			512									
4	16	16	:				:					:
			272	1	0	0	1	0	1	0	1	264
			256									
3	16	8	:				:					:
			136	1	1	1	0	0	1	0	1	132
			128									
2	16	4	:				:					:
			68	1	1	1	1	0	1	0	1	66
			64									
1	32	2	:				:					:
			2	1	1	0	1	0	1	0	1	1
			0									

NOTES:
1. Characteristics are symmetrical about analog zero with sign bit = 0 for negative analog values.
2. Digital code includes inversion of all magnitude bits.

MOTOROLA

MC145516

Product Preview

TONE/PULSE REPERTORY DIALER WITH FLASH

The MC145516 is a member of the Motorola HCMOS dialer family, with options available to meet UK, French, and Australian national requirements. Three dialing modes are pin selectable: pulse, DTMF, and mixed. Mixed mode allows changing from pulse to DTMF by key entry.

Memory storage is 9 x 18 digit Repertory numbers, 3 x 18 digit Abbreviated recall numbers and 22 digit Last Number Recall (LNR).

LNR uses the moving cursor method with a prefix and main registers, for use in residential and PBX connections.

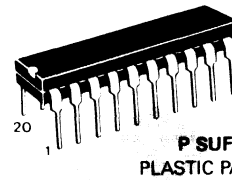
Memory storage is effected off-hook; Memory Recall numbers can be cascaded.

The Flash or Timed Break Recall time is 90 ms nominal, but is extendable with an external RC.

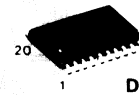
A power-on reset feature avoids problems due to corrupted memory if the power supply fails.

FEATURES

- Standalone DTMF Dialer
- Standalone Pulse Dialer
- Mixed Dialing
- Dial Mode Pin Selectable and Switchable Pulse to Tone from Keyboard.
- Pulse Rate 10 PPS and Make/Break Ratio 33/67
- 4 x 5 Keypad
- Pulse to Tone Mode change with * Key
- Mute during Signalling
- PBX Pause Storage for Memory Dial
- Low Voltage Power-on Reset of Memories
- Flash with Extendable Duration
- 9 x 18 Repertory Memory Stores
- 3 x 18 Abbreviated Recall Stores
- 4 Digit Prefix and 18 Digit External Register moving Cursor LNR (Total 22 Digits).
- Dial Mode Change Storage in 12 x 18 Memories in Mixed Mode
- Memory Cascaded Dialing
- 3.579545 MHz CTV Crystal Reference
- HCMOS, 1.7 - 6V for Pulse and 2.5 - 6V for Tone Operating Voltage
- Voltage Reference for Supply Voltage and Temperature Independent DTMF

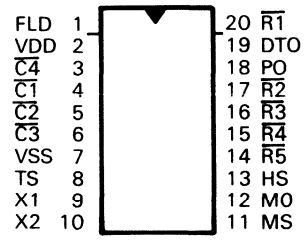


P SUFFIX
PLASTIC PACKAGE
CASE 738



DW SUFFIX
PLASTIC PACKAGE
CASE 751D

PIN ASSIGNMENT



Pin compatible from 2 to 19 with MC145410/12/13

This document contains information on a new product.
Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply voltage	V_{DD}	-0.5 to +8.0	V
Input Voltage, any input	V_{in}	-0.5 to V_{DD}	V
DC Current drain, per pin	I	10	mA
Operating Temperature	TA	-25 to +60	°C
Storage Temperature	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.0V, V_{SS} = 0, FO = 3.579545 MHz, TA = -25 to +60°C unless otherwise stated)

Parameter	Symbol	Min	Typ	Max	Unit
Operating Supply Voltage Tone Pulse	V_{DD}	 2.5 1.7		 6.0 6.0	V
Operating Supply Current Tone Pulse	I_{DD}			 1.0 200	 mA µA
Memory Retention Voltage	V_{stby}			1.5	V
Stand-by Current (V_{DD} = 2.5V)	I_{stby}		0.05	2.0	µA
Input Voltage 0 Level 1 Level	 V_{il} V_{ih}	 0 .8 V_{DD}		 .2 V_{DD} V_{DD}	V
Input Leakage Current HS, MU, PO	I_{lg}			1.0	µA
Output Current MU, FLD, PO, TO sink source	 I_{ol} $-I_{oh}$	 0.7 0.6			 mA mA
Flash Output Duration Flash Duration Extension Flash Hold-over time	T_{fg} T_{fext} T_{fhd}	80	90 300	100 30	ms ms ms
Keyboard Debounce Time	T_{db}		20		ms
Clock Start up Time	T_{stck}		4		ms
Row/Column Input Impedance To V_{DD} To V_{SS}	R_{in}		 100 k 5 k		 ohm ohm
HS Reset Delay Time		140	160		ms
Mute Output Overlap Time	T_{mh}		80	90	ms
Power-on Reset Delay MC145516 MC145516-1		100 220			ms

ELECTRICAL CHARACTERISTICS (continued)

TONE DIALING

Parameter	Symbol	Min	Typ	Max	Unit
Tone Output Level high group low group	 V_{toh} V_{tol}	 0.34 0.28	 0.40 0.32	 0.46 0.37	V_{rms}
Frequency deviation of Tones from nominal		-0.65		+0.65	%
Output Tone Leakage Rl = 600 Ω				-80	dBm
Output Impedance	Z_{to}		0.1	0.5	k ohm
Tone Output Distortion 300 - 4000 Hz Rl = 1k Ω	THD		-25	-25	dB
Tone output DC level	V_{tdc}	0.45 V_{DD}	0.50 V_{DD}	0.55 V_{DD}	V
Preemphasis High Group			2		dB
Tone Output Duration Manual Memory MC145516 Memory MC145516-1	T_{do}	 80 100 80			ms
Tone Output Interdigit Time MC145516 MC145516-1	T_{Id}	 100 80			ms

PULSE DIALING

Parameter	Symbol	Min	Typ	Max	Unit
Pulse Interdigit Time			820		ms
Make/Break Ratio			33/67		%
Start of Outpulsing Delay Time		240			ms

PAUSE TIMING

Parameter	Symbol	Min	Typ	Max	Unit
Pause Time			4		s

PIN DESCRIPTION

V_{DD} - POSITIVE POWER SUPPLY

Maximum 6V. Minimum 1.7V in Pulse mode and 2.5V in Tone and Mixed mode. The Power on Reset has highest reset priority, and resets without delay if the voltage drops below the Memory Retention voltage regardless of the state of the hook switch (HS) input.

V_{SS} - NEGATIVE POWER SUPPLY Connect to Ground

MS - MODE SELECT

Tristate input. logic 0 = pulse mode at 10 pps
logic 1 = tone mode
open = mixed mode

In mixed mode, after activation of the HS pin or Flash function key, the circuit is reset and stays in pulse mode until activation of the mode change key *. The mode then changes to DTMF dialing, but cannot be changed back again. The mode change function is inactive if the MS pin is set to logic 1 or 0.

C1-4/R1-5 - COLUMN ROW KEYBOARD INPUTS

Standard single or double contact keys can be connected. A logic 0 simultaneously present at a single Row and a single Column is defined as a valid key entry. When a valid key entry is detected, the debounce counter is enabled. Key entry is debounced on the leading edge for 12-20 ms and on the falling edge for an 8 ms hold-on time. During debounce hold-on time any other key depressions are ignored.

X1, X2 - CLOCK OSCILLATOR

On-chip oscillator connections for a low cost CTV crystal or resonator reference of 3.5795 MHz.

DTO - DTMF OUTPUT

DTMF tone output pin. 12 DTMF tones are available, and single tones are obtained by simultaneous depressions of two keys on the same row or colum. The tone output duration is as long as the key is active, or minimum 80 ms in manual dialing. In memory dialing, the tone output duration is 100 ms, with 100 ms interdigit time (80 ms/80 ms for France, MC145516-1)

PO - PULSE OUTPUT

Open Drain Output. Loop-Disconnect timing pulses appear at this pin after a valid key entry with a minimum delay of 240 ms. The Flash timing pulse is also output on this pin. The standard option is active high (i.e. output high at break).

MO - MUTE OUTPUT

Open Drain Output.

Mute is active high for the period of the pulse dialing string (including the interdigit time and break and make time) until the last digit is out. It is also active high for the Flash period with a flash hold over time of typ. 30 ms. During DTMF tone output, the mute is active high for the period of tone emission with a mute hold over time of typ. 80 ms.

HS - HOOK SWITCH

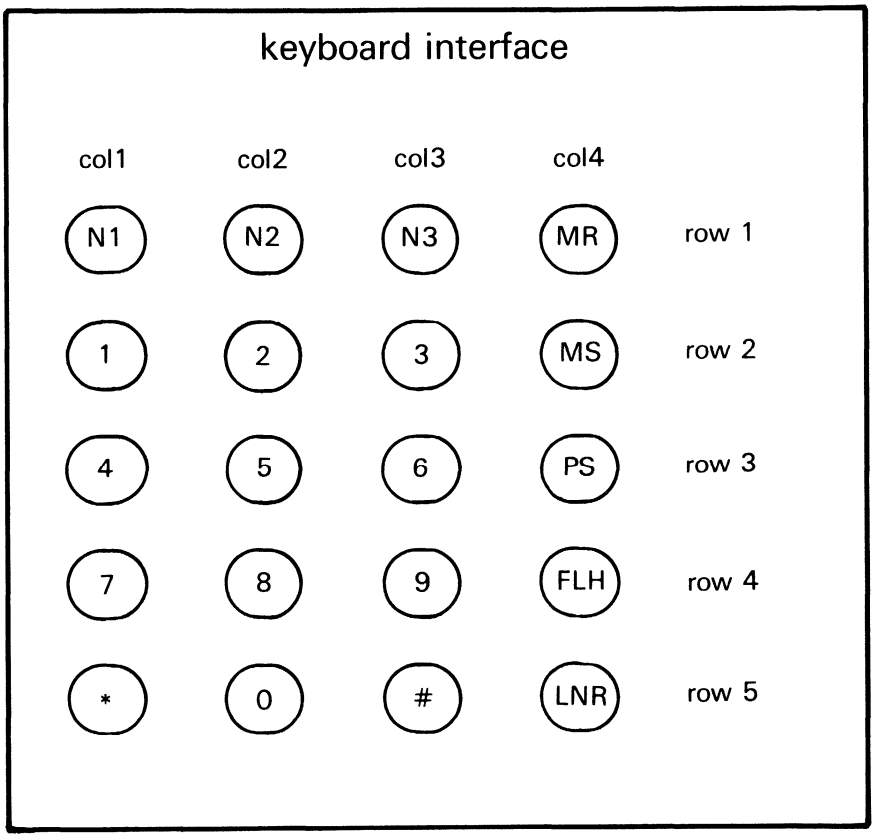
A low to high transition input on the HS pin activates the clock oscillator and initialises the chip for dialing. If HS goes low for more than the reset delay time of 160 ms (220 ms for MC145516-1), a reset pulse is generated at the end of the reset delay period to reset the circuit to the standby mode. In the standby mode the keyboard is inhibited but the memory contents are preserved as long as V_{DD} is higher than the memory retention voltage. In standby mode the current consumption is typically much below one microampere.

FLD - FLASH DURATION CONTROL

This is used for control of the Flash or Timed Break Recall duration. If the FLD pin is left unconnected, the Flash duration is 90 ms, timed by the circuit internally. This duration can be extended to a maximum of 300 ms by connecting an RC to FLD. The extended duration is equal to R x C.

TS - TEST MODE

This pin is used for factory testing of the device, and should be left unconnected for normal and standby operation.



KEYBOARD

FLH	FLASH
FS	PAUSE
MS	MEMORY STORE
MR	MEMORY RECALL
LNR	LAST NUMBER REDIAL
*	PULSE TO TONE MODE KEY and respective DTMF tones (see note on different versions)
N1, N2, N3	ABBREVIATED RECALL

OPERATION

(Keyboard entries shown in **bold** type)

A MANUAL DIALING, MS PIN SET AT ANY MODE
PUBLIC EXCHANGE CONNECTION - OFF HOOK

D1, ... DN

A1) e.g. 816702
Contents of LNR prefix register 8167
Contents of LNR main register: 816702

PABX CONNECTION - OFF HOOK
D1, . . . Dn wait for access pause **D1, . . . DN**
A2) e.g. 9 - 816702
Contents of LNR prefix register: 9816
Contents of LNR main register: 9816702
ON HOOK - OFF HOOK
P1, . . . P4
A3) e.g. 2156 internal call
Contents of LNR prefix register: 2156
Contents of LNR main register: 9816702

A maximum of 4 digits prefix entry to access the line prior to external dialing is possible. An internal extension call of not more than 4 digits will not affect the previous external call number stored in the main register.

The first four digits are stored in the LNR prefix register. On the 5th digit entry an overflow condition occurs and the first four digits are copied into the least significant digits of the main register and all following digits will be stored in the main register. If a total of more than 22 digits is entered, Redial (LNR) will be inhibited.

USE OF * AND #
When in DTMF mode, depression of the # or * key produces the corresponding output tones, but these and subsequent key entries are not dialed in LNR in any of the dialing modes provided more than 4 digits were dialed before depressing # or *. (They can be stored for Memory Redial - see below).

In pulse mode, pressing of # or * produces no signal output and the key entry is ignored. Use of * does not change the dial mode if pin MS is connected logic high or low.

B LNR - MODE (MS) PIN SET TO ANY OF THE THREE MODES
PUBLIC EXCHANGE CONNECTION - OFF HOOK

LNR

e.g. following example A1) above: 816702 is dialed
PABX CONNECTION - OFF HOOK

LNR

e.g. following example A3) above: 2156 is dialed.
PABX CONNECTION - OFF HOOK
P1, . . . P4 wait for access tone **LNR**
A4) e.g. following example A3) above: **9** - 816702 is dialed.

If LNR is the first key entry after an on- to off-hook transition, redial starts from the prefix register. A moving cursor advances to the next digit upon completion of output. If the number of previously entered digits between an on-hook/off-hook transition was 4 or less, overflow was not set, and the moving cursor will not move on to the main register. Only the contents of the prefix register will be redialed. Otherwise the moving cursor will move on continuously to the 5th position of the main register and continue on to dial out the remainder of the digits in the main LNR register.

If a dialing sequence of n digits is entered after going off-hook, followed by LNR, the moving cursor starts at the (n + 1)th position in the main register and dials out the remaining digits. If n was 4 or less and the digits entered were different from those stored previously in the corresponding positions, the new digits overwrite the previous ones in the prefix register and the redial starts as before at the next position. If n was greater than 4, LNR will be ignored. After redial of an external number in the main register, any internal number in the prefix register will be cleared.

C MIXED MODE DIALING.
MS PIN NOT CONNECTED

D1, . . . Dn * D, . . . DN

Digits D1 to Dn will dial out in pulse mode, digits D to DN in tone mode. * produce no signalling output in MC145516. If however * is keyed in a second time it is transmitted normally in the DTMF part of the number. The -1 option (France) does however produce the MF tones upon first entry of *.

In mixed mode dialing, on the first pulse dial part of the number will be redialed after entering LNR, unless the * key is entered before LNR, in which case the DTMF digits will be dialed on depressing LNR.

e.g.
i) manual dial **956457*123**
on-hook/off-hook **LNR**
956457 (pulse) is dialed

ii) manual dial **915432#31*2**
191543231 (pulse) is dialed and 2 in dtmf. The # is ignored in the pulse part of the number.

on-hook/off-hook **LNR**
91543231 (pulse) is dialed. The * and following 2 in dtmf are inhibited in redial.

D USE OF PAUSE (PS)
Pause is normally stored in memory recall dialing where for example a PBX access pause is required. Pause can also be keyed in manual dialing as if it were a digit in any position if desired, creating a pause at that position during LNR. It produces a pause of 4 seconds. PS is stored as one digit in memory. Multiple PS entries can be cascaded to produce a total pause length of a multiple of 4 seconds.

During the time pause is active, in LNR or in memory dialing, it can be interrupted to resume dialing by depressing any key.

E MEMORY STORE

A typical sequence to store a number in memory is:

MS, A D1, . . . DN

Where A is the address of the storage location, and D1 to DN are valid key entries including digits, PS, # and *. Address A is any single digit 1 - 9, N1, N2 or N3. Memory storage is possible in the off-hook (HS high) state only, and to avoid drawing current in the on-hook state the keyboard is inhibited when HS is low. After pressing the MS key, the signal output is inhibited, and the first numeric key (except 0) or N1, N2, N3, which follows is treated as the memory address and subsequent digits as data. A total of 18 digits can be stored. If the first key entry after MS is not a valid address, it will be ignored until the next entry of a valid address key, i.e. 1 - 9, N1, N3, N3. Memory storage can be entered during conversation, enabling the use of memory as a NOTEPAD facility.

F MEMORY REDIAL

PUBLIC EXCHANGE, ANY DIALING MODE - OFF HOOK

A typical sequence using memory redial is:

MR A

where A is any valid address, i.e. 1 - 9,
or using abbreviated redial:

N1 or **N2** or **N3**

Mixed dialing in memory is only possible if the mode select pin MS is set to mixed dialing.

PABX CONNECTION

Memory recall can be cascaded with the prefix digits in a PABX connection e.g.:

P1, . . . P4 wait **MR A** or **N1** or **N2** or **N3**

If the first key entry after MR is not a valid address, it will be ignored until the next entry of a valid address key, i.e. 1 - 9. Digits entered after a valid address will be dialed in cascade after emission of the number in memory. If the storage address contains no stored number, no signalling is output and the device reverts to conversation mode.

G CASCADED MEMORY REDIAL

Memory redial can be cascaded with LNR, other memories and manual dialing. All of the following sequences are valid:

LNR MR A,
MR A1 MR A2,
MR A1 D1, . . . D2,
P1, . . . P4 wait **MR A1 MR A2.**

During dialing out all key entry is inhibited, so that the second function key must be entered after completion of the previous number.

H FLASH

Flash provides a timed break recall, generating a pulse of fixed duration at the PO output. The moving cursor is reset and if the number of subsequently dialed digits is a maximum of 4, they are stored in the LNR prefix register and can be used for convenient internal call transfer. The Flash output is only generated when the chip is in the DTMF dialing state, and inhibited in the pulse state. (MC145516-1 allows Flash in pulse and DTMF dialing). During the flash pulse, the Reset Delay counter is inhibited.

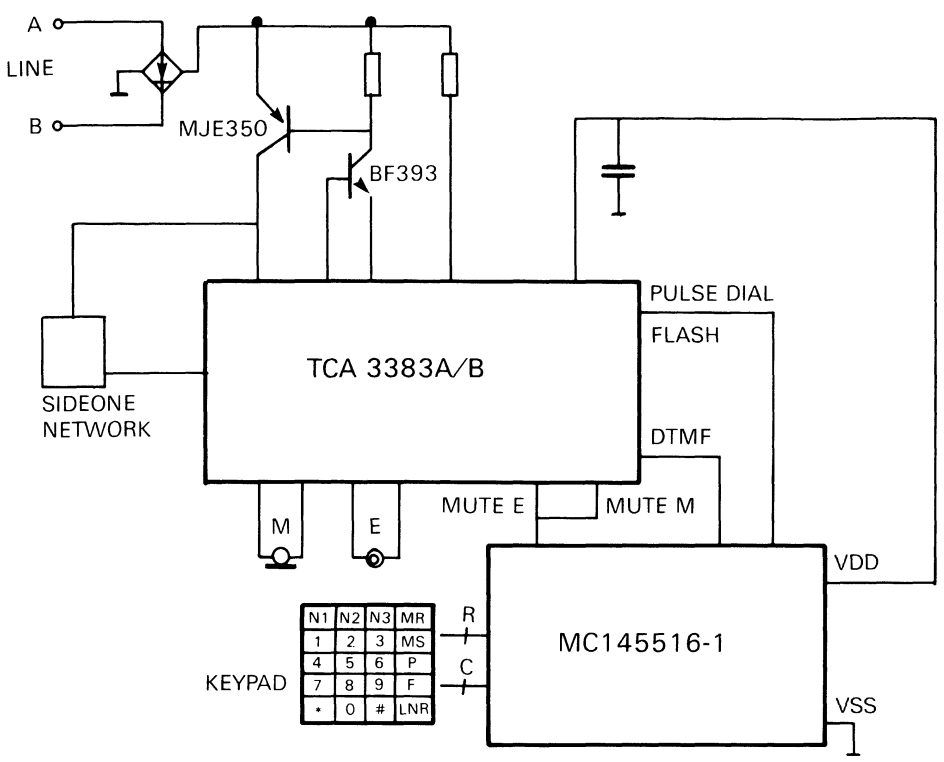
3

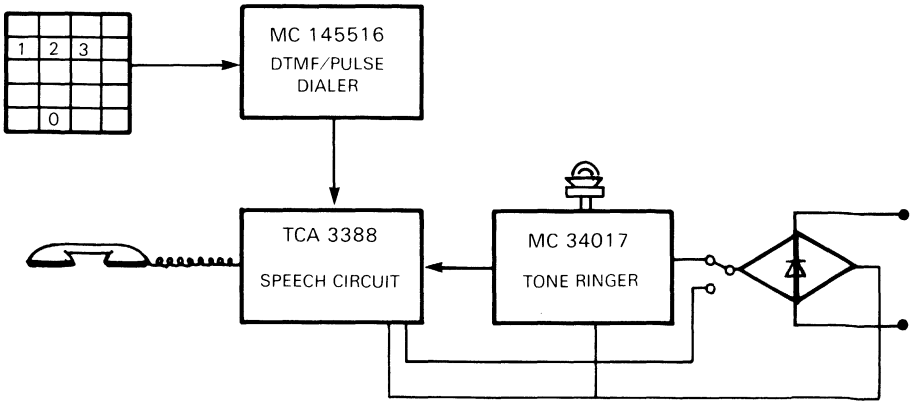
MC145516 OPTIONS

MC145516-1	FRENCH REQUIREMENTS	
	Power Up Reset Delay	220 ms
	DTMF Duration	80 ms
	DTMF Interdigit Time	80 ms
	FLASH in all dialing modes	
	In mixed mode, entry of * emits corresponding tones and switches signalling from pulse to DTMF simultaneously.	
ON REQUEST	Pulse output PO active low	

APPLICATION EXAMPLES

APPLICATION - TELEPHONE SET TO FRENCH REQUIREMENTS





LOW END TELEPHONE SET

MOTOROLA

MC145532

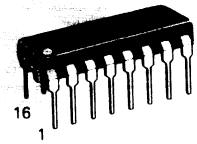
Product Preview

ADPCM TRANSCODER

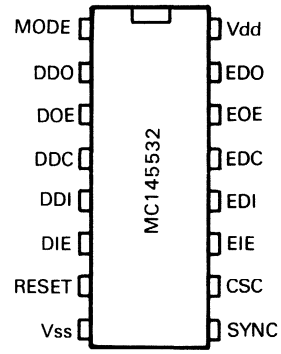
ADPCM TRANSCODER

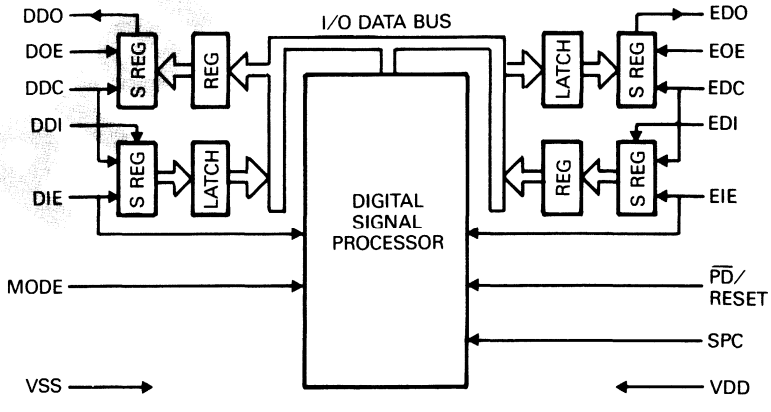
The MC145532 Adaptive Differential Pulse Code Modulation (ADPCM) Transcoder provides a low cost full duplex single channel transcoder to (from) a 64 kbps PCM channel from (to) either a 16 kbps, 24 kbps, 32 kbps, or 64 kbps channel.

- Complies with CCITT Recommendation G.721 (Geneva 1986)
- Complies with the American National Standard (T1.301-1987)
- Full Duplex Single channel operation
- μ-Law or A-Law coding is pin selectable
- Synchronous or Asynchronous Operation
- Easily interfaces with any member of Motorla's PCM CODEC/Filter Mono-Circuit Family or other Industry Standard CODECs
- Serial PCM and ADPCM data transfer rate from 64 kbps to 4.1 Mbps
- Power Down Capability for low current consumption
- The Reset State, an option specified in the standards, is automatically initiated on Power Up
- CMOS Input/Output Compatable
- Single 5 Volt Power Supply
- 16 Pin Package



CASE 648
PLASTIC





This document contains information on a new product. Specifications and information herein are subject to change without notice.

MOTOROLA

MC145601

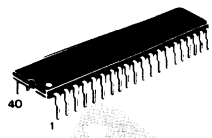
Product Preview

TIME SLOT INTERCHANGE CIRCUIT

SILICON - GATE CMOS

The MC145601 Time Slot Interchange Circuit (TSIC) is a CMOS IC specially designed for switching Pulse Code Modulation (PCM) voice or data, under microprocessor control, in a digital exchange or central office. It connects any 256 incoming PCM channels to any 256 outgoing PCM channels.

- 5 Volt supply.
- 8 x 32 channel input.
- 8 x 32 channel output.
- 256 ports non-blocking digital switching matrix.
- building block for digital PABX.
- expandable to larger capacity block.
- 32 serial channels per frame.
- typical bit rate: 2.048 Mbit/s.
- typical synchronization rate: 8 KHz.
- interface to MC68XXX family microprocessors.
- 8 instructions available.
- 40 pin dual in line package.



P SUFFIX
PLASTIC PACKAGE
CASE 711-03

PIN ASSIGNMENT

OC4	1	40	RESET
OC3	2	39	CLOCK
OC2	3	38	SYNC
OC1	4	37	TX7
OC0	5	36	TX6
RX7	6	35	TX5
RX6	7	34	TX4
RX5	8	33	VDD
RX4	9	32	TX3
VSS	10	31	TX2
RX3	11	30	TX1
RX2	12	29	TX0
RX1	13	28	D7
RX0	14	27	D6
READY	15	26	D5
DTACK	16	25	D4
RS1	17	24	D3
RS0	18	23	D2
R/W	19	22	D1
CS	20	21	D0

This document contains information on a new product. Specification and information herein are subject to change without notice.

MOTOROLA

MC145611

Product Preview

PCM CONFERENCE CIRCUIT

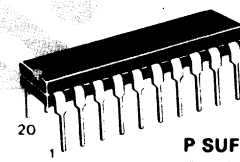
The PCM conference circuit MC145611 is a CMOS device designed for voice conference in a digital (PCM) telephone switch such as a TDM PABX. The device is capable of providing mixing of up to 8 channels (parties) such that every party can hear when one, or more parties speak at the same time.

The technique of level priority coding is used. It provides a low cost means of mixing of PCM voice codes for voice conference application.

Features:

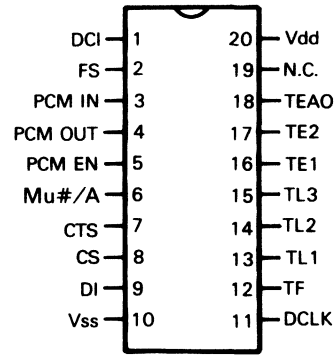
- 20 pins DIL package.
- Single +5V power supply.
- Support standard Mu-law or A-law PCM codes.
- Directly off the PCM highways.
- 4.096 MHz clock, 8 KHz frame sync and serial PCM data comply with codec timing used in the PABX system.
- One-frame delay to PCM data.
- Built-in time slot assignment circuit.
- Serial data with MCU interface.
- 8 parties conference in single group or split into two groups.
- Intrusion party channel time slot assignment provided.
- Built-in maskable tone signalling. Tone level and frequency external adjustable.

HCMOS
PCM CONFERENCE CIRCUIT



P SUFFIX
PLASTIC
CASE 738

PIN ASSIGNMENT



MOTOROLA

TCA 3381

TELEPHONE RING SIGNAL IMPEDANCE MATCHING AND PROTECTION CIRCUIT

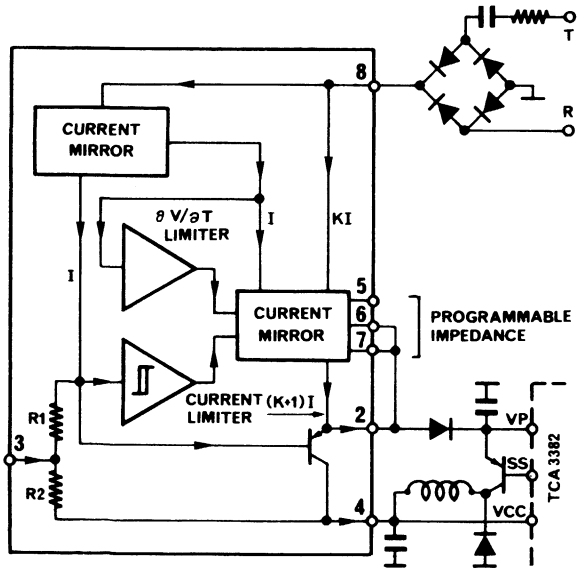
The TCA 3381 Ring Signal Impedance Matching and Protection Circuit is designed for use with the companion TCA 3383A/B Transmission Circuit, and TCA 3382 Telephone Set Speaker Amplifier Circuit. These devices, together with a microcomputer unit form the basis of a fully electronic telephone set. With the telephone on-hook, the TCA 3381 is connected to the line and converts the ring voltage into a current which feeds the TCA 3382. The conversion voltage/current is necessary to decrease the harmonic distortion of the ring signal.

The input impedance of the circuit is programmable so that it can be matched by the designer to the line impedance in order to maximize the available energy in the case of a long line. Five programmed impedance values can be pin-selected, other values by adding external resistors.

The inputs include circuitry to protect the device against overvoltage surges due to lightning and accidental connection to the mains.

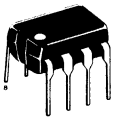
- Line impedance matching, programmable
- Lightning and mains protection
- Voltage/current conversion
- Breakdown voltage 150V

FIGURE 1 – TCA 3381 REPRESENTATIVE CIRCUIT SCHEMATIC



TELEPHONE RING SIGNAL IMPEDANCE MATCHING AND PROTECTION CIRCUIT

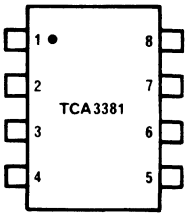
BIPOLAR INTEGRATED CIRCUIT



8 PIN DIL PACKAGE
CASE 626

ORDERING INFORMATION
TCA 3381-DP

Pin Connections



1 – Must not be connected
2 – Z_{output}
3 – Threshold selection
4 – V_{CC}
5 – Z_{adjust}
6 – Z_{adjust}
7 – Z_{adjust}
8 – V_{line}

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Value	Unit
Line Voltage	V_L	150	V
Operating Ambient Temperature	T_A	– 20 to 60	°C
Storage Temperature	T_{stg}	–65 to 150	°C
Operating Junction Temperature	T_J	150	°C
Thermal Resistance Plastique Package	R_t	65 to 95	°C/W

ELECTRICAL CHARACTERISTICS

Characteristic (T_A = 25°C)	Figure	Symbol	Min	Typ	Max	Unit
Input Impedance (T_A = – 20 to + 60)	2	Z_L	50 · R_{ext}	65 · R_{ext}	75 · R_{ext}	Ω
$Z_L = \frac{\Delta V_L}{\Delta I_L}$ = impedance	3	Z_L	4.2	4.9	6.2	KΩ
between pin 8 and 4	4	Z_L	4.4	5.2	6.6	KΩ
(Slope between 20 and 80 V)	5	Z_L	5.5	6.5	8.3	KΩ
	6	Z_L	6.6	7.8	10.5	KΩ
	7	Z_L	7.1	8.3	11.0	KΩ
I_L (V_L) Characteristics	9					
Threshold up	10	V_{LU}	110		130	V
Threshold down	10	V_{LD}	90		120	V
Hysteresis	10	V_L	5		30	V
Inhibited current	10	I_{LI}	–		5	mA
Breakdown (I pin8 = 10 mA)	10	V_{BK}	150		–	V
Distortion						
Level of each harmonic	11	L_H	–	–14	0	dBm

FIGURE 2 – INPUT IMPEDANCE

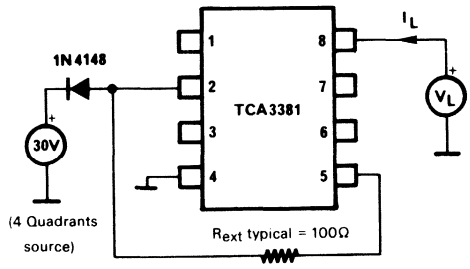


FIGURE 3 – INPUT IMPEDANCE

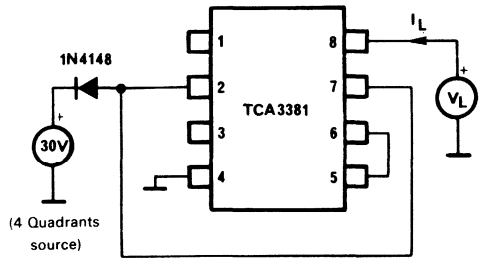


FIGURE 4 – INPUT IMPEDANCE

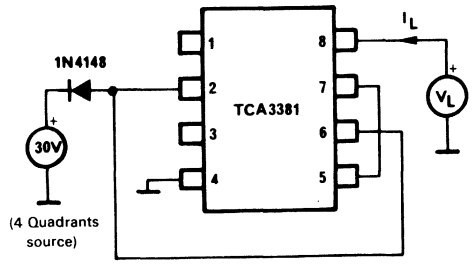


FIGURE 5 – INPUT IMPEDANCE

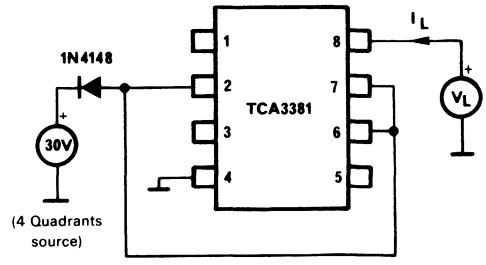


FIGURE 6 – INPUT IMPEDANCE

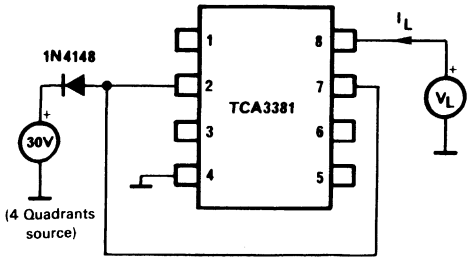
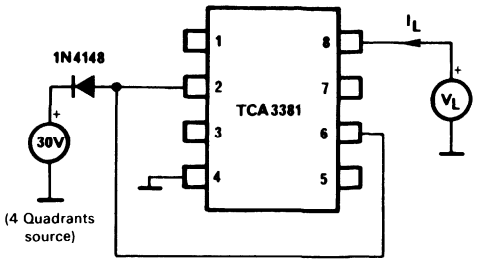


FIGURE 7 – INPUT IMPEDANCE



3

FIGURE 8 – CHOICE OF Z_L

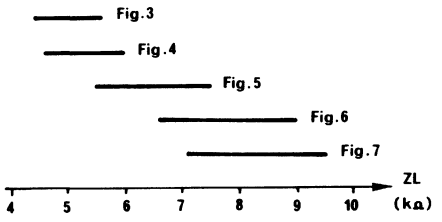


FIGURE 9 – CURRENT/VOLTAGE CHARACTERISTIC MEASUREMENT SET-UP

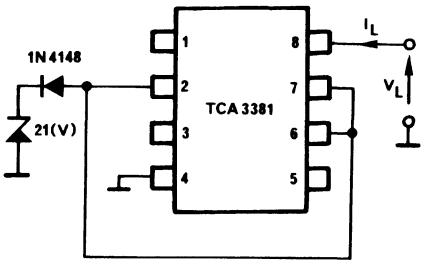
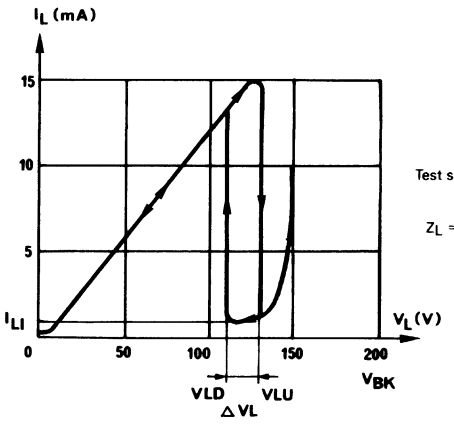


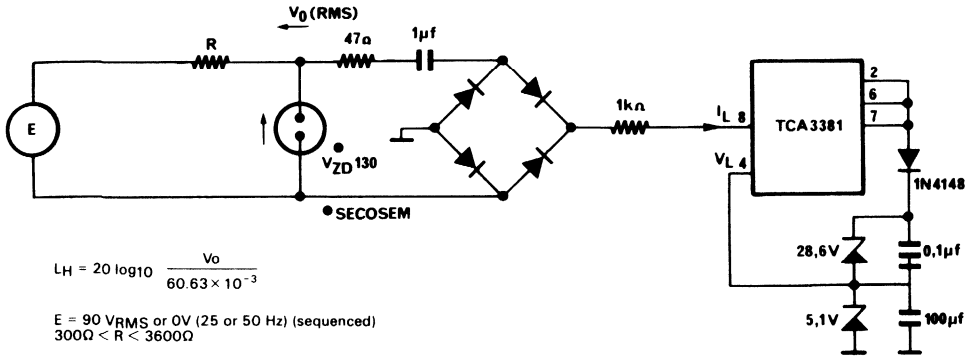
FIGURE 10 – CURRENT/VOLTAGE CHARACTERISTICS



Test set-up like fig. 9

$$Z_L = \frac{\Delta V_L}{\Delta I_L} = \frac{80\text{-}20}{(10.4\text{-}2)\cdot 10^{-3}} = 7143\ \Omega$$

FIGURE 11 – RINGING DISTORTION TEST SET-UP



$$L_H = 20 \log_{10} \frac{Vo}{60.63 \times 10^{-3}}$$

E = 90 V_{RMS} or 0V (25 or 50 Hz) (sequenced)
300Ω < R < 3600Ω

FIGURE 12 – LIGHTNING PROTECTION MEASUREMENT
as described in TMA/PRL/192 recommendation edited by the CNET-France

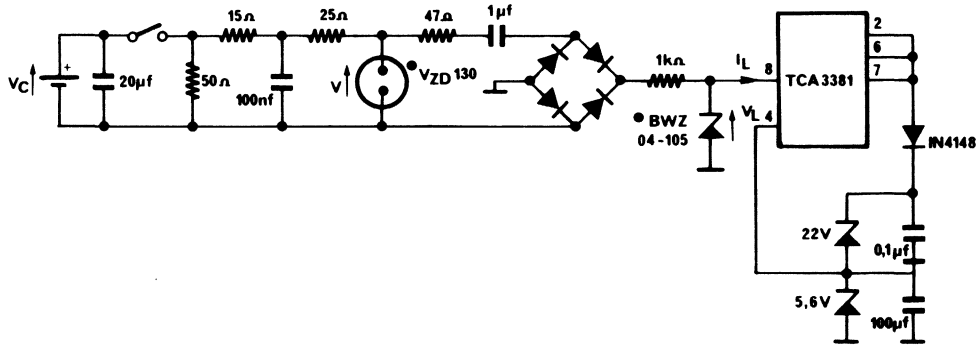


FIGURE 13 – SHAPE OF THE SURGE APPLIED ON THE SPARK-GAP (Fig. 14)

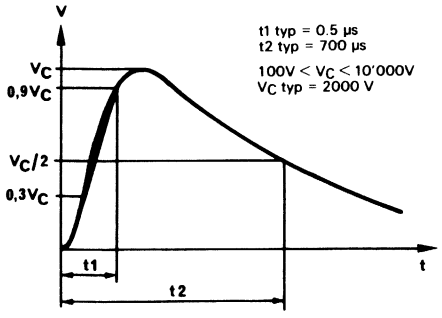
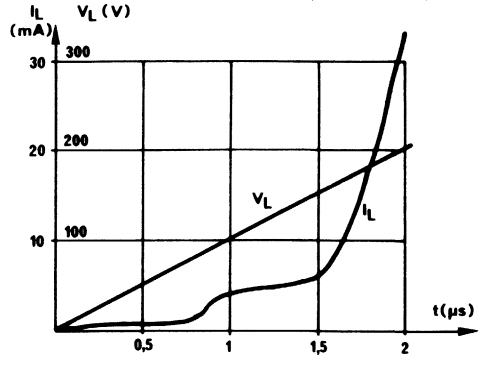


FIGURE 14 – TYPICAL PERFORMANCE UNDER LIGHTNING TEST CONDITIONS (Computer simulation)



MOTOROLA

TCA 3382
TCA 3382A
TCA 3382B

3

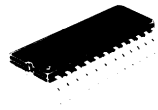
TELEPHONE SET RING DETECTION AND LOUDSPEAKER AMPLIFIER CIRCUIT

The TCA 3382 Telephone Set Speaker Amplifier I.C. is designed for use with the companion TCA 3383 Transmission Circuit, and TCA 3381. These devices together with a microcomputer form the basis of a fully electronic telephone set. With the telephone on-hook, the TCA 3382 detects the presence of a call signal on the line and energy is derived from this signal to power up the system so that a ring melody generated by the microcomputer is heard at the loudspeaker. With the telephone off-hook, the received speech signal is heard at the loudspeaker. Sidetone and line length compensation of the speaker amplifier gain are provided by the TCA 3383.

- Power derived from Ring Signal
- Reset/$\overline{\text{Reset}}$ and $\overline{\text{Ring}}$ outputs for microcomputer
- Amplifier gain controlled by microcomputer
- Guaranteed ring signal detection limits
- On-chip protection against microphone/loudspeaker howl ("Antilarsen")
- TCA 3382 B: Input Voltage of Switching Power Supply (Ring Mode) lower
- TCA 3382 A: Like TCA 3382 B but external feedback for loudspeaker amplifier gain.

TELEPHONE SET RING DETECTION AND LOUDSPEAKER AMPLIFIER CIRCUIT

BIPOLAR INTEGRATED CIRCUIT

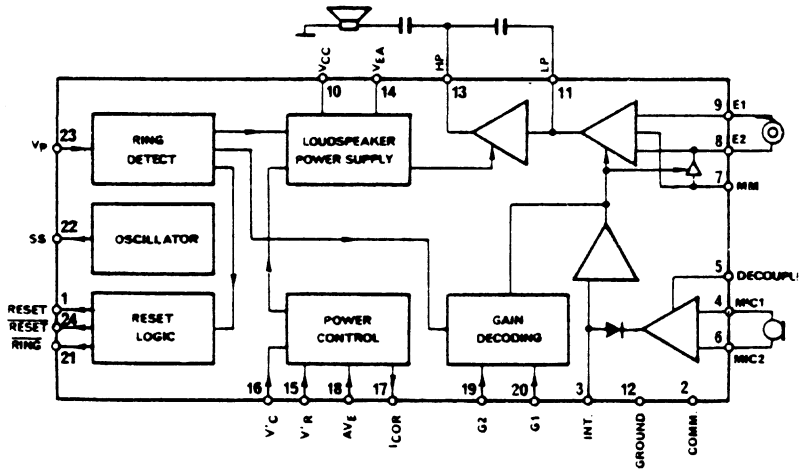


24 PIN DIL PACKAGE

ORDERING INFORMATION:

TCA 3382-DP
TCA 3382A-DP
TCA 3382B-DP

TCA 3382 BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Speech Mode						
1) Inhibited Circuit						
(G1 = G2 = 0; pulled to V_{COMM})						
V_C = 14 V						
V_{CC} Consumption I_{CC}	1	I_{CCOO}	–	300	700	µA
Line Current I_{EA}	1	I_{EAOO}	–	5	100	µA
2) Working Circuit						
($G_1 \neq 0$; $G_2 \neq 0$; G_1 and/or						
G_2 pushed to V_{CC})						
V_{CC} Consumption ($G_1 = G_2 = 1$)	1	I_{CC11}	–	600	800	µA
V_{CC} Consumption ($G_1 = 0$; $G_2 = 1$)	1	I_{CC01}	–	1.1	1.6	mA
a) A_{VE} = 2 V						
Line Current (I_{EA})	1	I_{EA2}	–	100	500	µA
Line Current Correction (I_{COR})	1	I_{COR2}	–	0.5	1	µA
b) A_{VE} = 2.9 V						
Line Current (I_{EA})	1	I_{EA29}	5.5	7	9.5	mA
Correction Ratio: k = I_{EA}/I_{COR}	1	k_{29}	530	550	600	None
Amplifier Power Supply (V_{EA})	1	V_{EA29}	V_{CC}–1	V_{CC}–0.6	V_{CC}	
c) A_{VE} = 3.25 V						
Line Current (I_{EA})	1	I_{EA325}	7	10	14	mA
Correction Ratio: K = I_{EA}/I_{COR}	1	K_{325}	530	550	610	None
Amplifier Power Supply (V_{EA})	1	V_{EA325}	V_{CC}–1	V_{CC}–06	V_{CC}	
d) A_{VE} = 3.55 V						
Line Current ($\overline{I_{EA}}$)	1	I_{EA355}	10	12	17	mA
Correction Ratio: k = I_{EA}/I_{COR}	1	K_{335}	530	560	610	None
Amplifier Power Supply (V_{EA})	1	V_{EA355}	V_{CC}–1	V_{CC}–0.6	V_{CC}	
e) A_{VE} = 6.0 V						
Line Current (I_{EA})	1	I_{EA6}	11	14	18	mA
Correction Ratio: k = I_{EA}/I_{COR}	1	K6	530	570	620	None
Amplifier Power Supply (V_{EA})	1	V_{EA6}	6.5	7.5	8.5	V
3) Any G_1, G_2						
Reference Voltage Input Bias	1	$I_{V'R}$	–	15	200	nA
Line Length Sense Input Bias	1	I_{AVE}	–	10	200	nA
Earphone Input Bias E_1	1	I_{E1}	–	10	50	µA
Earphone Input Bias E_2	1	I_{E2}	–	10	50	µA
Microphone Input Bias	1	I_M	–	0.05	1	µA
4) Gain Control						
Logical "0" Level (G_1 or G_2)		V_{G0}	V_{COM}	–	V_{com} +0.4	V
Logical "1" Level (G_1 or G_2)		V_{G1}	V_{CC}–1	–	V_{CC}	V
Bias Current at Logical "0" (G_1 or G_2)		$\|I_{G0}\|$	–	1	10	µA
Bias Current at Logical "1" (G_1 or G_2)		$\|I_{G1}\|$	–	35	100	µA
5) Ringing Information Off						
V_{RING}	1	V_{RGS}	V_{CC}–0.4	V_{CC}–0.1	V_{CC}	V
6) Amplified Speech Gains						
$G_1 = G_2$ = "1"						
•TCA 3382 – TCA 3382 B	2	G_{AS11}	18	20	22	dB
•TCA 3382 A	2	G_{AS11}	23	27	31	dB
a) Gain Variation (Ref. $G_1 = G_2 = 1$)						
G_1 = "1"; G_2 = "0"	2	ΔG_{AS10}	5	7	9	dB
G_1 = "0"; G_2 = "1"	2	ΔG_{AS01}	13	15	17	dB
b) Inhibited Amplified Speech						
G_1 = "0"; G_2 = "0"						
•TCA 3382 – TCA 3382 B	2	G_{AS00}	–	–30	–20	dB
•TCA 3382 A	2	G_{AS00}	–	–25	–15	dB
7) Max. Power on Loudspeaker						
$G_1 = G_2$ = "1"; Distortion < 3%	2	P_L	500	600	–	mV_{RMS}

ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C unless otherwise noted)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Speech Mode						
8) "Larsen" Effect Cancellation						
a) $V_{M2} \leq$ 0.1 mV Peak						
•TCA 3382 – TCA 3382 B	3	G_{AS11A0}	18	20	22	dB
•TCA 3382 A	3	G_{AS11A0}	23	27	31	dB
b) $V_{M2} \geq$ 0.8 mV Peak						
•TCA 3382 – TCA 3382 B	3	G_{AS11A1}	–	–4	0	dB
•TCA 3382 A	3	G_{AS11A1}	–	3	8	dB
9) Amplified Melody/Supervision						
a) $G_1 = G_2$ = "1"						
Gain to Loudspeaker						
•TCA 3382 – TCA 3382 B	4	G_{AM11}	4	7	10	dB
•TCA 3382 A	4	G_{AM11}	9	14	19	dB
Gain to Earphone						
•TCA 3382 – TCA 3382 B	4	G_{AME11}	–	–60	–30	dB
•TCA 3382 A	4	G_{AME11}	–	–55	–25	dB
b) $G_1 = G_2$ = "0" (Long Test)						
Gain to Loudspeaker						
•TCA 3382 – TCA 3382 B	4	G_{AM00}	4	7	10	dB
•TCA 3382 A	4	G_{AM00}	9	14	19	dB
Gain to Earphone						
•TCA 3382 – TCA 3382 B	4	G_{AME00}	–23	–17	–11	dB
•TCA 3382 A	4	G_{AME00}	–23	–17	–11	dB
c) Gain Variation (Loudspeaker)						
Reference $G_1 = G_2$ = "1"						
G_1 = "1"; G_2 = "0"	4	ΔG_{AM10}	1	4	7	dB
G_1 = "0"; G_2 = "1"	4	ΔG_{AM01}	8	11	15	dB
Microprocessor Protection						
Limitation of $V_{CC} - V_{COM}$	5	V_{ALM}	5.2	5.6	6	V
Start-Up Information						
1) $V_{CC} - V_{COM}$ = 3.2 V						
V_{RESET}	6	V_{RST1}	V_{CC}–0.4	–	V_{CC}	V
$V_{\overline{RESET}}$	6	V_{RSTNO}	V_{COM}	–	V_{COM}+0.4	V
$V_{\overline{RING}}$	6	V_{RGL32}	V_{CC}–0.4	–	V_{CC}	V
2) $V_{CC} - V_{COM}$ = 3.7 V						
V_{RESET}	7	V_{RST0}	V_{COM}	–	V_{COM}+0.4	V
$V_{\overline{RESET}}$	7	V_{RSTN1}	V_{CC}–0.4	–	V_{CC}	V
$V_{\overline{RING}}$	7	V_{RGL37}	V_{CC}–0.4	–	V_{CC}	V
Ringing						
1) Ringing Information						
a) I = 2.8 mA; $V_{\overline{RING}}$	8	V_{RG1}	V_{CC}–04	–	V_{CC}	V
b) I = 8.5 mA; $V_{\overline{RING}}$	8	V_{RG0}	V_{COM}	–	V_{COM}+0.4	V
2) Max. Loudspeaker Power						
I = 14 mA; V_{MM} = 1 kHz Large Square Waves Signal						
V_{HP} peak to peak						
•TCA 3382	8	P_{LR}	2.8	3	–	V
•TCA 3382 A – TCA 3382 B	8	P_{LR}	2.4	2.7	–	V
3) Amplified Melody (I = 8.5 mA)						
a) $G_1 = G_2$ = "1"; Gain to Loudspeaker						
•TCA 3382 – TCA 3382 B	8	G_{AMR11}	3	6	9	dB
•TCA 3382 A	8	G_{ARM11}	9	13	17	dB
b) Variations to Loudspeaker						
Reference G_1 = 1; G_2 = 1						
G_1 = "1"; G_2 = "0"	8	ΔG_{AMR10}	8	11	14	dB
G_1 = "0"; G_2 = "1"	8	ΔG_{AMR01}	20	24	28	dB
4) Input Switching Power Supply						
I = 8.5 mA; V_p						
•TCA 3382	8	V_p	26	28.5	31	V
•TCA 3382 A – TCA 3382 B	8	V_p	19	22	25	V
5) Correction Saturation						
I = 8.5 mA; V_{ICOR}	8	V_{ICOR}	0	–	0.8	V

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Operating Ambient Temperature	T_A	− 20 to + 60	°C
Storage Temperature	T_S	-65 to +150	°C
Operating Junction Temperature	T_J	150	°C
Thermal Resistance(Plastique Package)	R_θ	70 to 95	°C/W

CIRCUIT DESCRIPTION

On-hook mode

In this mode, the functions realized by the TCA 3382 are:

- Threshold detection of a ring signal current, normally provided by the TCA 3381, establishing the power for the microcomputer via the TCA 3383 power supply output.
- Logic signals $\overline{RING}$, RESET and $\overline{RESET}$ for the microcomputer.
- Amplification to the loudspeaker of a ring melody signal (square waves) generated by the microcomputer.
- Control of amplifier gain by two bits from microcomputer.

In this mode of operation, the current consumption of the TCA 3383 is limited to 600 µA typically in order to allow the maximum of power to drive the loudspeaker.

The ring melody applied on pin 7 is active when the signal reaches 1.5 V above COMM (pin 2). Above this level an audio signal on this pin is transmitted analogically to the HP output (loudspeaker) and to the earphone. Below this level the HP output maintains a steady DC level equal to $V_{CC}/2$ ($V_{EA}/2$ in Off-Hook mode).

Off-hook mode

In this mode, the 3382 is powered by the TCA 3383 and provides a voice signal amplification. The voice signal inputs (pin 8,9) are directly connected to the earphone output pin 4 and 5 of the TCA 3383.

The mean current of the output amplifier (pin 13) is controlled as a function of the line length by the TCA 3383 and, due to I_{COR} (pin 17) the total current consumption of the system respects the same limits of line current/voltage characteristic as the TCA 3383 transmission circuit alone (see TCA 3383 data sheet, fig. 8). The gain of the speaker amplifier can be set by two logic inputs G_1, G_2 (pin 20,19). If $G_1 = G_2 = 0$, the speaker amplifier is turned off.

The power delivered to the loudspeaker is a function of the line length and the loudspeaker impedance (50 Ω recommended). A system (Antilarsen) minimizes the howling caused by mic./speaker coupling.

TCA 3382 PIN DESCRIPTION

V_{CC} : Positive power supply, voltage controlled externally e.g. by TCA 3383 (pin 28). Amplifier power supply in ring mode.

GROUND : Most negative voltage of line bridge.

COMM : Digital ground. Regulated 4V supply is provided between V_{CC} and V_{COMM} by TCA 3383 in Off-Hook mode.

V_p : Ring signal sense input (Switching power supply input).

SS : Switched supply. A square wave signal (50 kHz typically) appears between V_p and SS for switch-mode power supply to external PNP transistor.

V_{EA} : Amplifier power supply in amplifier speech mode, derived from V'c.
Must be decoupled by a grounded capacitor.

V'c : Unregulated supply from pin 15 of TCA 3383.

AVE : Part of DC line voltage needed for loudspeaker amplifier peak current limiting as function of line length. Must be connected to pin 17 of TCA 3383.

V'R : Input: 2.4 V provided by TCA 3383 as a reference for current limiting as function of line length, connected to pin 25 of TCA 3383.

I_{COR} : DC current feedback to pin 13 of TCA 3383 providing a compensation to retain same line current/voltage characteristic when TCA 3382 is connected.

DECOUPLE : Decoupling capacitor to COMM for sidetone cancellation by howling effect.

INT. : Connection for integrator capacitor for microphone sidetone reduction and minimisation of howling caused by mic./speaker coupling.

MM : External ring melody inputs.

HP : Loudspeaker output. Typically loaded by 50 Ω.

LP : Connection for external feedback between LP and HP (TCA 3382 only). This feedback is internal (typ. 220K) in TCA 3382 and TCA 3382 B.

MIC1, MIC2 : Microphone inputs for howling effect sensing.

E1, E2 : Earphone inputs for amplified speech.

G1, G2 : Logic inputs for gain control of loudspeaker amplifier.

RESET, $\overline{RESET}$: Push-Pull outputs saturated to V_{CC} or V_{COMM} logic signals for microcomputer initialisation or re-initialisation.
RESET follows V_{CC} if ($V_{CC} - V_{COMM} < 3.4$ V (typ.)
RESET = V_{COMM} for ($V_{CC} - V_{COMM} > 3.4$ V (typ.)
$\overline{RESET} = V_{COMM}$ for ($V_{CC} - V_{COMM} < 3.4$ V (typ.)
$\overline{RESET}$ follows V_{CC} if ($V_{CC} - V_{COMM} > 3.4$ V (typ.)

$\overline{RING}$: Open collector output saturated to V_{COMM} during ring signal. MUST be pulled up.

BASIC TEST CIRCUIT

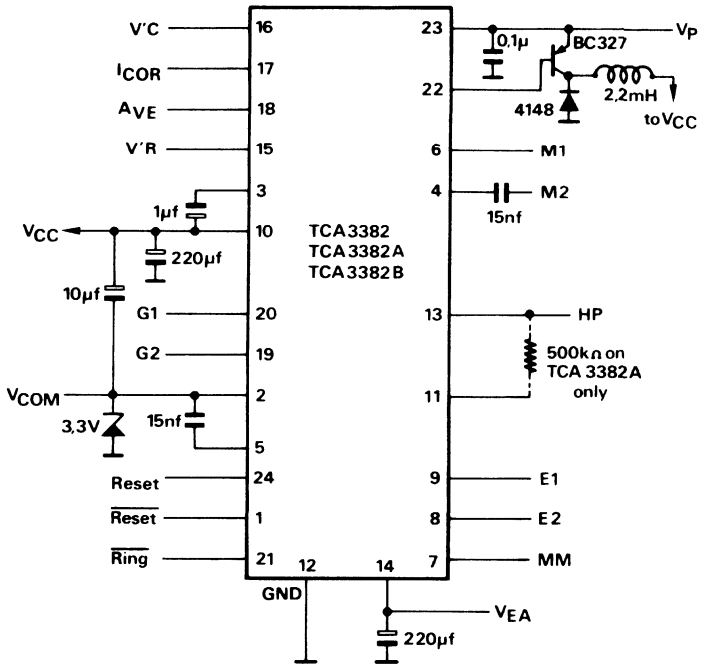


FIGURE 1 – SPEECH MODE CURRENTS/VOLTAGES MEASURES

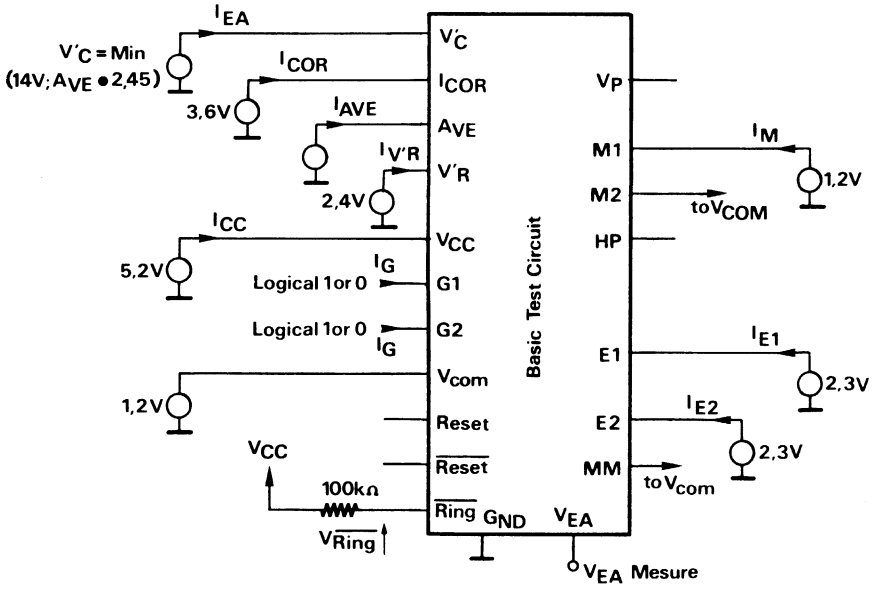


FIGURE 2 – SPEECH GAINS/MAX. LOUDSPEAKER POWER

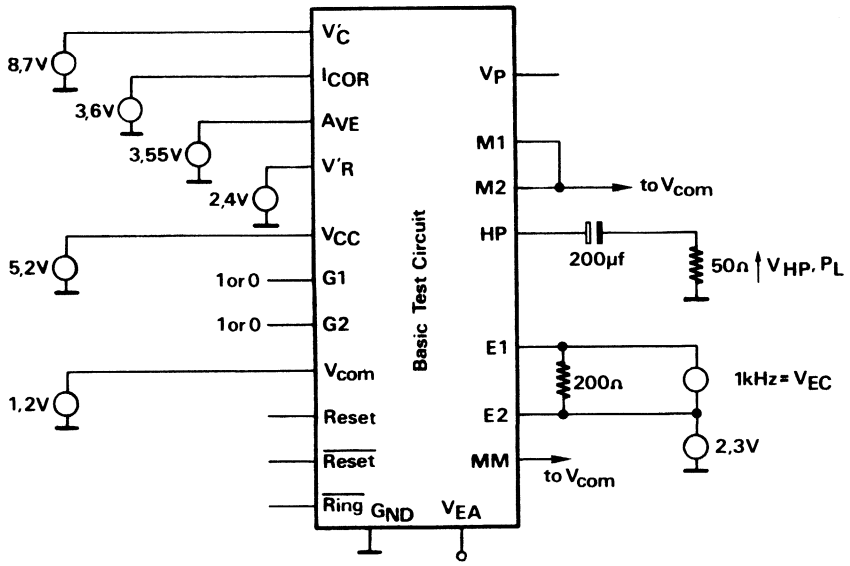


FIGURE 3 – ANTILARSEN

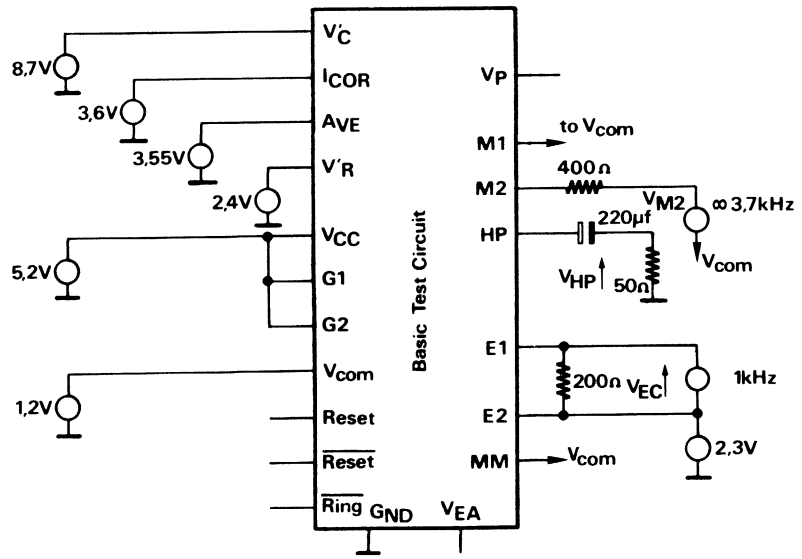


FIGURE 4 – AMPLIFIED MELODY

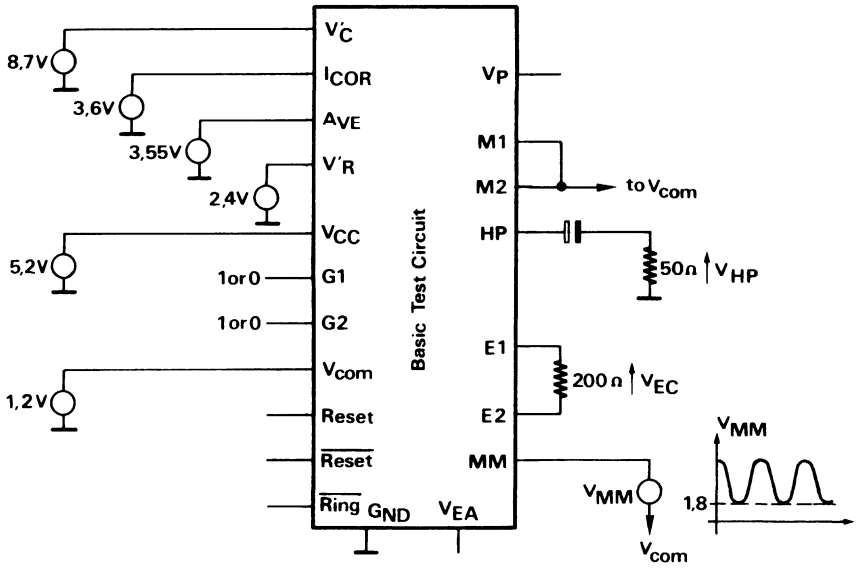


FIGURE 5 – LIMITATION OF V_{AL}

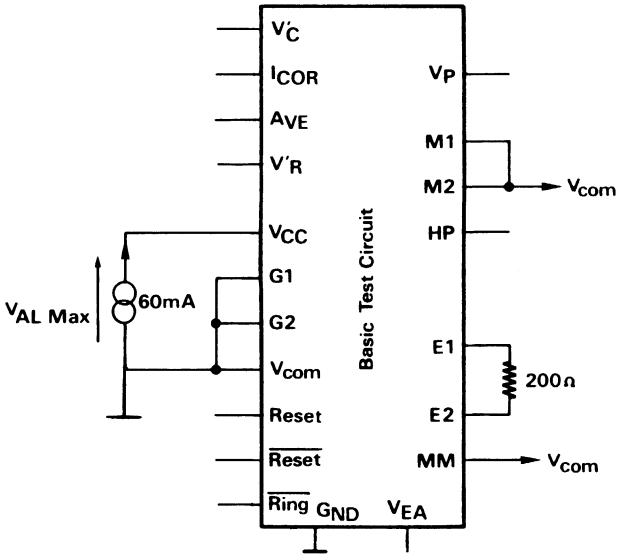


FIGURE 6 – RESET, $\overline{\text{RESET}}$, $V_{\overline{\text{RING}}}$ for V_{AL} = 3.2 V

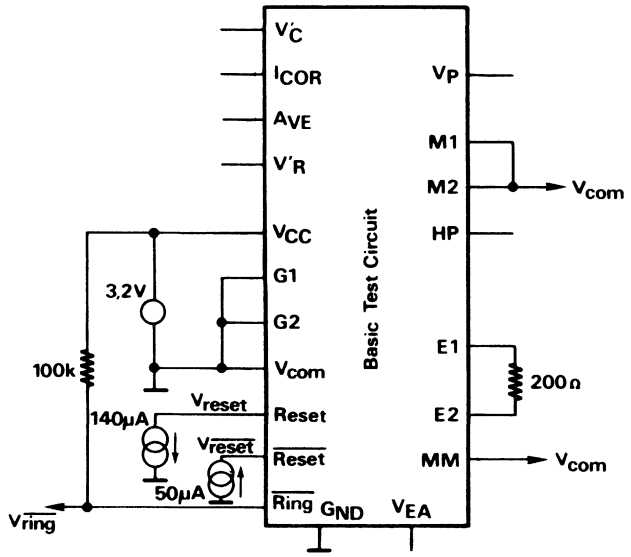


FIGURE 7 – RESET, $\overline{\text{RESET}}$, $V_{\overline{\text{RING}}}$ for V_{AL} = 3.7 V

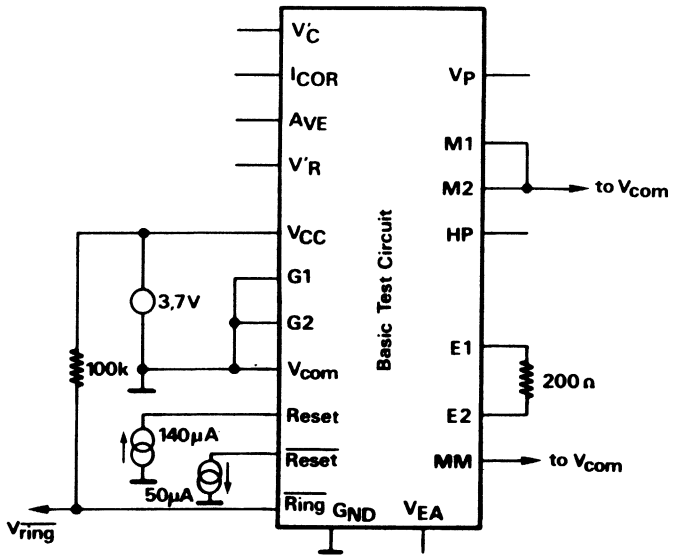
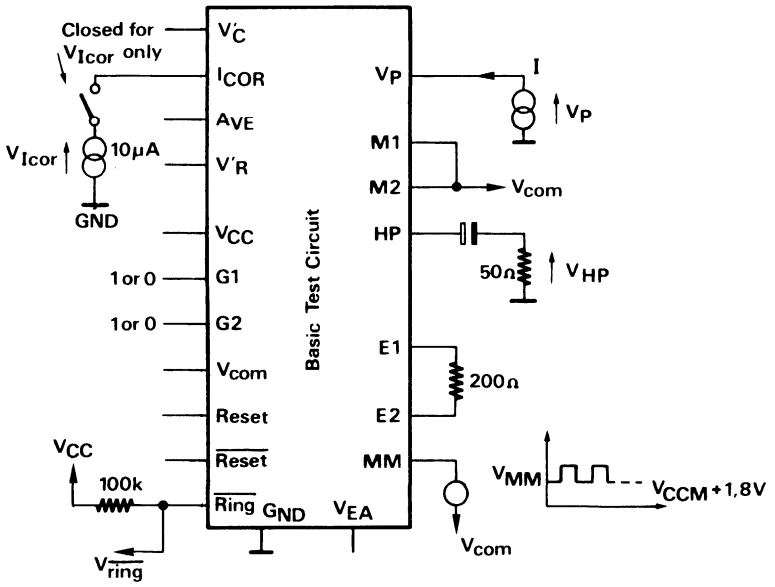
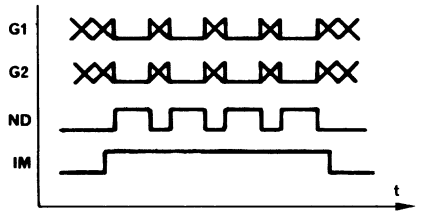


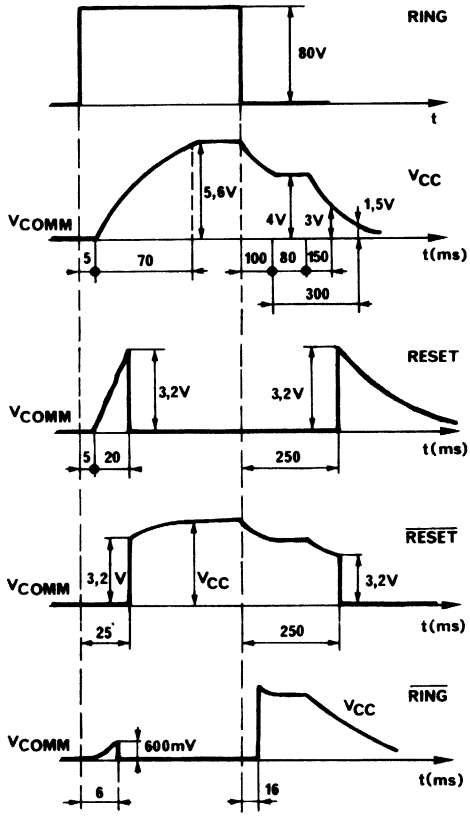
FIGURE 8 – RINGING



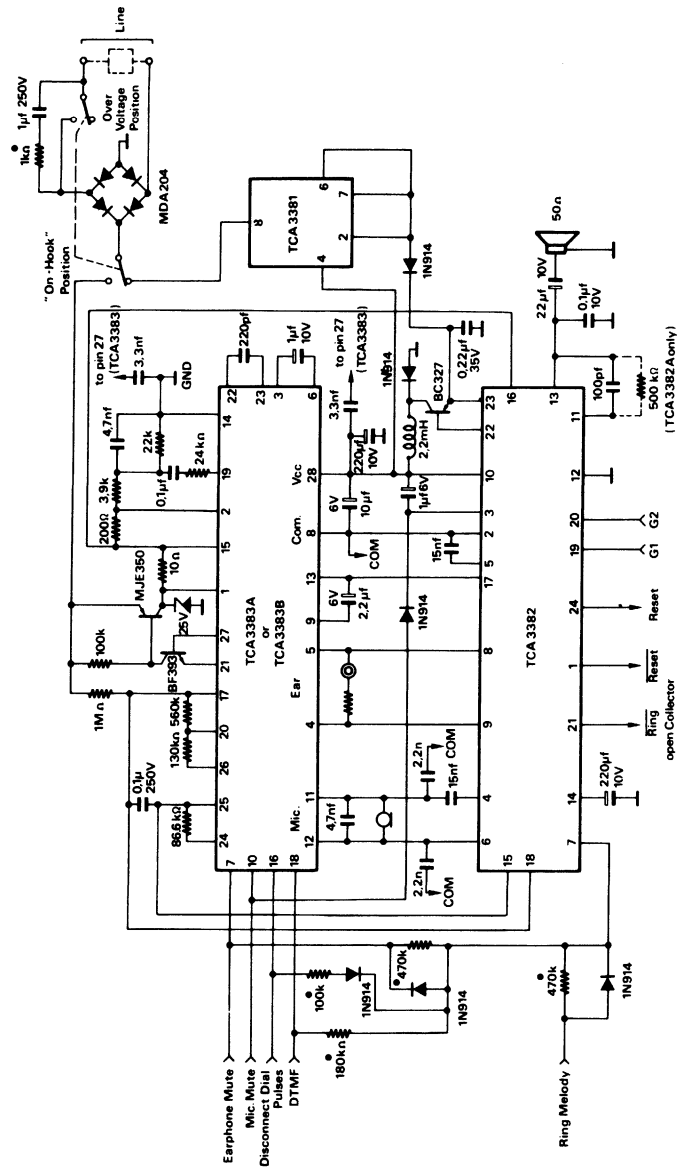


TIMING EXAMPLE

Disconnect dial pulse ("4") output (ND) from the microcomputer. Microinhibit (IM) can go low with ND (or MF) but not before. G1, G2 should be different from 0,0 between train of pulses in order to load the capacity c1 (see application circuit).


RING
80V
t
VCC
5,6V
4V
3V
1,5V
VCOMM
5
70
100
80
150
t(ms)
300
RESET
3,2V
3,2V
VCOMM
5
20
250
t(ms)
RESET
3,2V
VCC
3,2V
VCOMM
25
250
t(ms)
RING
VCC
VCOMM
600mV
6
16
t(ms)

3



● ALL RESISTORS 1% EXCEPT (●) = 5%
●● AVOID TANTALUM CAPACITORS
●● RECOMMENDED EARPHONE IMPEDANCE: 200Ω (WITHOUT SERIAL RESISTOR)
● ALL LOGIC SIGNALS REFERENCED TO COM (INCLUDING DTMF) ↓

MOTOROLA

TCA 3383 A/B

TELEPHONE SET TRANSMISSION CIRCUIT

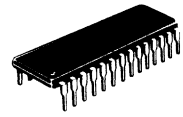
The TCA3383A and TCA3383B telephone set transmission circuits replace the hybrid transformer in a telephone set, include transmit and receive amplifiers and provide line matching and sidetone cancellation. Automatic gain control is available for line length compensation. Together with companion TCA3381 and TCA3382, plus a CMOS microcomputer, a fully electronic telephone set with loudspeaker amplified reception can be built.

- Nominal transmit and receive gains accurate to ±1 dB
- Automatic preset sidetone network adjustment, compensates for line length variations
- Optional microphone and earphone amplifier automatic gain control to compensate variations in line length
- Regulated D.C. output to power external circuitry
- Multifrequency or Loop Disconnect Dialling Inputs
- Mute facility for transmit and receive amplifiers
- Low noise
- Low current consumption.

TELEPHONE SET TRANSMISSION CIRCUIT

BIPOLAR INTEGRATED CIRCUIT

3

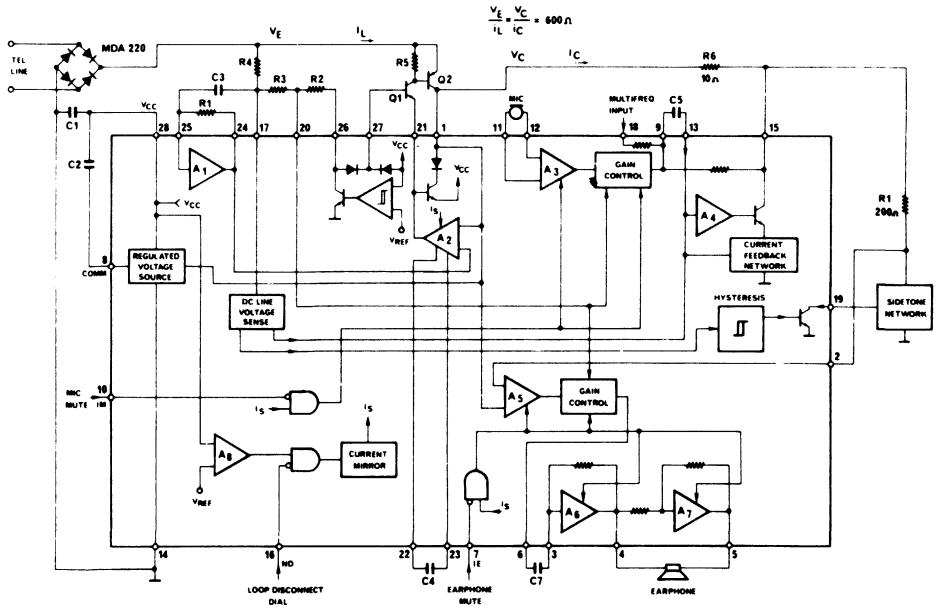


28 PIN DIL PACKAGE

Ordering Information:

TCA3383A-DP/TCA3383B-DP

TCA 3383 BLOCK DIAGRAM



3

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Operating Ambient Temperature	T_A	− 20 to + 60	°C
Storage Temperature	T_S	−65 to +150	°C
Operating Junction Temperature	T_J	150	°C
Thermal Resistance: Plastic Package	R_T	80 to 110	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Start-up Characteristics (I_{CH} = 1mA max)	2					
Line current (V_E >10V)		I_{LD}	28	120	150	mA
Q_2 Emitter voltage (I_{LD} <28 mA)		V_{ED}	–	4.6	5.6	V
Start-up delay time	13	t_D	150	–	350	ms
(C_1 = 220 µF, C_5 = 2,2 µF)						
Power Supply Characteristics	2					
(−25°C ≤ T_A ≤ 70°C, I_{CH} = 1 mA)						
Line current (V_E > 11 V)		I_L	27.5		57.5	mA
Q2 Emitter voltage		V_E				
I_L = 15 mA			–	6.3	6.9	V
I_L = 25 mA			–	7.8	10.9	V
Regulated supply:						
Voltage (V_{AL} = V_{CC} − V_{COM})		V_{AL}	3.8	4	4.2	V
Regulation (0 < I_{CH} < 3 mA)		ΔV_{AL}	–	10	80	mV
Internal supply:						
Voltage (I_{CH} = 0)		V_{CC}	4.8	5.2	5.6	V
Regulation (0 < I_{CH} < 5 mA)		ΔV_{CC}	–	500	–	mV
Output impedance (0 < I_{CH} < 5 mA)		Zout	–	150	300	Ω
Transmit Gain						
(300-3400 Hz)						dB
TCA3383A	3					
Nominal gain, DC Resist. = 1280 Ω, 0 dBm on line		G_{EN}	45.5	46.5	47.5	
Short line gain, DC Resist. = 300 Ω, 0 dBm on line		G_{EC}	39	41	43	
TCA3383B						
Nominal Gain, DC Resist. = 1280 Ω, 0 dBm on line		G_{EN}	51.5	52.5	53.5	
Short line gain, DC Resist. = 300 Ω, 0 dBm on line		G_{EC}	45	47	49	
Receive Gain	4					
(300-3400 Hz)						dB
Nominal gain, DC Resist. = 1280 Ω − 10 dBV receive level		G_{RN}	3	4	5	
Short line gain, DC Resist. = 300 Ω, − 10 dBV receive level		G_{RC}	−4.5	−2.5	−0.5	
Line Terminating Impedance	4					
(I_L ≥ 18 mA)						
300 − 500 Hz		Z_P	360	600	1000	Ω
500 − 3400 Hz		Z_P	450	600	750	
Microphone Amplifier Input Impedance	3					
300 − 3400 Hz TCA 3383 A		Z_E	350	400	450	Ω
TCA 3383 B			9000	14000		
Earphone Amplifier Output Impedance	4					
300 − 3400 Hz		Z_R	–	3	10	Ω
Common Mode Rejection						
Receive amplifier	5	R_{RCM}	–	65	–	dB
Microphone Muting	3					
Gain reduction (300-3400 Hz, I_L ≥ 18 mA, 0dBm, V_{IM} ≥ V_{IMH} min.)		A_{HM}	−60	−71	–	dB
Mute level "High" (COMM = Reference)		V_{IMH}	V_{AL} −0.8	–	–	V
Mute level "Low" (COMM = Reference)		V_{IMB}		–	0.8	V

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Earphone Muting						
Gain reduction	4	A_{HR}	−60	−69	–	dB
(300-3400 Hz, I_L > 18 mA, −10 dBV, V_{IE} > V_{IEH})						
Mute level "High" (COMM = Reference)		V_{IEH}	V_{AL} −0.8	–	–	V
Mute level "Low" (COMM = Reference)		V_{IEB}	–	–	1.5	V
Logic Ports Input Current						
IM, IE, ND	3,4	I	–	1	50	µA
Dialling Input Characteristics	3,4					
Input "High"		V_{NDH}	V_{AL} −0.8	–	–	V
Input "Low"		V_{NDB}	–	–	0.8	V
Open loop line current (V_E = 46.5V)		I_{LD}	–	45	150	µA
Switching of Sidetone Network Resistors	6					
Q_2 Emitter voltage, β off		$V_{E\beta OFF}$	10.5	11.2	–	V
Q_2 Emitter voltage, β on		$V_{E\beta ON}$	–	11.2	13	V
"ON" Resistance β (300-3400 Hz)		$R_{ON\beta}$	–	–	2	KΩ
"OFF" Resistance β (300-3400 Hz)		$R_{OFF\beta}$	100	–	–	KΩ
Transmit Harmonic Distortion RBC < 1280 Ω	3	d_E				
Line level +3 dBm (F = 1kHz)			–	0.4	3	%
Line level +6 dBm (F = 1kHz)			–	–	10	%
Receive Harmonic Distortion	4	d_R				
RBC < 1280 Ω, R_{phone} = 200 Ω)						
Receive level −11.5 dBV (F = 1 kHz)			–	1.5	3	%
Receive level −10 dBV (F = 1 kHz)			–	–	10	%
Receive Noise	2	B_R	–	–	500	µV
Transmit Noise (e = 0V, DCR = 300 Ω)	3	B_E	–	–	−64	dBmp
MF Input Gain						
Pin 18 to line (600 Ω)	7	G_{MF}	4.0	5.0	6.0	dB
MF Input Impedance	7	Z_{MF}	50	80	110	KΩ
Side Tone Cancellation	3					
F = 300 − 3400 Hz	3					
DCR = 1280 Ω						
− 10 dBV (316 mV_{RMS}) on line		G_{ST}	–	−38	−32	dBV

Note: The line voltage is equal to the voltage on the emitter of Q_2 (V_E) plus the forward voltage drop across the diode bridge (max. 1.5 V).

TCA3383A/B TELEPHONE SET TRANSMISSION CIRCUITS

CIRCUIT DESCRIPTION (See block diagram)

The TCA3383 A/B bipolar integrated circuits interface the microphone and earphone of a telephone set to the two-wire circuit of the telephone line. Controlled gain amplifiers are included for the microphone signal output to the line and the incoming line signal to the earphone. Automatic switching between two preset sidetone networks* is available and inputs are available for either multifrequency (DTMF) or loop disconnect dialling.

DC SUPPLY (See block diagram)

Power for the IC is derived from the line via external transistor Q_2 and pin 1, which supply current to the V_{CC} rail internally.

C_1 is a smoothing capacitor for the unstabilised 5V supply voltage V_{CC} (pin 28 − pin 14). The 4V stabilised supply between COMM and V_{CC} (pin 28 − pin 8) is smoothed by C_2. Power is available for external circuitry such as DTMF generator, MCU, etc.

In the start-up condition immediately after connection to the line C_1 (V_{CC}) is charged rapidly by biasing Q_2 on via Q_1, which in turn is biassed on by the resistor network R_4, R_3, R_2 and the internal circuitry on pins 26, 27. Fig. 8 shows the typical line current vs line voltage characteristic of the circuit and fig. 9 shows the typical regulation of the supply voltages (pins 28,8) as a function of external load current.

CONTROLLED GAIN

The gain of the microphone amplifier and earphone amplifier can be automatically controlled by the D.C. level on the line by the divider R_3/R_2 on pin 20. Additionally, the DC line voltage sensed at pin 17 is used to switch in or out additional resistors in the sidetone network to obtain preset levels of sidetone cancellation as a function of line length.

Fig. 11 shows how to suppress, with two diodes, the AGC for microphone and earphone if the compensation in line length is not needed.

The variation in amplifier gains between different units under given conditions is tightly controlled in manufacture – nominal gain variation in transmission is ±1 dB max, so that the performance in a given system is well defined.

MUTE FUNCTIONS

Separate microphone and earphone muting is provided through pins 10 and 7 respectively if they are logic level "high".

Muting is also provided during the start-up delay time.

DIALLING

Loop disconnect dialling pulses can be applied at pin 16 ("High" to disconnect). In order to avoid dial clicks, the earphone and the microphone amplifiers ought to be muted externally by applying a logic "1" on pin 7 and 10.

The line current is interrupted by switching of the transistor Q_1 which obtains emitter drive from amplifier A_2, which in turn derives its supply current from the current mirror controlled by the AND gate at pin 16.

Multifrequency dialling tones can be transmitted to the line via pin 18, which is linked internally to pin 9 via a 80k resistor.

*See application circuit: R8 serial + R9, C6 parallel to ground when beta OFF or R8 serial + R9, C6, R11 parallel to ground when beta ON (short line)

PIN DESCRIPTION

Pin 1: V_C	Low voltage line image
Pin 2 : V''_C	Speech signal to earphone
Pin 3 : V_{EAR}	Negative input of earphone amplifier
Pin 4, 5 : E1, E2	Earphone connections
Pin 6 : E_{CONT}	Speech signal to earphone, controlled in function of line length
Pin 7 : IE	Inhibit earphone (Active "High")
Pin 8 : COMM	Internal reference. External available ground.
Pin 9 : I_{AC}	Input of AC line current amplifier
Pin 10 : IM	Inhibit microphone (Active "High")
Pin 11, 12 : M1, M2	Differential input for 2-wires microphone
Pin 13 : I_{COR}	Input of DC line current controller
Pin 14 : GROUND	Most negative voltage
Pin 15 : V'_C	Analog signal output to line. Line terminating impedance matching
Pin 16 : ND	Loop disconnect dial pulses input ("High" to disconnect)
Pin 17 : AV_E	DC line voltage sense input
Pin 18 : MF	DTMF input
Pin 19 : Beta	Open collector output to switch sidetone network with regard to line length
Pin 20 : V_{CONT}	Part of DC line voltage for gain control of microphone and earphone amplifiers with regard to line length and Controlling DC part
Pin 21 : I_{REG}	Current line regulation control
Pin 22, 23 : C1, C2	Connection of an external capacity (typ. 470 pF) for internal stability
Pin 24 : V_{AC}	Op-amp output for AC impedance transfer
Pin 25 : V'_R	Op-amp negative input for AC impedance transfer
Pin 26 : V_{DEM}	Internally input connected to ground, except during start-up phase, providing then the control on external transistor Q1
Pin 27 : V'_{DEM}	Output to be connected to the base of external transistor Q1 start-up characteristic
Pin 28 : V_{CC}	Positive supply, regulated to 4.0 V between V_{CC} and COMM

FIGURE 1 – BASIC TEST CIRCUIT

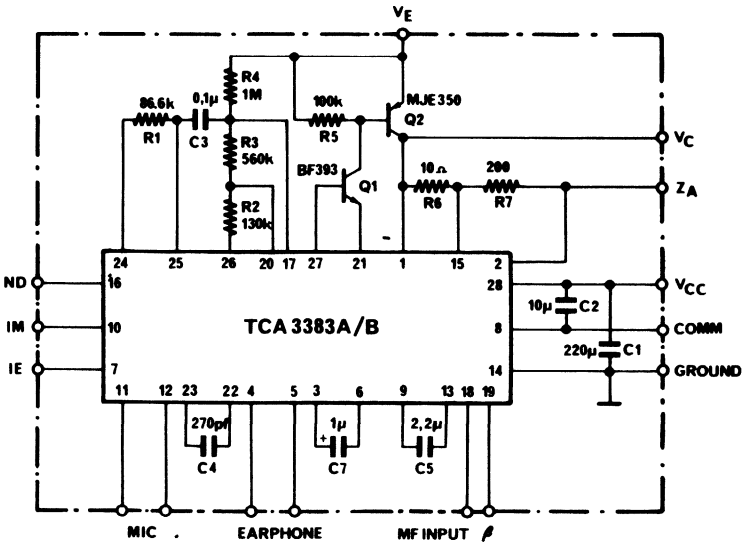
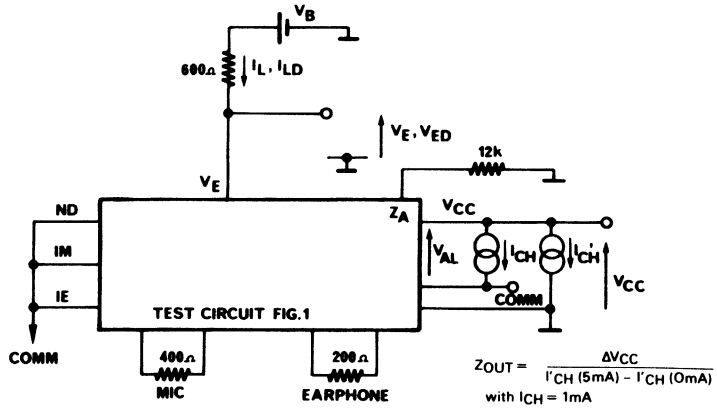


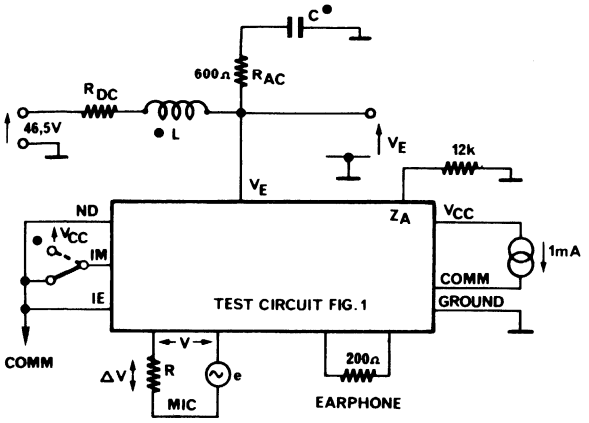
FIGURE 2 – I_{LD}, V_{ED}, t_D, I_L, V_E, V_{AL}, V_{CC}, BR TESTS



3

FIGURE 3 – G_{EN}, G_{EC}, Z_E, A_{HM}, V_{IMH}, V_{IMB}, B_E TESTS

$G_{EN} = G_E$ for nominal lines
$G_{EC} = G_E$ for short lines



● $L\omega >> 600\ \Omega$

$1/C\omega << 600\ \Omega$

$$A_{HM} = 20 \log \frac{U_E\ (I_M = 0)}{U_E\ (I_M = 1)}$$

$$G_E = 20 \log \frac{U_E}{e}$$

$$Z_E = \frac{V_{MIC} \cdot R^{\bullet}}{\Delta V}$$

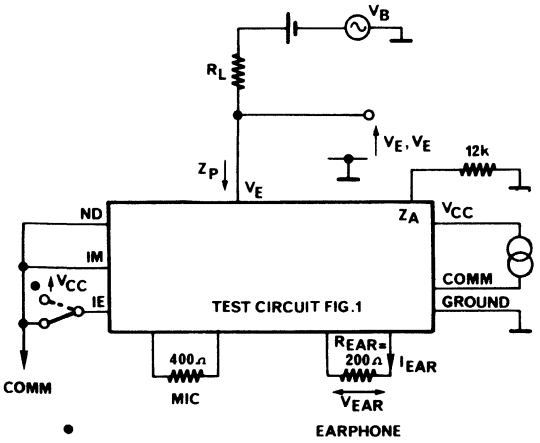
• R = 400 Ω for TCA 3383 A
R = 14000 Ω for TCA 3383 B

$$G_{ST} = 20 \log \frac{U_{EAR}}{1\ V}$$

(Note: A_{HM}, G_E, B_E, G_{ST} with R = 400 Ω)

FIGURE 4 – G_{RN}, G_{RC}, Z_P, Z_R, A_{HR} TESTS

$G_{RN} = G_R$ for nominal lines
$G_{RC} = G_R$ for short lines



$$A_{HR} = 20 \log \frac{U_{EAR}\ (I = 0)}{U_{EAR}\ (I = 1)}$$

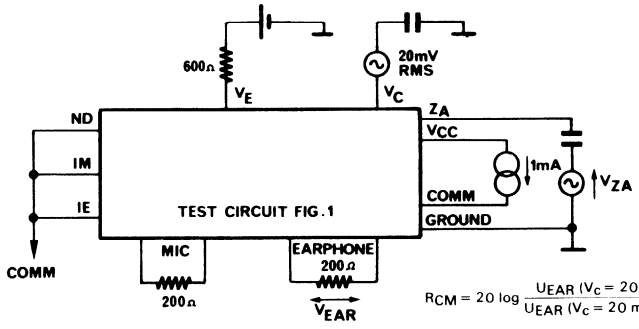
$$G_R = 20 \log \frac{U_{EAR}}{U_E}$$

$$Z_P = \frac{R_L\ U_E}{V_B - U_E}$$

$$Z_R = \frac{400\ (U_{EAR}\ (400) - U_{EAR}\ (200)}{2\ U_{EAR}\ (200) - U_{EAR}\ (400)}$$

(R_{EAR} = 400 Ω or 200 Ω for Z_R calculation)

FIGURE 5 – COMMON MODE REJECTION – RECEIVE AMPLIFIER TEST CIRCUIT



3

FIGURE 6 – $V_{E\beta}$ $R_{ON\beta}$ $R_{OFF\beta}$ TEST CIRCUIT

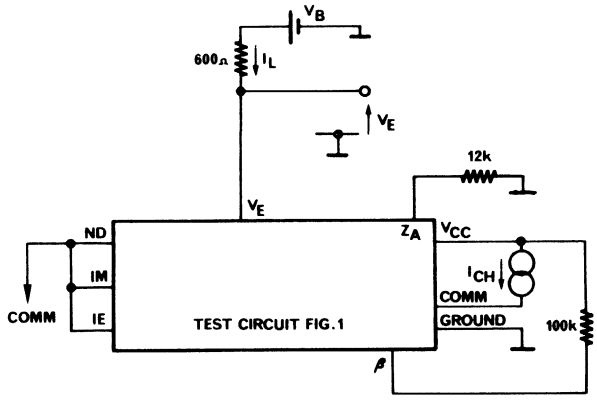


FIGURE 7 – MF TRANSMISSION

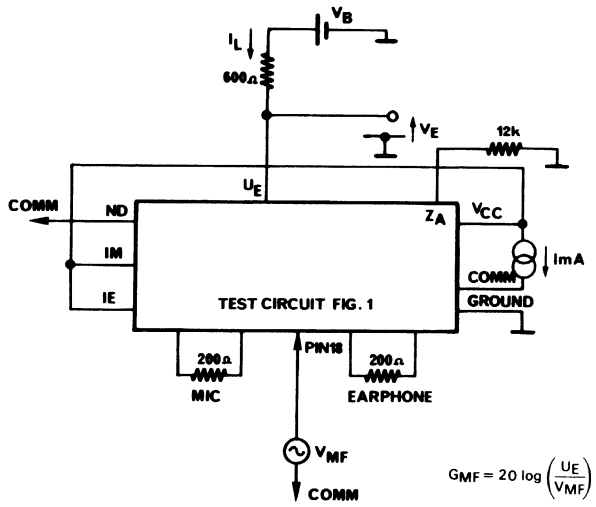


FIGURE 8 – DC SUPPLY MASK
(including diode Bridge)

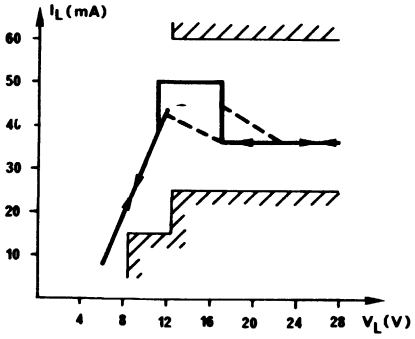


FIGURE 9 – TYPICAL REGULATION CHARACTERISTICS OF SUPPLY VOLTAGES

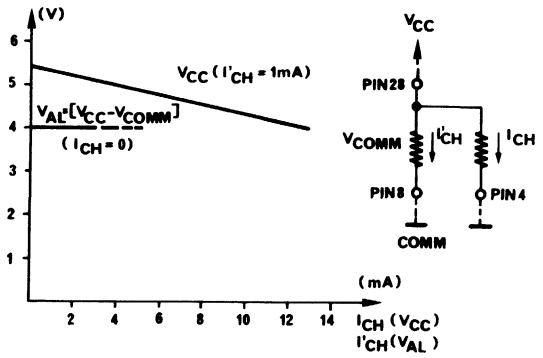


FIGURE 10 - TYPICAL VARIATION OF TRANSMIT AND RECEIVE GAINS WITH LINE VOLTAGE

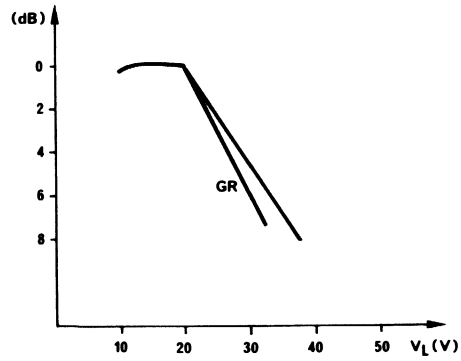
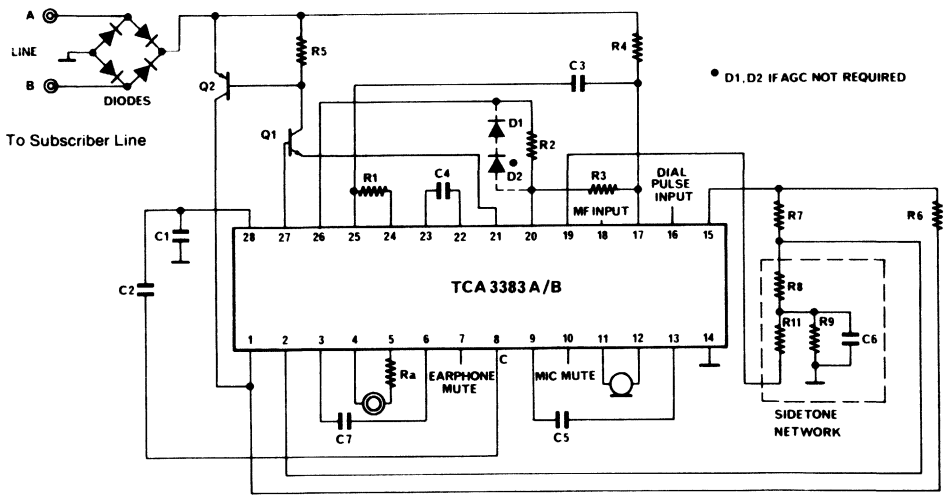


FIGURE 11 - TCA 3383A/B BASIC APPLICATION CIRCUIT
ND, IM, IE tied to COM if not used.

Typical Application



COMPONENT LIST – APPLICATION FIGURE 11

1. Transistors

Type	Nr	V_{CEOmin}	βmin (I_C = 10 mA)	I_{Cmax}(mA)	I_{Cpeak}(mA)	Location
PNP	MJE350	150V	30	60	150	Q2
NPN	BF393	150V	30	5	15	Q1

2. Diode bridge: MDA 204

V_{min} = 200 V

3. Resistors

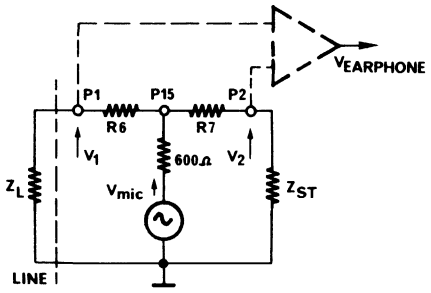
R_1 = 86.6 KΩ ±1%
R_2 = 130 KΩ ±1%
R_3 = 560 KΩ ±1%
R_4 = 1 MΩ ±1%
R_5 = 100 KΩ ±10%
R_6 = 10 Ω ±1%
R_7 = 200 Ω ±1%
$R_8 + R_9$ = 12 K for 600Ω line (modulus)

4. Capacitors

C_1 = 220 µF V = 6V
C_2 = 10 µF V = 5V
C_3 = 100 µF V = 20V
C_4 = 270 µF V = 6V
C_5 = 2.2 µF V = 5V
*C_6 = 3.3 nF V = 10V
C_7 = 1.0 µF V = 5V

*indicative value

FIGURE 12 – CALCULATION OF SIDETONE NETWORK



In balance, $U_{earphone}$ resulting from U_{mic} = 0

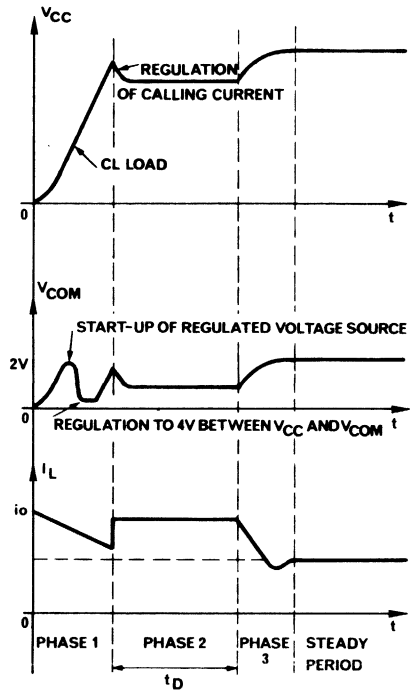
ie $U_1 = U_2$

hence $\frac{Z_L}{Z_L + R_6} = \frac{Z_{ST}}{Z_{ST} + R_7}$

thus $Z_{ST} = Z_L \frac{R_7}{R_6}$

(For Z_L = 600 Ω, R_6 = 10 Ω, R_7 = 200 Ω ∴ Z_{ST} = 12K)

FIGURE 13 – START-UP PERIOD (See block diagram)



MOTOROLA

TCA 3385

Product Preview

TELEPHONE RING SIGNAL CONVERTER

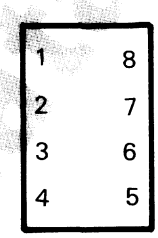
The TCA3385 is a high density bipolar telephone ring converter. This circuit is designed for use with the TCA3386 (speech circuit and monitoring speaker amplifier). These devices, together with a microprocessor form the basis of a fully electronic telephone set. In On-Hook position, this circuit detects the presence of a ring signal on the line, sends this information to the MPU and powers all the system (MPU and TCA3386). Energy is derived from ring line signal. A switching regulator, with high efficiency, converts the available high voltage, low current into a low voltage, high current.

Threshold level detection and input impedance may be set by an external resistor.

The output for microprocessor can optionally contain ring signal frequency information which can be used by the microprocessor to distinguish between different tones (useful for German specifications). This circuit includes protection against over-voltages.

- Power derived from Ring Signal
- Regulated supply voltage: 5.25V
- Ring detection output for microprocessor
- High efficiency switching regulator
- Line impedance matching, programmable
- Threshold ring detector, programmable
- Lightning and mains protection.

PIN ASSIGNMENT



This document contains information on a new product.
Specifications and information herein are subject to change without notice.

MOTOROLA

TCA3386

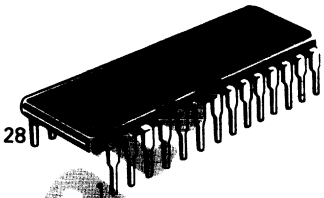
Product Preview

FEATURE TELEPHONE SET I.C.

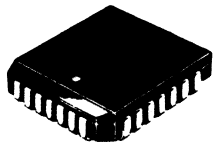
TCA3386 is designed to be used in mid- and high-end telephone sets, associated with a microcomputer. It contains the circuitry for the d.c. mask, transmit and receive amplifiers, 2-4 wire conversion, impedance matching, sidetone balance, for a high performance speech circuit. It also contains a monitor amplifier to drive a loudspeaker, with anti-acoustic feedback. Tone generators for dtmf dial and ring signal generation are also on chip.

The d.c. mask, volume control, muting, dial pulse timing, dtmf frequencies and levels, ring tones, and monitor functions are all programmable/controllable through the 2-wire MCU port. Power supply and reset for the MCU are provided, and the TCA3386 can be used in ring mode with the addition of the Ring Power circuit TCA3385. TCA3386 is implemented in an advanced high density bipolar process.

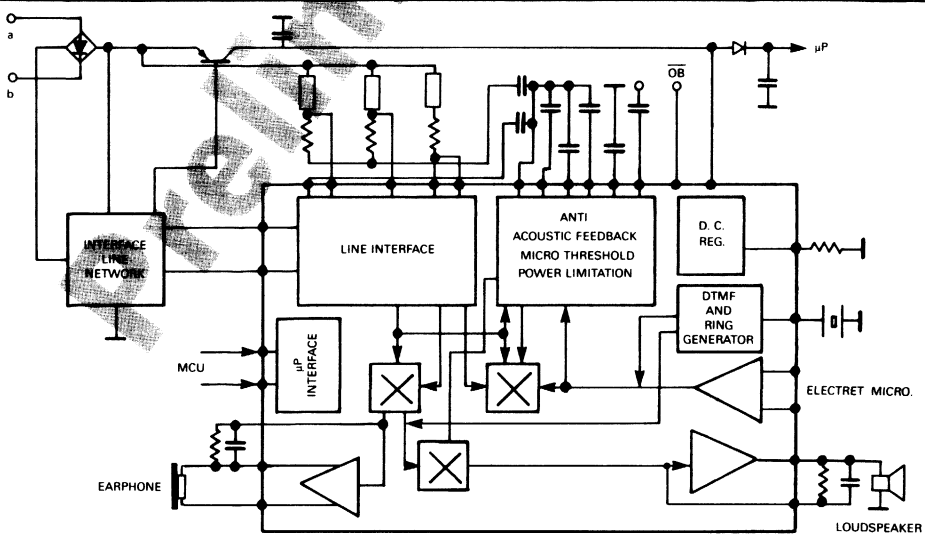
- MCU controlled feature telephone set with integrated loudspeaker monitor.
- Software programmable d.c. mask (France, UK, German, PABX)
- 2-4-wire conversion with programmable impedance and sidetone balance, and automatic adjustment with line length
- DTMF and ring tone generator, with timing and level controlled by MCU
- 2-wire serial MCU port, and regulated d.c. supply with reset for MCU
- Loudspeaker monitor with anti-howl circuit and automatic power adjustment to available line current, and facility to inter face external Speakerphone (MC34118)
- Uses low cost 500 kHz ceramic resonator



P SUFFIX
PLASTIC PACKAGE
CASE 710-02



FN SUFFIX
PLCC-28
CASE 776-01



MOTOROLA

TCA 3388

Product Preview

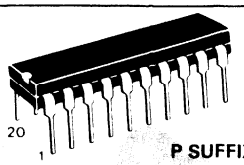
SPEECH CIRCUIT

The TCA3388 is a high density bipolar telephone speech network to replace the hybrid circuit in a telephone set.

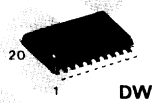
This circuit includes sidetone balance, microphone and push pull earphone amplifier with loop length compensation, programmable impedance (real or complex), programmable DC mask (French, UK Low voltage and PABX configuration for each), direct interface for a DTMF/pulse dialer (adjustble DTMF input, pulse input, hook status output and mute input), regulated power supply and protection against excess signal voltage.

Design precautions have been taken to increase RFI immunity. This circuit associated with a DTMF/pulse dialer (MC145516) and a tone ringer (MC34017) forms the basis of a low cost telephone set.

- Low voltage, low current operation: high peak-to-peak signal on the line
- DC mask programmable by external pins
- 2 to 4 wire conversion
- Programmable impedance (real or complex)
- Programmable sidetone balance with automatic line length tracking
- Automatic line length receiving and sending gain control
- Microphone amplifier with externally adjustable gain (piezo or electret transducers)
- Earphone push pull amplifier with externally adjustable gain (piezo or electrodynamic transducers)
- Mute facility for transmit and receive amplifier
- Regulated supply voltage (3.6V) with high output current capability
- Protection against excess signal voltage
- Interface for DTMF/pulse dialer
- Positive and negative logic input for pulse and mute
- Hook status output

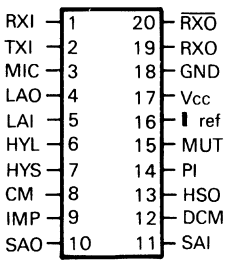


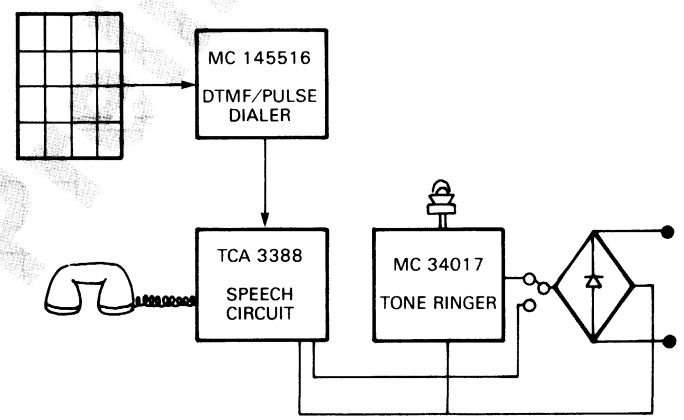
P SUFFIX
PLASTIC PACKAGE
CASE 738



DW SUFFIX
PLASTIC PACKAGE
CASE 751D

PIN ASSIGNMENT

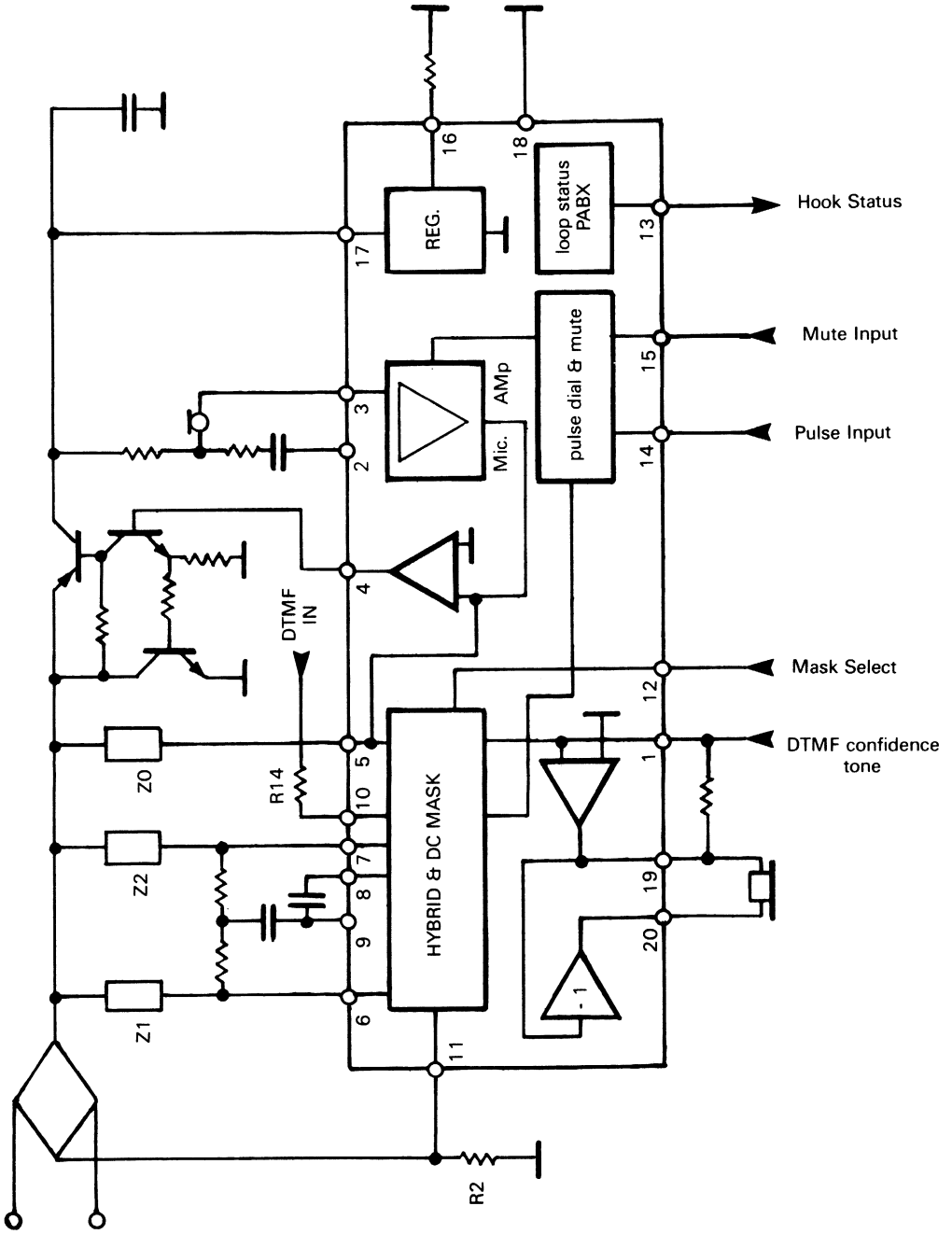


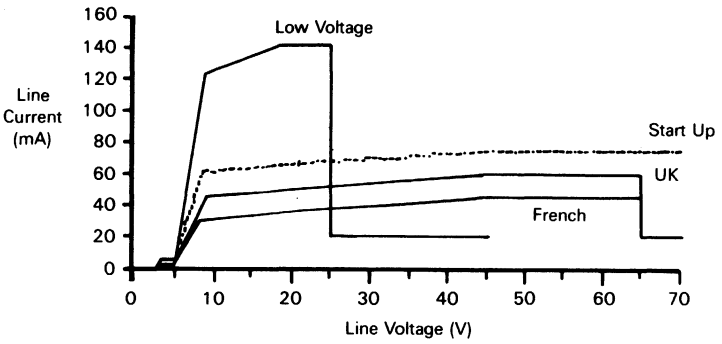


LOW END TELEPHONE SET

This document contains information on a new product.
Specifications and information herein are subject to change without notice.

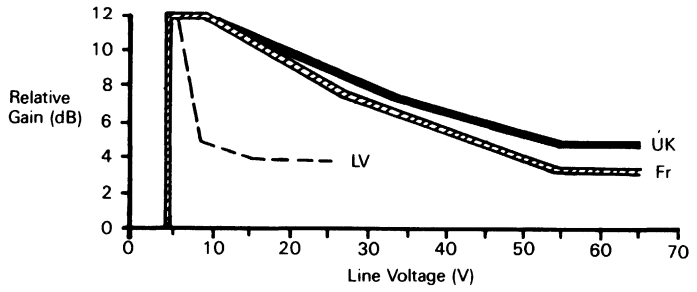
TCA 3388 BLOCK DIAGRAM



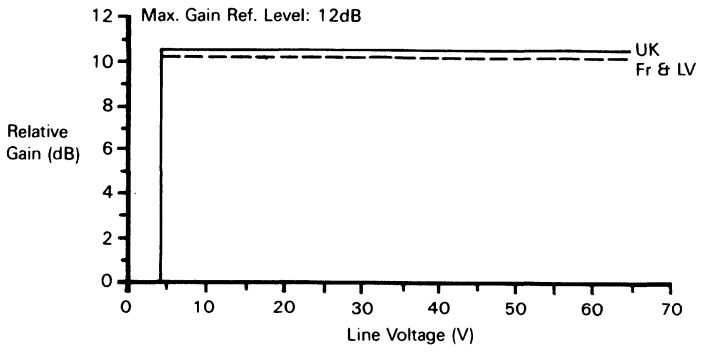


3

TCA 3388: DC MASKS



TCA 3388: GAIN REGULATION



TCA 3388: GAIN REGULATION, PABX MODE

PIN DESCRIPTION

1:RXI - Input for Earphone Amplifier and Confidence Tone

This pin receives the line signal via the hybrid balance and gain regulation circuits. A confidence tone (current) may also be applied to this point.

2:TXI - Microphone Current Amplifier Input

3:MIC - Microphone Negative Supply

Bias current from the electret microphone is returned to ground through this pin.

4:LAO - Line Interface Drive Amplifier Output

This pin controls the base of the high voltage line interface transistor.

5:LAI - Line Interface Drive Amplifier Input

This pin receives the AC line voltage from the input impedance network and the current for DTMF signalling. The circuit input impedance is determined by line voltage and current feedback to this pin (which is at virtual earth). The line current signal developed at pin 11 and transferred to pin 10 is received via R14 and the line voltage signal via the network Z0.

This pin may also receive a current for DTMF signalling.

6:HYL - Input for Long Line Hybrid Network

7:HYS - Input for Short Line Hybrid Network

The line signal is received between pins 6 and 10 and between pins 7 and 10. Pin 6 is connected to a network providing hybrid balance for long lines and pin 7 to a network providing hybrid balance for short lines. The received signals are weighted, according to the line length detected, summed and fed via the gain regulation and mute circuit to the earphone amplifier input (pin 1).

Both the hybrid balance impedance and the gain are therefore adapted to the line length. If this pin 7 is left open, the circuit will operate with a fixed hybrid balance impedance defined by the network on pin 6. In PABX mode, the receive mode and hybrid balance impedance are independant of the line length.

8:CM - Mask Decoupling Capacitor

For a return loss greater than 20 dB, and an imput impedance equal to 600 ohms at 300 Hz, C = 0.68µF.

9:IMP - Impedance Network Return Point

10:SAO - Line Current Sense Amplifier Output

11:SAI - Line Current Sense Amplifier Input

Voltage at this pin is proportional to the line current (I line x R2).

12:DCM - DC Mask Selection

Four dc masks are selected according to the DC voltage at this pin. An internal current generator sources (loop closed) or sinks (during line break) a constant current. The DC mask can be chosen by connecting appropriate external components (resistor, capacitor, or resistor plus capacitor) between this pin and ground.

13:HSO - Hook Status Output/PABX Mode

This pin is a digital output and reflects the status of the loop. HSO is high when the loop is closed, and low when loop is open. This pin also sets PABX mode if the load current is greater than 20µA. In PABX mode the transmission and reception gains are fixed. The hybrid balance impedance is fixed whether a single or double network is used.

14:PI - Pulse Dialing Input

This pin is a bidirectional input current for pulse dialing.

15:MUT - Mute Input

This pin is bidirectional input current for combined microphone and earphone mute.

16:I Ref - Reference Current

A programmable resistance connected to this pin sets a reference current for the circuit.

17:V_{CC} - Regulated Supply Voltage

18:GND - Ground

This pin is ground for the entire circuit.

19:RXO - Receive Amplifier Output

This pin is the output of the first receive amplifier. Receive gain is set by connecting a resistor between RXO and RX1.

20:$\overline{RXO}$ - Complementary Receive Amplifier Output

This pin is the output of the second receive amplifier.

Protection Mode

Protection is incorporated. Detection of excess continuous or signal voltage causes a transfer to a low dissipation mode after a delay.

MOTOROLA

TCA4901

Product Preview

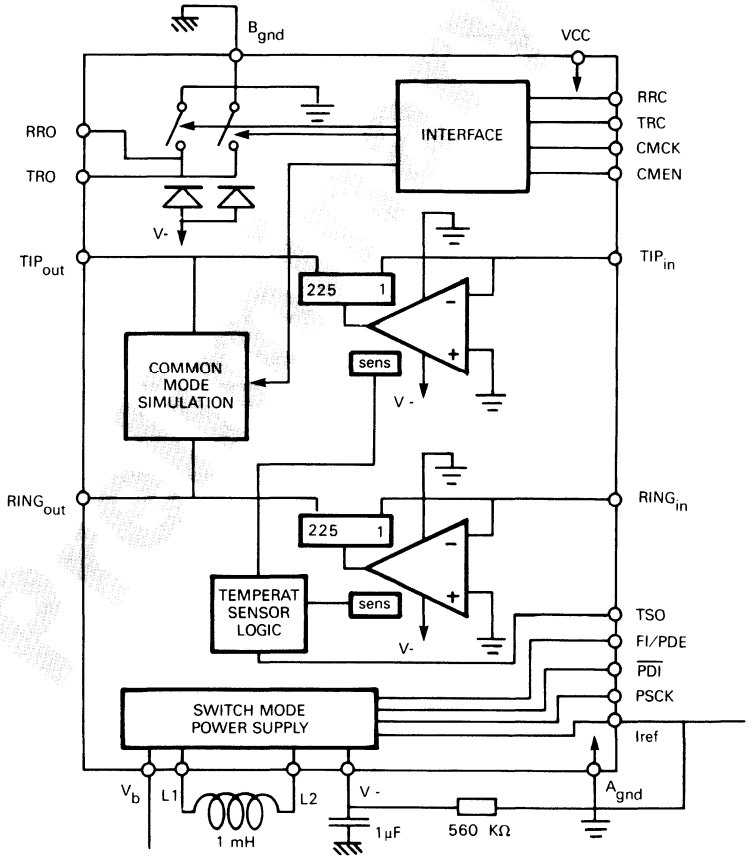
HV SUBSCRIBER LINE INTERFACE
(HV MALC)

The TCA4901 is the high voltage line interface circuit part of the Motorola Advanced Line Card system (MALC). Together with the TCA4905 PCM Subscriber Line Interface Circuit, it performs the BORSCHT functions for an analog subscriber line for Central Office or PBX exchanges. The TCA4901 contains current amplifiers which act as slaves to the low voltage device. It is equipped with Buck-Boost switch-mode power supply unit for optimum power dissipation, and has an on-chip temperature sensor in case of excessive power dissipation. TCA4901 is fabricated in a Dielecrically isolated process, with a voltage handling capability of over 150V.

- Switch Mode Power Supply for optimum power saving
- Step Down to Feed Short Loop
- Step Up to Supply Up to -80V to Long Loop
- Power Down and Power Denial
- On Chip Temperature Sensor
- Test and Unbalanced Ring Relay Driver
- Common Mode Simulation to Calibrate Longitudinal Rejection
- Standard Battery of -48 Volts (-20 to -80 Volts)

3

BLOCK DIAGRAM



MOTOROLA

TCA4905

Product Preview

PCM SUBSCRIBER LINE CIRCUIT
(LV MALC)

The TCA4905 is the low voltage digital signal processing VLSI circuit part of the Motorola Advanced Line Card system (MALC). Together with the TCA4901 High Voltage Line Interface Circuit, it performs the BORSCHT functions for an analog subscriber line for PCM Central Office or PBX exchanges. The TCA4905 contains: D/A and A/D converters; digital filters to define balance and input impedance and receive and transmit gains; d.c. characteristic; and ring-trip detection. High transhybrid rejection is achieved by an adaptive 24 filter set which continually assures that the echo return loss is optimal.

TCA4905 is fabricated in a 2μ BiMOS process, combining high density CMOS with high performance Bipolar circuitry.

FEATURES OF THE MOTOROLA ADVANCED LINE CARD

- 2-chip subscriber line interface providing most of the BORSCHT functions of Battery feed, Ring feed, Supervision, Cofidec, Hybrid 2 to 4 and 4 to 2 wire conversion.
- Adaptive, Programmable Hybrid balance digital filters
- Programmable 2-wire impedance matching digital filter
- Programmable Transmit and Receive gains
- Programmable d.c. line feed characteristics (feed voltage, feed resistance, constant current, battery reversal)
- Switched mode power supply
- 120V line drive circuit
- Self calibrating for balance about earth
- Balanced ringing through SLIC
- Ring trip detection (balanced/unbalanced)
- Loop status detection
- Tax tone injection (Subscriber Private Meter)
- Oversampled sigma-delta A/D, D/A conversion
- A- or μ-law data conversion
- Universal PCM interface
- Performance exceeds CCITT G.713 and Q.517
- Power Saving Power Down/Service denial modes

MALC DESCRIPTION

The Motorola Advanced Line Card I.C.s interface the subscriber line to the PCM digital bus. They offer the designer of an analogue subscriber line card an economical response to the problem of matching the large range of impedances to be found in the local network.

The 2-to 4-wire converter balance impedance is programmable and adaptive to line conditions. Gains and terminating impedances are programmable. These features are provided by DSP techniques with control by an MPU port on the TCA4905 LV chip.

A/D and D/A conversion is performed by 2nd order Σ-Δ converters operating at 4096k sample/s, having a dynamic range greater than 90 dB, in order to achieve the required performance margins.

The 2-wire terminating impedance is synthesised by means of a digital filter. The 4-wire balance impedance uses a repertoire of 24 predetermined programmable filters. At any one time two of the filters are implemented, one actively supplying the inter-path coupling, the other supplying coupling only for comparison. The implemented filters are updated every 32 ms, based on estimates of the received and echoed speech signals from the two implemented filters.

DC Loop

The three sections of the battery feed characteristics are software programmable through the interface bus: constant current, resistive voltage and constant voltage.

Constant current feed is provided in 4 mA steps from 0 to 64 mA.

Resistive feed is 0, 400, 800 and 1600 ohms.

Constant voltage feed is provided in 4V steps from -20V to -80V, 4 mA d.c. Feed with full longitudinal rejection allows hook status detection and telephone battery charging. Battery feed reversal is possible, maintaining all performance features.

Balance about Earth

A longituduinal balance adjustment mode is available which can be used to detect or compensate for any differential components, and achieve high common mode rejection.

Taxation Pulses

Taxation pulses can be input in the range 12k Hz to 18k Hz. The pulse duration is programmable at 50, 100, 150, and 200 ms. The d.c. voltage is adjusted automatically to avoid saturation, and an AGC system adjusts the output to the required level.

Ring Trip

Ring trip detection is performed by the digital filters, giving 100 ms ring trip time.

Standby Modes

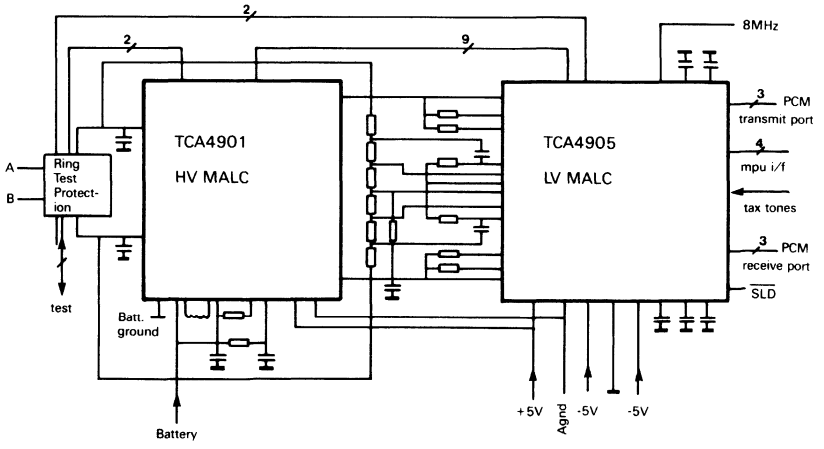
The loop can be placed in a service denial condition where there is no output, or longitudinal rejection. It can also be placed in a zero d.c. loop current condition with longitudinal rejection maintained, allowing hook status detection in a reduced power mode.

PCM and MPU Interface

Two modes for exchange of control and PCM data are possible, pin selectable by the SLD pin. In the first mode the control data is exchanged through a 4-wire MPU port and PCM data passes through separate transmit and receive parts. In the second mode, PCM and control data are multiplexed on the same 3-wire bus. MPU control information includes loop status, reset, digital filter coefficients and other control and status bits arranged in words of 3 bytes.

TCA4905 synchronizes to PCM bus clock frequencies of 512k Hz, 2 MHz, and 8 MHz. The internal synchronisation is adjusted to the appropriate time slot, or in SLD mode is adjusted to the frame sync.

Motorola ALC System Configuration



List of Application Notes and Technical Articles

4

APPLICATION NOTES AND TECHNICAL ARTICLES

SWITCHING

Understanding Telephone Key Systems (AN893)

VOICE DATA

UDLT Evaluation Board (AN943)
Interfacing the MC145418/19 to a Single Twisted Wire Pair (AN945)
Limited Distance Modem using the UDLT Chip Family (AN946)
Data Multiplexing using the UDLT and the Data Set Interface (AN948)
A Voice Data Modem using the MC14522/26 MC145428 and MC14403 (AN949)
A Digital Voice/Data Telephone Set (AN968)
A new High Performance Current Mode Controller teams up with Current Sensing Power MOSFETS (AN976)
Implementing Intergrated Office Communications (AR239)

SUBSCRIBER

A variety of uses for the MC34012 and MC34017 Tone Ringers (AN933)
A Telephone Ringer which complies with FCC and EIA
Impedance Standards (AN937)
Interfacing the Speakerphone to the MC34010/11/13
Speech Networks (AN957)
Transmit Gain -Adjustments for the MC34014 Speech Network (AN958)
A Speakerphone with Receive Idle Mode (AN959)
Equalization of DTMF Signals using the MC34014 (AN960)
The Application of a Telephone Tone Ringer as a Ring Detector (EB112)
The MC145409 Pulse Dialer Application Circuit (EB113)

MODEM

300 Baud Smart Modem with Intelligent MCU Controller using MC145445 and MC145440 (ANHK01)
Low Speed Modem Fundamentals (AN731)
MC14412/MC145440 Chip Set sets new standard in 300 Baud Modem Designs (AN891)
2400 BPS DPSK Modem System using the MC6172/6173 (AN870)
A Four-Wire Full Duplex 1200 Baud Modem Implementation using the MC145450 and MC145415 (AN904)
The application of a Duplexer (EB111)

FILTER

The MC145432 Application Circuit (EB98)

Glossary 5

Glossary of Terms and Abbreviations

The list reproduced here refers to terms found in this and other Motorola publications concerned with Motorola Semiconductor products for Telecommunications.

A law – An European companding/encoding law commonly used in PCM systems.

A/B signaling – A special case of 8th-bit (LSB) signaling in a μ-law system that allows four logic states to be multiplexed with voice on PCM channels.

A/D (analog-to-digital) converter (ADC) – A converter that uniquely represents all analog input values within a specified total input range by a limited number of digital output codes, each of them exclusively representing a fractional part of the total analog input range.

Aliasing noise – A distortion component that is created when frequencies present in a sampled signal are greater than one-half the sample rate.

Answer back – A signal sent by receiving data-processing device in response to a request from a transmitting device, indicating that the receiver is ready to accept or has received data.

Anti-aliasing filter – A filter (normally low pass) that band limits an input signal *before* sampling to prevent aliasing noise.

Asynchronous – A mode of data transmission in which the time occurrence of the bits within each character or block of characters relates to a fixed time frame, but the start of each character or block of characters is not related to this fixed time frame.

Attenuation – A decrease in magnitude of a communication signal.

Bandwidth – The information-carrying frequencies between the limiting frequencies of a communication line or channel.

Baseband – The frequency band occupied by information-bearing signals before combining with a carrier in the modulation process.

Baud – A unit of signaling speed equal to the number of discrete signal conditions or events per second. This refers to the physical symbols/second used within a transmission channel.

Bit rate – The speed at which data bits are transmitted over a communication path, usually expressed in bits per second. A 9600 bps terminal is a 2400 baud system with 4 bits/baud.

Blocking – A condition in a switching system in which no paths or circuits are available to establish a connection to the called party even though it is not busy, resulting in a busy tone to the calling party.

BORS(C)HT – Battery, Overvoltage, Ringing, Supervision, (Codec), Hybrid, Test; the functions performed by a subscriber line card in a telephone exchange.

Broadband – A transmission facility whose bandwidth is greater than that available on voice-grade facilities. (Also called wide band.)

C message – A frequency weighting that evaluates the effects of noise based on its annoyance to the "typical" subscriber of standard telephone service or the effects of noise (background and impulse) on voice-grade data service.

Carrier – An analog signal of fixed amplitude and frequency that combines with an information-bearing signal by modulation to produce an output signal suitable for transmission.

CCITT – Consultative Committee for International Telephone and Telegraph; an international standards group of the European International Telecommunications Union.

Central Office (CO) – A main telephone office, usually within a few miles of a subscriber, that houses switching gear; commonly capable of handling about 10,000 subscribers.

Channel bank – Communication equipment commonly used for multiplexing voice-grade channels into a digital transmission signal (typically 24 channels in the U.S. and 30 channels in Europe).

Circuit, two-wire – A circuit with two conductors providing a "go" and "return" channels.

Circuit, four-wire – A circuit with two pairs of conductors, one pair for the "go" channel and one pair for the "return" channel.

CODEC – COder-DECoder; the A/D and D/A function on a subscriber line card in a telephone exchange.

COFIDEC – COder-FIlter-DECoder; the combination of a codec, the associated filtering, and voltage references required to code and decode voice in a subscriber line card.

Common mode rejection – The ability of a device having a balanced input to reject a voltage applied simultaneously to both differential-input terminals.

Companding – The process in which dynamic range compression of a signal is followed by expansion in accordance with a given transfer characteristic (companding law) which is usually logarithmic.

Compandor – A combination of a compressor at one point in a communication path for reducing the amplitude range of signals, followed by an expander at another point for restoring the original amplitude range, usually to improve the signal-to-noise ratio.

Conference call – A call between three or more stations, in which each station can carry on a conversation simultaneously.

Crosspoint – The operating contacts or other low-impedance-path connection over which conversations can be routed.

Crosstalk – The undesired transfer of energy from one signal path to another.

CTS – Clear to send; a control signal between a modem and a controller used to initiate data transmission over a communication line.

CVSD – Continuous Variable Slope Delta (modulation); a simple technique for converting an analog signal (like voice) into a serial bit stream.

D3 – D3 channel bank; a specific generation of AT&T 24-channel PCM terminal that multiplexes 24 voice channels into a 1.544 MHz digital bit stream. The specifications associated with D3 channel banks are the basis for all PCM device specifications.

D/A (digital-to-analog) converter (DAC) – A converter that represents a limited number of different digital input codes by a corresponding number of discrete analog output values.

Data compression – A technique that provides for the transmission of fewer data bits than originally required without information loss. The receiving location expands the received data bits into the original bit sequence.

dB (decibel) – A power or voltage-level measurement unit.

dBm – The decibel signal level level referred to one milliwatt, i.e., 0 dBm = 1 mW.

dBmO – Signal power measured at a point in a standard test tone level at the same point.

i.e., dBmO = dBm – dBr

where dBr is the relative transmission level, or level relative to the point in the system defined as the zero transmission level point.

dBmOp – Relative power expressed in dBmp. (See dBmO and dBmp.)

dBmp – Indicates dBm measurement made with a psophometric weighting filter.

dBrn – Relative signal level expressed in decibels above reference noise, where reference noise is 1 pW. Hence, 0 dBrn = 1 pW = –90 dBm.

dBrnC – Indicates dBrn measurement made with a C-message weighting filter. (These units are most commonly used in the U.S., where psophometric weighting is rarely used.)

dBrnc0 – Noise measured in dBrnc referenced to zero transmission level.

Decoding – A process in which one of a set of reconstructed analog samples is generated from the digital character signal representing a sample.

Delay distortion – Distortion that occurs on communication lines due to the different propagation speeds of signals at different frequencies, measured in microseconds of delay relative to the delay at 1700 Hz. (This type of distortion does not affect voice communication, but can seriously impair data transmission.)

Delta modulation – A simple digital coding technique that produces a serial bit stream corresponding to changes in analog input levels; usually utilized in devices employing continuously variable-slope delta (CVSD) modulation.

Demodulator – A functional section of a modem that converts received analog line signals to digital form.

Digital telephone – A telephone terminal that digitizes a voice signal for transmission and decodes a received digital signal back to a voice signal. (It will usually multiplex 64 kbps voice and separate data inputs at multiples of 8 kbps.)

Distortion – The failure to reproduce an original signal's amplitude, phase, delay, etc. characteristics accurately.

DPSK – Differential Phase Shift Keying; a modulation technique for transmission where the frequency remains constant but phase changes will occur from 90°, 180° and 290° to define the digital information.

DTMF – Dual Tone Multi Frequency (dialing).

Duplex – A mode of operation permitting the simultaneous two-way independent transmission of telegraph or data signals.

Echo – A signal that has been reflected or returned as a result of impedance mismatches, hybrid unbalance, or time delay. Depending upon the location of impedance irregularities and the propagation characteristics of a facility, echo may interfere with the speaker/listener or both.

Echo suppressor – A device used to minimize the effect of echo by blocking the echo return currents; typically a voice-operated gate that allows communication one way at a time.

Encoder (PCM) – A device that performs repeated sampling, compression, and A/D conversion to change an analog signal to a serial stream of PCM samples representing the analog signal.

Equalizer – An electrical network in which phase delay or gain varies with frequency to compensate for an undesired amplitude or phase characteristic in a frequency-dependent transmission line.

FDM – Frequency-Division Multiplex; a process that permits the transmission of two or more signals over a common path by using a different frequency band for each signal.

Frame – A set of consecutive digit time slots in which the position of each digit slot can be identified by reference to a frame alignment. The frame alignment signal does not necessarily occur, in whole or in part, in each frame.

Full duplex -- A mode of operation permitting simultaneous transmission of information between two locations in both directions.

Gain – The increase in signal amplitude realized when a signal passes through an amplifier or repeater (normally measured in decibels).

Gain tracking error – The variation of gain from a constant level (determined at 0 dBm input level) when measuring the dependence of gain on signal level by comparing the output signal to the input signal over a range of input signals.

HDLC – High-Level Data Link Control; a CCITT standard data communication line protocol.

Half duplex – A mode of operation permitting transmission of information between two locations in only one direction at a time.

Handset – A rigid assembly providing both telephone transmitter and receiver in a form convenient for holding simultaneously to mouth and ear.

Hookswitch – The switch on a telephone set that is operated by the removal or replacement of the receiver on the hook (defined as off-hook and on-hook conditions, and corresponding to busy and idle circuits).

Idle channel noise (ICN) – The total signal energy measured at the output of a device or channel under test when the input of the device or channel is grounded (often a wideband noise measurement using a C-message weighting filter to band-limit the output noise).

Intermodulation – The modulation of the components of a complex wave by each other (in a nonlinear system).

Intermodulation distortion – An analog line impairment when two frequencies interact to create an erroneous frequency, in turn distorting the data signal repreentation.

ISDN – Integrated Services Digital Network; A future communication network intended to carry digitized voice and data multiplexed onto the public network.

Jitter – A type of analog communication line distortion caused by abrupt, spurious signal variation from a reference timing position, and capable of causing data transmission errors, particularly at high speeds. (The variation can be in amplitude, time, frequency or phase.)

Key system – A miniature PABX that accepts 4 to 10 lines and can direct them to as many as 30 telsets.

μ-law – A companding law accepted as the North American standard for PCM based systems.

LAN – Local Area Network; a data-only communication network between data terminals using a standard interface to the network.

Line – The portion of a circuit external to an apparatus that consists of the conductors connecting the apparatus to the exchange or connecting two exchanges.

Longitudinal balance – The common-mode rejection of a telephone circuit.

Loopback – Directing signals back toward the source at some point along a communication path.

MCU – MicroComputer Unit (also MicroController Unit).

MPU – MicroProcessor Unit.

Mu law – A companding/encoding law commonly used in U.S. (same as μ-law).

MUX – Multiplex or multiplexer.

Modem – MOdulator-DEModulator; a unit that modulates and demodulates digital information from a terminal or computer port to an analog carrier signal for passage over an analog line.

Multiplex – To simultaneously transmit two or more messages on a single channel.

Off hook – The circuit condition resulting when the handset is lifted from the hook switch of the telephone set; i.e., a low dc impedance is placed across the line causing loop current flow that is recognized by a relay at the central office as a request for service.

On hook – The circuit condition resulting when the handset of a telephone is replaced on its cradle (approximately an open circuit).

PABX – Private Automatic Branch Exchange; a customer-owned, switchable telephone system providing internal and/or external station-to-station dialing.

Pair – The two associated conductors that form part of a communication channel.

Pass-band filter – A filter used in communications systems that allows only the frequencies within a communication channel to pass, and rejects all frequencies outside the channel.

PBX – Private Branch Exchange; a class of service in standard Bell System terminology that typically provides the same service as PABX.

PCM – Pulse Code Modulation; a method of transmitting data in which signals are sampled and converted to digital words that are then transmitted serially, typically as 8-bit words.

Phase jitter – Abrupt, spurious variations in an analog line, generally caused by power and communication equipment along the line that shifts the signal phase relationship back and forth.

Propagation delay – The time interval between specified reference points on the input and output voltage waveforms.

Psophometric weighting – A frequency weighting similar to C-Message weighting that is used as the standard for European telephone system testing.

Pulse dialer – A device that generates pulse trains corresponding to digits or characters used in impulse or loop-disconnect dialing.

Quantizing noise – Signal-correlated noise generally associated with the quantizing error introduced by A/D and D/A conversions in digital transmission systems.

RTS – Request to send; an RS-232 control signal between a modem and user's digital equipment that initiates the data transmission sequence on a communication line.

Repeater – An amplifier and associated equipment used in a telephone circuit to process a signal and retransmit it.

Repertory dialer – A dialer that stores a repertory of telephone numbers and dials any one of them automatically on request.

Sampling rate – The frequency at which the amplitude of an analog signal is gated into a coder circuit. The Nyquist sampling theorem states that if a band-limited signal is sampled at regular intervals and at a rate equal to or greater than twice the highest frequency of interest, the sample contains all the information of the original signal. The frequency band of interest in telephony ranges from 300 to 3400 Hz, so a sampling rate of 8 kHz provides dc to 4000 Hz reproduction.

SCU – Subscriber Channel Unit; the circuitry at a telephone exchange associated with an individual subscriber line or channel.

Signaling – The transmission of control or status information between switching systems in the form of dedicated bits or channels of information inserted on trunks with voice data.

Signal-to-distortion ratio (S/D) – The ratio of the input signal level to the level of all components that are present when the input signal (usually a 1.020 kHz sinusoid) is eliminated from the output signal (e.g., by filtering).

SLIC – Subscriber Line Interface Circuit; a device that performs the 2-4 wire conversion, battery feed and other line interface functions on a subscriber telephone line.

Speech network – An electric circuit that connects a transmitter and a receiver to a telephone line or telephone test loop and to each other.

Subscriber line – The permanent connection between a station and the switching center that serves it.

Switchhook – A synonym for hookswitch.

Syn (Sync) – (1) A bit of character used to synchronize a time frame in a time-division multiplexer. (2) A sequence used by a synchronous modem to perform bit synchronization or by a line controller for character synchronization.

Synchronous modem – A modem that uses a derived clocking signal to perform bit synchronization with incoming data.

T1 carrier – A PCM system operating at 1.544 MHz and carrying 24 individual voice-frequency channels.

Tandem trunk – See trunk.

Telephone exchange – A switching center for interconnecting the lines that service a specific area.

TELETEX – A text communication service between entirely electronic work stations that will gradually replace TELEX with the introduction of the digital network. (Not to be confused with teletext.)

TELETEXT – The name usually used for broadcast text (and graphics) for domestic television reception. (Not to be confused with teletex.)

Time-division multiplex – A process that permits the transmission of two or more signals over a common paty by using a different time interval for each signal.

Tip (T) and ring (R) – Terms used to identify the two conductors of a circuit. (These terms originate from switchboard terminology for cord circuits, in which a four-wire circuit is designated T1, T2, and R1 and R2.)

Trunk – A telephone circuit or channel between two central offices or switching entities.

TSAC – Time Slot Assigner Circuit; a circuit that determines when a CODEC will put its 8 bits of data on a PCM bit stream.

TSIC – Time Slot Interchange Circuit; a device that switches digital highways in PCM based switching systems; a "digital" cross-point switch.

Twist – The amplitude ratio of a pair of DTMF tones. (Because of transmission and equipment variations, a pair of tones that originated equal in amplitude may arrive with a considerable difference in amplitude.)

UDLT – Universal Digital Loop Transceiver; a Motorola originated name for a voice/data transceiver circuit.

Voice frequency – A frequency within that part of the audio range that is used for the transmission of speech of commercial quality, i.e. 300-3400 Hz.

Weighting network – A network whose loss varies with frequency in a predetermined manner.

5

Handling and Design Guidelines

6

MOTOROLA

HANDLING AND DESIGN GUIDELINES

HANDLING PRECAUTIONS

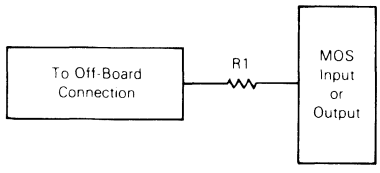
All MOS devices have an insulated gate that is subject to voltage breakdown. The gate oxide for Motorola's devices is about 800 Å thick and breaks down at a gate-source potential of about 100 V. The high-impedance gates on the devices are protected by resistor-diode networks. However, these on-chip networks do not make the IC immune to electrostatic damage (ESD). Laboratory tests show that devices may fail after one very high voltage discharge. They may also fail due to the cumulative effect of several discharges of lower potential.

Static-damaged devices behave in various ways, depending on the severity of the damage. The most severely damaged are the easiest to detect because the input or output has been completely destroyed and is either shorted to V_{DD}, shorted to V_{SS}, or open-circuited. The effect is that the device is no longer functional. Less severe cases are more difficult to detect because they appear as intermittent failures or degraded performance. Another effect of static damage is, often, increased leakage currents.

CMOS and NMOS devices are not immune to large static voltage discharges that can be generated while handling. For example, static voltages generated by a person walking across a waxed floor have been measured in the 4-15 kV range (depending on humidity, surface conditions, etc.). Therefore, the following precautions should be observed.

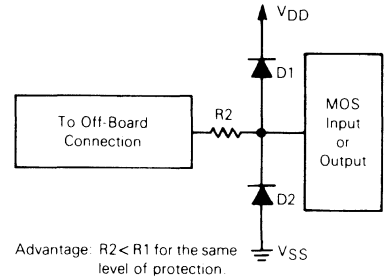
1. Do not exceed the Maximum Ratings specified by the data sheet.
2. All unused device inputs should be connected to V_{DD} or V_{SS}.
3. All low-impedance equipment (pulse generators, etc.) should be connected to CMOS or NMOS inputs only after the device is powered up. Similarly, this type of equipment should be disconnected before power is turned off.
4. A circuit board containing CMOS or NMOS devices is merely an extension of the device and the same handling precautions apply. Contacting edge connectors wired directly to devices can cause damage. Plastic wrapping should be avoided. When external connections to a PC board address pins of CMOS or NMOS integrated circuits, a resistor should be used in series with the inputs or outputs. The limiting factor for the series resistor is the added delay caused by the time constant formed by the series resistor and input capacitance. This resistor will help limit accidental damage if the PC board is removed and brought into contact with static generating materials. For convenience, equations for added propagation delay and rise time effects due to series resistance size are given in Figure 1.
5. All CMOS or NMOS devices should be stored or

FIGURE 1 — NETWORKS FOR MINIMIZING ESD AND REDUCING CMOS LATCH UP SUSCEPTIBILITY



Advantage: Requires minimal board area

Disadvantage: R1 > R2 for the same level of protection, therefore rise and fall times, propagation delays, and output drives are severely affected.



Advantage: R2 < R1 for the same level of protection. Impact on ac and dc characteristics is minimized.

Disadvantage: More board area, higher initial cost

Note: These networks are useful for protecting the following:
A. digital inputs and outputs
B. analog inputs and outputs
C. 3-state outputs
D. bidirectional (I/O) ports

EQUATION 1 — PROPAGATION DELAY vs. SERIES RESISTANCE

$$R \approx \frac{t}{C \bullet k}$$

where:
R = the maximum allowable series resistance in ohms
t = the maximum tolerable propagation delay in seconds
C = the board capacitance plus the driven device's input capacitance in farads
k = 0.33 for the MC145040/1
k = 0.7 for other devices

EQUATION 2 — RISE TIME vs. SERIES RESISTANCE

$$R \approx \frac{t}{C \bullet k}$$

where:
R = the maximum allowable series resistance in ohms
t = the maximum rise time per data sheet in seconds
C = the board capacitance plus the driven device's input capacitance in farads
k = 0.7 for the MC145040/1
k = 2.3 for other devices

transported in materials that are antistatic. Devices must not be inserted into conventional plastic "snow", styrofoam or plastic trays, but should be left in their original container until ready for use.

6. All CMOS or NMOS devices should be placed on a grounded bench surface and operators should ground themselves prior to handling devices, since a worker can be statically charged with respect to the bench surface. Wrist straps in contact with skin are strongly recommended. See Figure 2.
7. Nylon or other static generating materials should not come in contact with CMOS or NMOS circuits.
8. If automatic handling is being used, high levels of static electricity may be generated by the movement of devices, belts, or boards. Reduce static build-up by using ionized air blowers or room humidifiers. All parts of machines which come into contact with the top, bottom, and sides of IC packages must be grounded metal or other conductive material.
9. Cold chambers using CO_2 for cooling should be equipped with baffles, and devices must be contained on or in conductive material.
10. When lead-straightening or hand-soldering is necessary, provide ground straps for the apparatus used and be sure that soldering ties are grounded.
11. The following steps should be observed during wave solder operations.
    a. The solder pot and conductive conveyor system of the wave soldering machine must be grounded to an earth ground.
    b. The loading and unloading work benches should have conductive tops which are grounded to an earth ground.
    c. Operators must comply with precautions previously explained.
    d. Completed assemblies should be placed in antistatic containers prior to being moved to subsequent stations.
12. The following steps should be observed during board cleaning operation.
    a. Vapor degreasers and baskets must be grounded to an earth ground. Operators must likewise be grounded.
    b. Brush or spray cleaning should not be used.
    c. Assemblies should be placed into the vapor degreaser immediately upon removal from the antistatic container.
    d. Cleaned assemblies should be placed in antistatic containers immediately after removal from the cleaning basket.
    e. High velocity air movement or application of solvents and coatings should be employed only when module circuits are grounded and a static eliminator is directed at the module.
13. The use of static detection meters for line surveillance is highly recommended.
14. Equipment specifications should alert users to the presence of CMOS or NMOS devices and require familiarization with this specification prior to performing any kind of maintenance or replacement of devices or modules.
15. Do not insert or remove CMOS or NMOS devices from test sockets with power applied. Check all power supplies to be used for testing devices to be certain there are no voltage transients present.
16. Double check test equipment setup for proper polarity of voltage before conducting parametric or functional testing.
17. Do not recycle shipping rails. Continuous use causes deterioration of their antistatic coating.

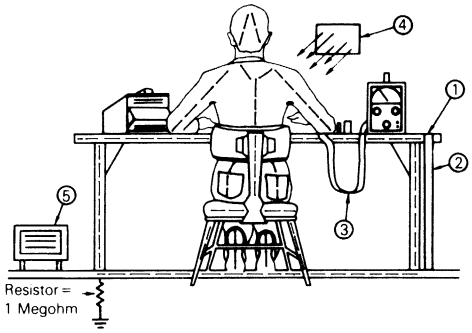
RECOMMENDED FOR READING

"Total Control of the Static in Your Business"

Available by writing to:
Static Control Systems Div.
Box ELB-3, 225-4S
3M Center
St. Paul, MN 55144

Or calling:
1-800-328-1368
1-612-733-9420 (in Minnesota)

FIGURE 2 — TYPICAL MANUFACTURING WORK STATION



NOTES: 1. 1/16 inch conductive sheet stock covering bench top work area.
2. Ground strap.
3. Wrist strap in contact with skin.
4. Static neutralizer. (Ionized air blower directed at work.) Primarily for use in areas where direct grounding is impractical.
5. Room humidifier. Primarily for use in areas where the relative humidity is less than 45%. Caution: building heating and cooling systems usually dry the air causing the relative humidity inside of buildings to be less than outside humidity.

CMOS LATCH UP

Latch up will not be a problem for most designs, but the designer should be aware of it, what causes it, and how to prevent it.

Figure 3 shows the layout of a typical CMOS inverter and Figure 4 shows the parasitic bipolar devices that are formed. The circuit formed by the parasitic transistors and resistors is the basic configuration of a silicon controlled rectifier, or SCR. In the latch-up condition, transistors Q1 and Q2 are turned on, each providing the base current necessary for the other to remain in saturation, thereby latching the devices on. Unlike a conventional SCR, where the device is turned on by applying a voltage to the base of the NPN transistor, the parasitic SCR is turned on by applying a voltage to the emitter of either transistor. The two emitters that trigger the SCR are the same point, the CMOS output. Therefore, to latch up the CMOS device, the output voltage must be greater than V_{DD} + 0.5 Vdc or less than − 0.5 Vdc and have sufficient current to trigger the SCR. The latch-up mechanism is similar for the inputs.

Once a CMOS device is latched up, if the supply current is not limited, the device will be destroyed. Ways to prevent such occurrences are listed below.

1. Insure that inputs and outputs are limited to the maximum rated values, as follows:
   $-0.5 \le V_{in} \le V_{DD} + 0.5$ Vdc referenced to V_{SS}
   $-0.5 \le V_{out} \le V_{DD} + 0.5$ Vdc referenced to V_{SS}
   $|I_{in}| \le 10$ mA
   $|I_{out}| \le 10$ mA when transients or dc levels exceed the supply voltages.
2. If voltage transients of sufficient energy to latch up the device are expected on the outputs, external protection diodes can be used to clamp the voltage. Another method of protection is to use a series resistor to limit the expected worst case current to the Maximum Ratings values. See Figure 1.
3. If voltage transients are expected on the inputs, protection diodes may be used to clamp the voltage or a series resistor may be used to limit the current to a level less than the maximum rating of I_{in} = 10 mA. See Figure 1.
4. Sequence power supplies so that the inputs or outputs of CMOS devices are not powered up first (e.g., recessed edge connectors may be used in plug-in board applications and/or series resistors).
5. Power supply lines should be free of excessive noise. Care in board layout and filtering should be used.
6. Limit the available power supply current to the devices that are subject to latch-up conditions. This can be accomplished with the power supply filtering network or with a current-limiting regulator.

FIGURE 3 – CMOS WAFER CROSS SECTION

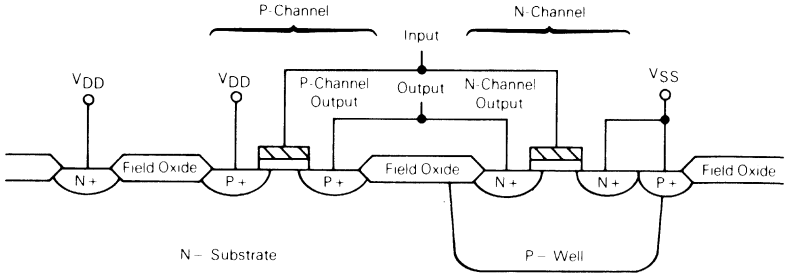
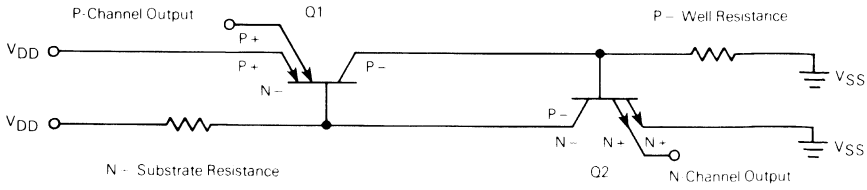


FIGURE 4 – LATCH UP CIRCUIT SCHEMATIC



Quality and Reliability 7

MOTOROLA QUALITY & RELIABILITY ASSURANCE

Analog Integrated Circuits

Aiming for the bottom line in component quality. . .

MOTOROLA

Are you buying a sure thing?

What do you consider—in addition to price and function—when buying a product? You probably need to know how well and how long you can expect it to work. But product dependability can be difficult to assess:

- How do you know that a company is doing all that's necessary to ensure the quality and reliability of its products?
- How do you measure the results—and what is the company's track record?

At Motorola we're proud of our quality and reliability record, and we want you to understand and share our confidence in Motorola products. That's why we are introducing you to

Our dynamic and supportive corporate quality policy

Programs that have been instrumental in our quality and reliability success

Recent quality/reliability achievements and goals for the future

—so you will know what else you're buying when you buy Motorola.

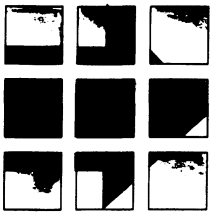
"It is the policy of the Motorola Semiconductor Products Sector to produce products and provide services exactly according to specifications and delivery schedule. The system will be based on prevention using statistical process control. ***The standard will be error-free performance.*** *These results will be derived from the participative efforts of each employee in conjunction with supportive participation from all levels of management."*

James A. Norling
Executive Vice President
General Manager
Semiconductor Products Sector

Tommy George
Senior Vice President
Assistant General Manager
Semiconductor Products Sector

. . . Zero Defects

7



GOING BEYOND THE MOTTO
Motorola Quality Policy

"Dedication to quality" has a nice ring to it, but as a working concept it must encompass far more than fine-sounding rhetoric. To realize our quality goals at Motorola, we first had to formulate a quality policy capable of serving as a framework for an aggressive, ongoing improvement program.

Policy Goals

The highest possible level of quality—in concrete, measureable terms—is Motorola's goal for its products and services. We approach this goal through the combined efforts of dedicated employees and active, supportive management at all levels of the corporation.

Implementing the Policy

Motorola distributes quality responsibility throughout the company. Every sector, group, division, and business unit is charged with . . .

- Developing its own **supportive policies**
- Establishing and maintaining **regular programs** to improve product quality, reliability, and service
- Directing these programs toward **all phases** of its business
- Targeting a **ten-fold improvement** in measureable quality and reliability criteria over each five-year period

Features

Some standout features of our quality policy:

QA as Customer Advocate

Individual Quality Assurance groups are directed to perform as customer advocates; their organizational independence allows them to function from that perspective.

Targeting the Problem Causes

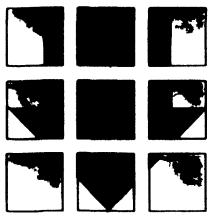
Every Motorola sector, group, division, and business unit designs its own formal processes to improve quality and reliability; each of these processes features a constant search for new ways of identifying and eliminating problem causes.

Assigned Responsibility; Regular Reviews

As part of its quality plan, each of these groups installs and documents a system detailing responsibility for executing the plan. To ensure continuing effectiveness, Motorola performs periodic reviews of the system, without exception.

Company-Wide Coordination

To ensure achievement of quality goals, Motorola maintains a Corporate Quality Council to oversee the company-wide coordination, promotion, and review of all quality systems and programs.



FORCING DOWN THE BOTTOM LINE
Three Programs for Excellence

Improve quality by an order of magnitude every five years. To achieve this ever tighter goal, we need aggressive improvement programs geared to every aspect of the manufacturing process. The following programs focus on three areas of particular importance—maintaining raw material quality, monitoring of statistics during manufacturing, and driving down the defect rate.

Vendor Improvement Plan

Built-in quality requires starting out with the best materials possible. To ensure the quality of incoming raw materials, we work with our vendors to verify:

- Mutual understanding of Motorola quality requirements
- Correlation between the outgoing (vendor) and incoming (Motorola) quality requirements and statistics

Once we certify a vendor under this plan, we can eliminate redundant testing after receipt of goods—thereby reducing time and costs associated with the parts while maintaining the quality.

Statistical Quality Control (SQC)

From design through finished product, the quality control sciences keep us manufacturing within Motorola standards:

Control charts monitor and plot the output of the wafer fabrication process, ensuring immediate response to undesirable situations. Charts used are from J. M. Juran's *Quality Control Handbook* (McGraw-Hill, 1974).

Advanced diagnostic techniques let us control certain variables that affect product quality. Statistical tools include multi-vari charts, randomization, factorials, and control techniques.

Planned experimentation explores relationships between variables, focusing on the effects of altering variables. Methods include analysis of data from component and variable search patterns and from full and fractional factorial experiments.

Pareto analysis rates proposed changes on a need/cost basis.

Control of yield variation. A continuous stream of yield variation data is provided during final test; equipment shutdown results if variation exceeds control limits.

No test of rejects (NTR). Parts rejected at final test are removed at once and not given a second chance to pass. (To carry out the NTR program with confidence, Motorola conducts regular qualification testing of products, test programs, test equipment, and operators.)

Our manufacturing process consists of a series of small, discrete operations that are continually tested and measured using these and other SQC tools. Resulting statistics are compared with control figures to identify non-random variations and determine when a change is needed.

Zero Defects Program

A corporate mandate to push down the defect rate prompted us to develop our own version of an established industry concept. Motorola's Zero Defects Program includes the following assorted processes:

Quality system procedures reinforcement. To ensure adherence to the procedures detailed in Motorola's *Quality Systems* manual, regular audits are conducted at several levels of the Quality and Reliability Assurance organizations.

In-line gating. This cooperative testing effort between Production and Quality Assurance:

- Fosters communication and shared responsibility
- Cuts down cycle time and cost

Sample testing, formerly done by QA alone, is now done by QA and Production—working together—before a lot leaves the production area. Recent quality improvement statistics (corrective actions, percent lot rejects, AOQ defects, and Return Material Requests) attest to the success of the shared effort.

ESD audits. Changes in fabrication technology have increased electrostatic discharge (ESD) sensitivity in many products. Product design, handling, and packaging must improve to accommodate ESD concerns. Motorola's ESD program monitors handling and packaging practices and identifies possible problems and improvements.

- Motorola is committed to designing ESD performance improvements directly into its products.
- Motorola's ESD-safe workstations protect devices from damage during manufacturing.
- Several levels of ESD-protective packaging ensure safe product transport and non-contamination of customers' static-free work areas.

Organizational quality meetings. Meetings are held monthly at operational, divisional, and group levels to:

- Review quality methods and goals
- Improve quality feedback
- Identify high-AOQ devices

Manufacturing quality involvement teams. Volunteers representing a cross-section of manufacturing meet to exchange information and work through problems.

Corrective action procedure. A part defect found at the wafer area, at assembly, or at final test triggers a corrective action request (CAR) that documents the problem in detail, complete with recommendations. The CAR is issued to the corresponding product group and serves as a prompt to resolve action items.

Statistical quality control. Functioning as part of the Zero Defects Program, SQC (described above) provides a regulating force to keep manufacturing and testing processes operating within prescribed standards.

Quality Bonus—New Return Policy Benefits OEMs

In early 1986, Motorola announced a major change in its return policy for **OEM quality-related product returns.** Under the new policy, semiconductor products found defective and returned to Motorola within 45 days of the shipment date will be accepted with **no questions asked.**

The "no questions asked" return policy reflects our growing confidence in the quality of Motorola products. Our quality improvement program has been so successful, as borne out by recent statistics, that we no longer see the need for acceptance quality level (AQL) stipulations regarding quality-related defects.

The new policy also reflects our wish to channel our success into a plan that will better serve our customers—and make dealing with Motorola even easier.

MEASURING UP
Yardsticks for Success

How do Motorola's quality efforts translate into achievement?

Product perfection, as the ultimate objective, is still in the future. But product excellence—the result of keeping pace with the deliberately aggressive goals that serve as major milestones—is not. We can offer you excellence today, as we show below.

Motorola measures overall product dependability in two ways. *Quality*, the physical status of a device at final test, is measured in terms of the AOQ (average outgoing quality) defect rate. *Reliability*, the long-term useful life projection based on statistics, is currently rated on the four different indices that make up the Reliability Monitor Program: operating life, temperature/humidity/bias, autoclave, and temperature cycling/thermal shock.

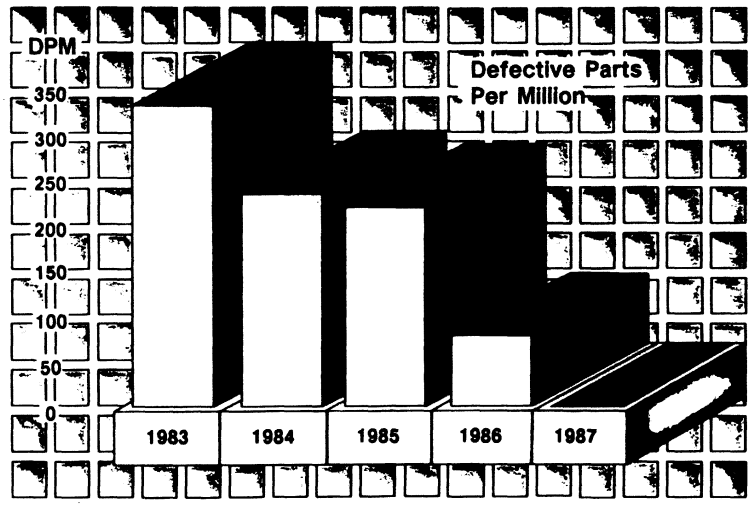
Consistent improvement in both quality and reliability marks another reason to turn to Motorola with confidence.

The Measure of Quality

Average outgoing quality has improved steadily over the last few years—despite increasing product complexity, changing technologies, and rapid introduction of new products.

Product lots slated for shipment are sampled for both electrical and visual/mechanical inspection. These AOQ figures show the declining defect rate (measured in defective parts per million, or PPM) for both criteria.

Motorola participates in the "Ship to Stock" product certification program (under which customers bypass incoming inspection) with many customers. The success of this program reflects the tightened PPM quality made possible by ongoing improvement programs in Wafer Fab, Assembly, and Final Test.



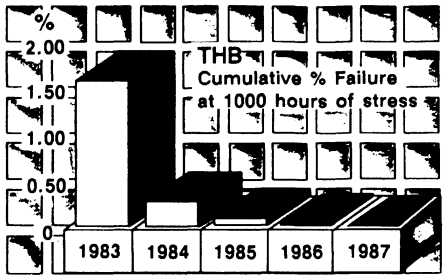
Electrical Average Outgoing Quality. Five-year summary of electrical performance measurements–actual and projected.

Reliability Monitor Program

Samples are pulled weekly from the generic product families and run through all appropriate reliability tests. The test results are continually fed into a database, identifying problem areas and spurring corrective action. At present, the Reliability Monitor program consists of four tests:

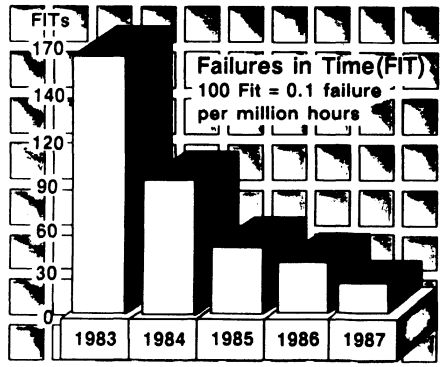
Temperature/Humidity/Bias (THB). An environmental test that determines moisture resistance of, and moisture-related effects on, plastic-packaged devices. Tests run for 1008 hours at 85°C with a relative humidity of 85 percent. Static voltage bias (applied to accelerate metal corrosion) is 5.0 V for high-speed devices and 15.0 V for metal-gate devices. Test is performed per JEDEC Standard 22, Method A101

Results. Improved THB performance enables plastic-encapsulated ICs to survive harsh environments. THB statistics for BIP & MOS Analog products continue to improve as we experiment with different mold components, tighten process controls, and further automate assembly facilities.



High-Temperature Operating Life. A tool to predict the failure rate, based on the Arrhenius equation for chemical relationships. Applies extreme temperature under static conditions to accelerate thermally activated failure. Tests run for a minimum of 1008 hours at 125°C; voltage bias level is 5.0 for high-speed logic devices and 15.0 for metal-gate devices. Test is performed per MIL-STD-883, Method 1005.

Results. Improvement has exceeded expectations, largely as a result of improved equipment and techniques in both Water Fabrication and Assembly. Goals shown reflect the extremely high reliability now demanded in the market.



Autoclave. A highly accelerated, destructive environmental test that measures device resistance to moisture penetrating the leadframe/plastic interface. Test is run for 240 hours at 121°C with 100 percent relative humidity and 15 psi.

Temperature Cycling and Thermal Shock. Accelerates the thermal expansion mismatch that ensues when different components of a package expand at different rates. Devices are subjected to extreme low and then extreme high temperatures for 1000 low/high cycles. Test is performed per MIL-STD-883, Methods 1010 and 1011, Condition C (−65°C to +150°C), or JEDEC Standard 22, Method A104 (−40°C to +125°C).

At the end of each quarter, Motorola compiles and publishes these test results as a service to customers. For information on receiving the quarterly *Reliability Report*, please contact your local Motorola representative.

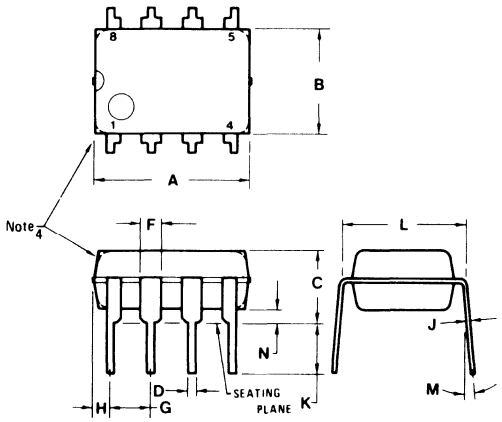
Mechanical Data 8

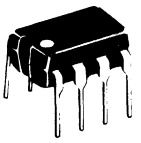
MECHANICAL DATA

The package availability for each device is indicated on the front page of the individual data sheets. Dimensions for the packages are given in this chapter.

8-PIN PACKAGE

P SUFFIX
PLASTIC PACKAGE
CASE 626-04





NOTES:
1. LEAD POSITIONAL TOLERANCE:
   ⌖ Ø 0.13 (0.005) Ⓜ | T | A Ⓜ | B Ⓜ
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
4. DIMENSIONS A AND B ARE DATUMS.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC - IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. VCC

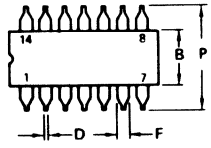
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	–	10^0	–	10^0
N	0.51	0.76	0.020	0.030

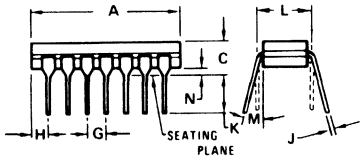
8

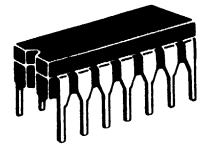
MECHANICAL DATA (Continued)

14-PIN PACKAGES

L SUFFIX
CERAMIC PACKAGE
CASE 632-07



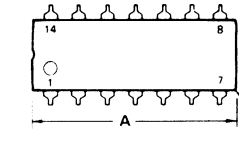


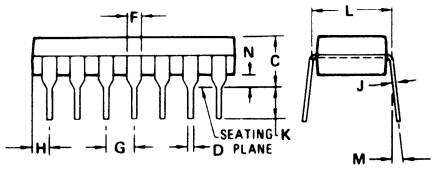


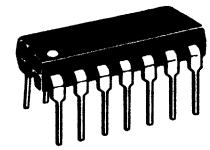
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.10	7.49	0.240	0.295
C	–	5.08	–	0.200
D	0.38	0.58	0.015	0.023
F	1.40	1.77	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	1.91	2.29	0.075	0.090
J	0.20	0.38	0.008	0.015
K	3.18	4.32	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH MO-001 AA OUTLINE SHALL APPLY.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "A" AND "B" (632-07) DO NOT INCLUDE GLASS RUN-OUT.
4. LEADS WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT SEATING PLANE AND MAXIMUM MATERIAL CONDITION.

P SUFFIX
PLASTIC PACKAGE
CASE 646-05





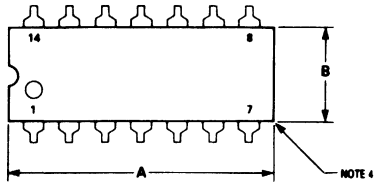


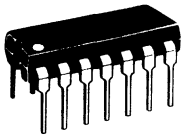
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

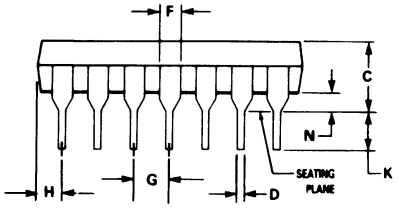
NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

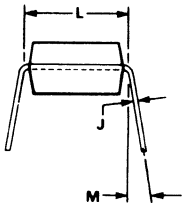
14-PIN PACKAGES

P SUFFIX
PLASTIC PACKAGE
CASE 646-06
$R_{\theta JA}$ = 100°C/W









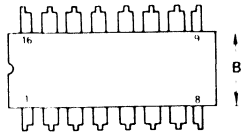
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.39	1.01	0.015	0.39

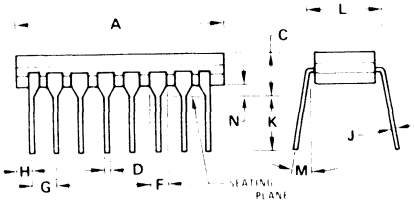
NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL; AS SHOWN IN PREVIOUS ISSUE.

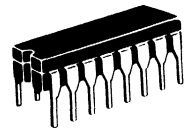
MECHANICAL DATA (Continued)

16-PIN PACKAGES

L SUFFIX
CERAMIC PACKAGE
CASE 620-08



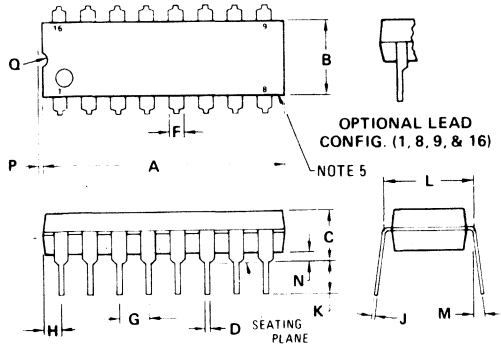


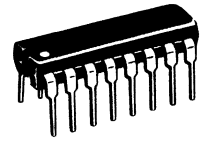


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.10	7.49	0.240	0.295
C	–	5.08	–	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. PACKAGE INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT
3. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIM "A" AND "B" DO NOT INCLUDE GLASS RUN OUT.
5. DIM "F" MAY NARROW TO 0.76 mm (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

P SUFFIX
PLASTIC PACKAGE
CASE 648-05



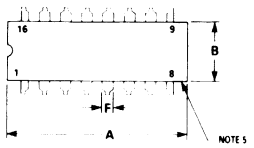


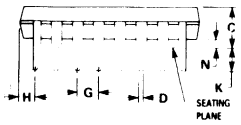
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	21.34	0.740	0.840
B	6.10	6.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.38	2.41	0.015	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

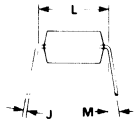
NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 8, 9, and 16).
5. ROUNDED CORNERS OPTIONAL.

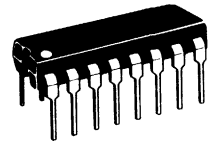
16-PIN PACKAGES

P SUFFIX
PLASTIC
CASE 648-06









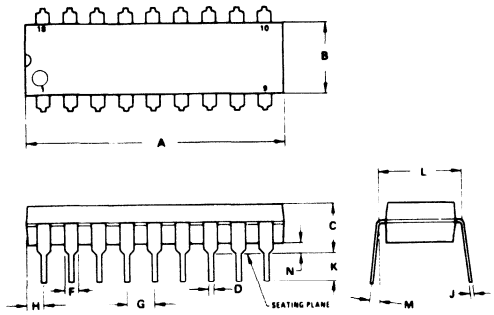
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	21.34	0.740	0.840
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.38	2.41	0.015	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.39	1.01	0.015	0.040

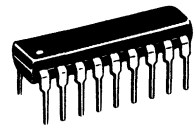
NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. "F" DIMENSION IS FOR FULL LEADS.
5. ROUNDED CORNERS OPTIONAL.

MECHANICAL DATA (Continued)

18-PIN PACKAGES

P SUFFIX
PLASTIC PACKAGE
CASE 707-02

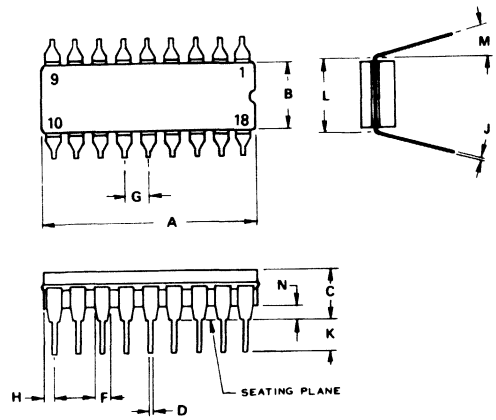


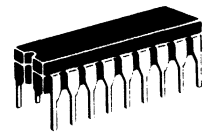


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

L SUFFIX
CERAMIC PACKAGE
CASE 726-04





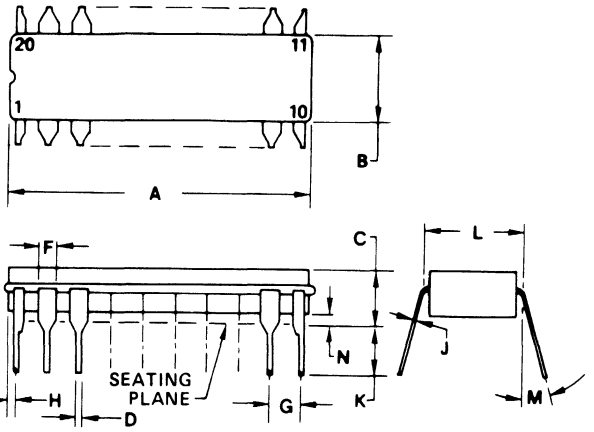
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.35	23.11	0.880	0.910
B	6.10	7.49	0.240	0.295
C	–	5.08	–	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

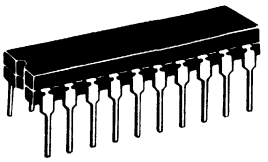
NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA. AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM "A" & "B" INCLUDES MENISCUS.

8

20-PIN PACKAGES

L SUFFIX
CERAMIC PACKAGE
CASE 732-03

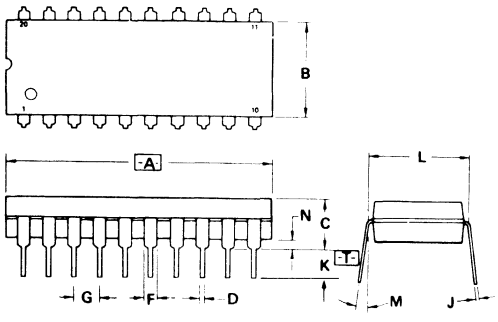


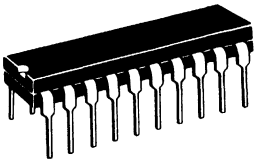


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	23.88	25.15	0.940	0.990
B	6.60	7.49	0.260	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.25	1.02	0.010	0.040

NOTES:
1. LEADS WITHIN 0.25 mm (0.010) DIA, TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM A AND B INCLUDES MENISCUS.

P SUFFIX
PLASTIC PACKAGE
CASE 738-02





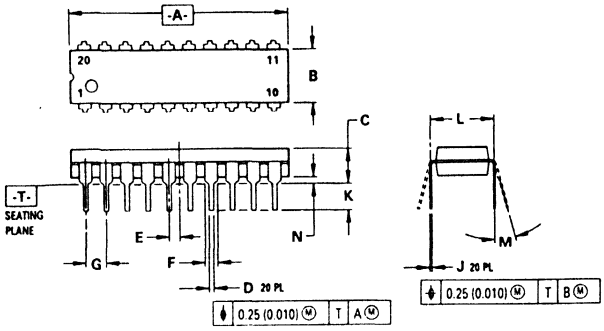
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	25.65	27.18	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.94	4.57	0.155	0.180
D	0.38	0.56	0.015	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.20	0.38	0.008	0.015
K	2.79	3.56	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

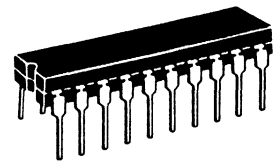
NOTES:
1. DIM -A- IS DATUM.
2. POSITIONAL TOL FOR LEADS; ⌖ Ø 0.25 (0.010)Ⓜ T A Ⓜ
3. -T- IS SEATING PLANE.
4. DIM "B" DOES NOT INCLUDE MOLD FLASH.
5. DIM -L- TO CENTER OF LEADS WHEN FORMED PARALLEL.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

8

20-PIN PACKAGES

P SUFFIX
PLASTIC PACKAGE
CASE 738-03



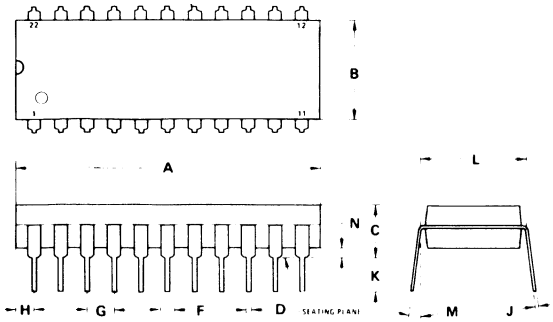


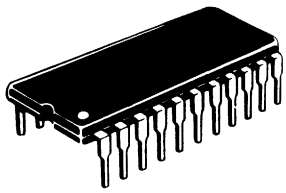
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	25.66	27.17	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.81	4.57	0.150	0.180
D	0.39	0.55	0.015	0.022
E	1.27 BSC		0.050 BSC	
F	1.27	1.77	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.

22-PIN PACKAGES

P SUFFIX
PLASTIC PACKAGE
CASE 708-04

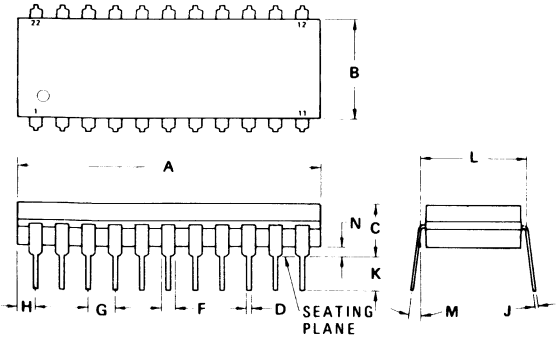


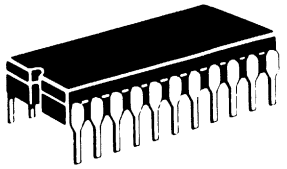


NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	27.56	28.32	1.085	1.115
B	8.64	9.14	0.340	0.360
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	10.16 BSC		0.400 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

L SUFFIX
CERAMIC PACKAGE
CASE 736-03





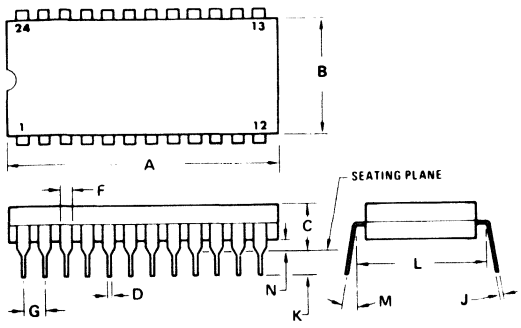
NOTES:
1. LEADS TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (DIM "D").
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

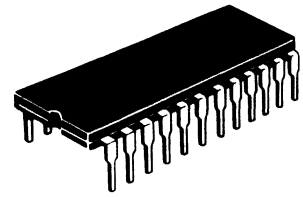
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	26.80	27.81	1.055	1.095
B	9.14	9.91	0.360	0.390
C	3.81	5.46	0.150	0.215
D	0.38	0.53	0.015	0.021
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	9.91	10.41	0.390	0.410
M	–	15°	–	15°
N	0.25	0.89	0.010	0.035

8

24-PIN PACKAGES

L SUFFIX
CERAMIC PACKAGE
CASE 623-05

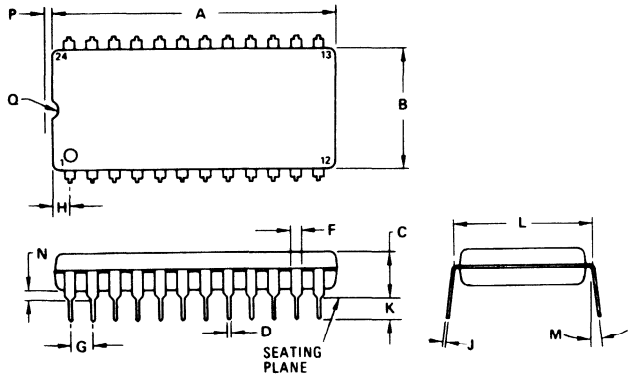


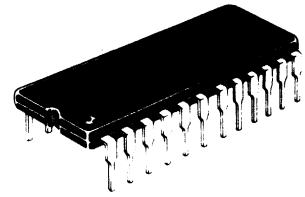


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL).

P SUFFIX
PLASTIC PACKAGE
CASE 649-03



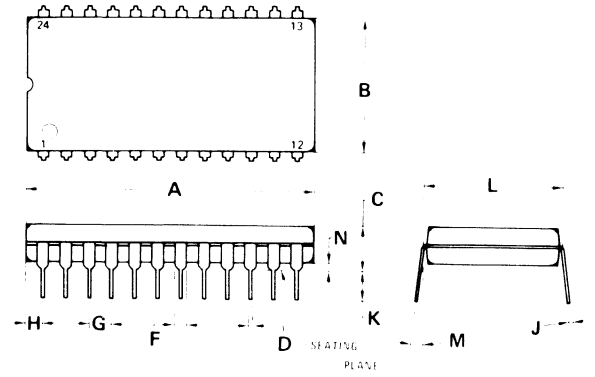


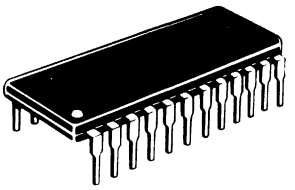
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.50	32.13	1.240	1.265
B	13.21	13.72	0.520	0.540
C	4.70	5.21	0.185	0.205
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	14.99	15.49	0.590	0.610
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

24-PIN PACKAGES (Continued)

P SUFFIX
PLASTIC PACKAGE
CASE 709-02





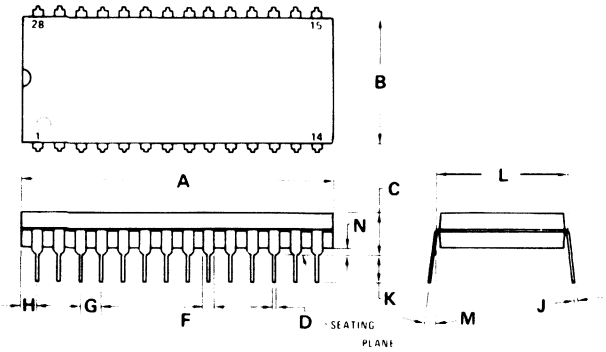
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.03	0.065	0.080
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

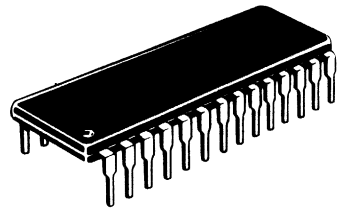
NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

8

28-PIN PACKAGES

P SUFFIX
PLASTIC PACKAGE
CASE 710-02





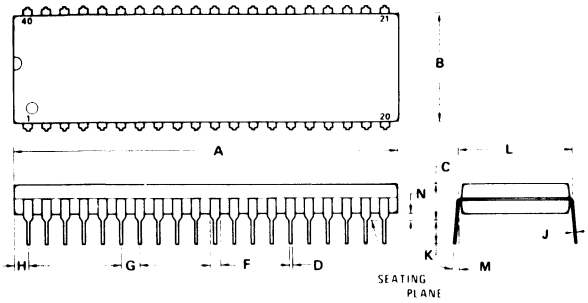
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

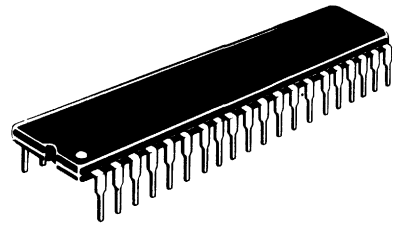
NOTES:

1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

40-PIN PACKAGES

P SUFFIX
PLASTIC PACKAGE
CASE 711-03





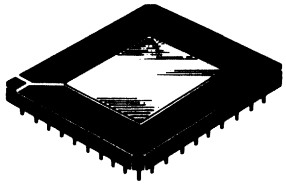
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0^0	15^0	0^0	15^0
N	0.51	1.02	0.020	0.040

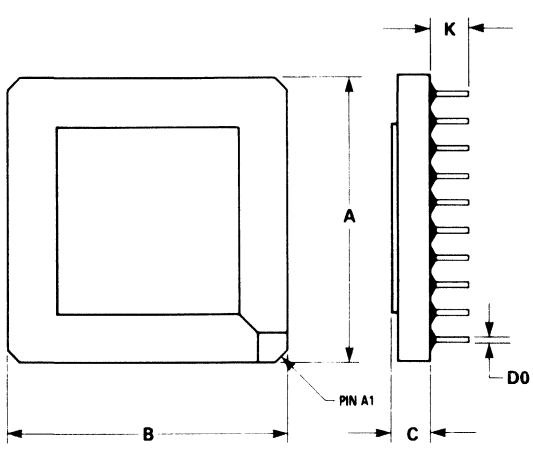
NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

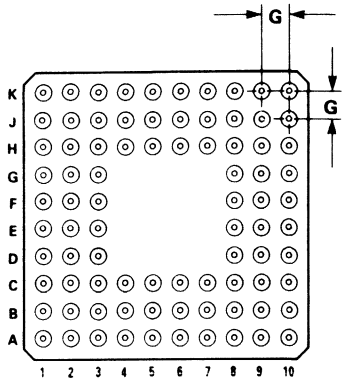
8

MECHANICAL DATA (Continued)

RC SUFFIX
PIN GRID ARRAY
(84 PIN)
CASE 793







NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. POSITIONAL TOLERANCE FOR LEADS: (84 PL)

⌖	ϕ 0.13 (0.005) Ⓛ	T	A Ⓢ	B Ⓢ

3. DIMENSIONING AND TOLERANCING PER Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	27.43	—	1.080
B	—	27.43	—	1.080
C	2.03	2.67	0.080	0.105
D	0.43	0.61	0.017	0.024
G	2.54 BSC		0.100 BSC	
K	3.56	4.95	0.140	0.195

8

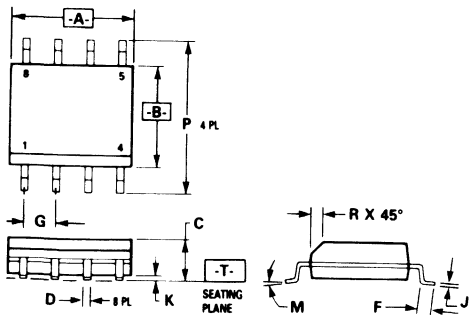
Integrated Circuit Package Dimensions

NOTE: Several versions of each package are in production (for example 751A-01 and 751A-02) with small dimensional variations.

The following pages show a representative example of each package. For precise details of any package please contact your local **MOTOROLA** representative.

CASE 751

SO-8

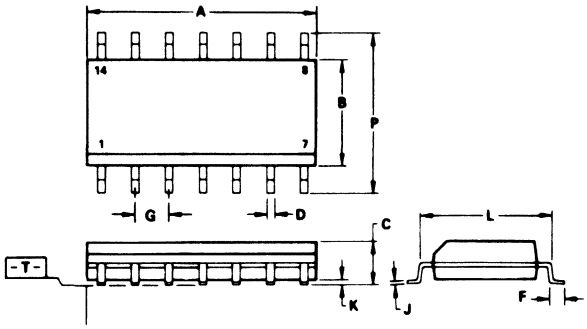


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. POSITIONAL TOLERANCE FOR D DIMENSION (8 PLACES):
   ⌖ | 0.25 (0.010) Ⓜ | T | B Ⓢ | A Ⓢ
3. POSITIONAL TOLERANCE FOR P DIMENSION (4 PLACES):
   ⌖ | 0.25 (0.010) Ⓜ | B Ⓜ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: MILLIMETER.
6. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
7. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

SO-14

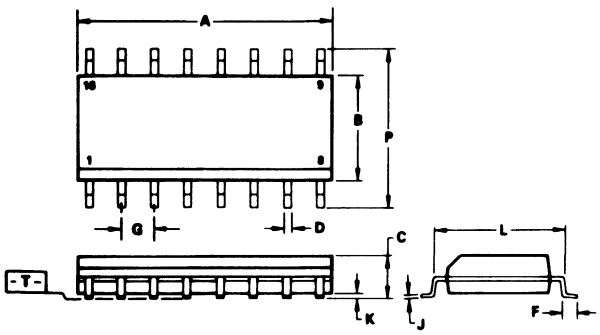
CASE 751A



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.54	8.74	0.336	0.344
B	3.81	4.01	0.150	0.158
C	1.35	1.75	0.053	0.069
D	0.35	0.46	0.014	0.018
F	0.67	0.77	0.026	0.030
G	1.27 BSC		0.050 BSC	
J	0.19	0.22	0.007	0.009
K	0.10	0.20	0.004	0.008
L	4.82	5.21	0.189	0.205
P	5.79	6.20	0.228	0.244

SO-16

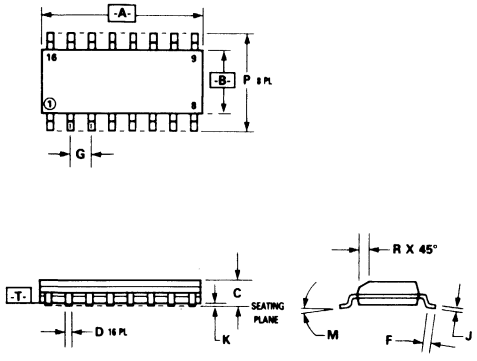
CASE 751B



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.78	10.01	0.385	0.394
B	3.81	4.01	0.150	0.158
C	1.35	1.75	0.053	0.069
D	0.35	0.46	0.014	0.018
F	0.67	0.77	0.026	0.030
G	1.27 BSC		0.050 BSC	
J	0.19	0.22	0.007	0.009
K	0.10	0.20	0.004	0.008
L	4.82	5.21	0.189	0.205
P	5.79	6.20	0.228	0.244

SO-16L (WIDE)

CASE 751G

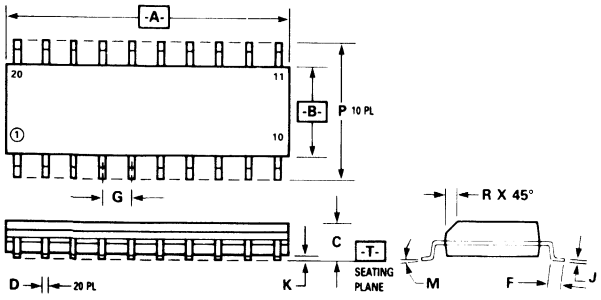


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
	0.25	0.75	0.010	0.029

NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. POSITIONAL TOLERANCE FOR D DIMENSION (16 PLACES):
   ⌖ | 0.25 (0.010) Ⓜ | T | B Ⓢ | A Ⓢ
3. POSITIONAL TOLERANCE FOR P DIMENSION (8 PLACES):
   ⌖ | 0.25 (0.010) Ⓜ | B Ⓜ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: MILLIMETER.
6. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
7. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

SO-20L (WIDE)

CASE 751D



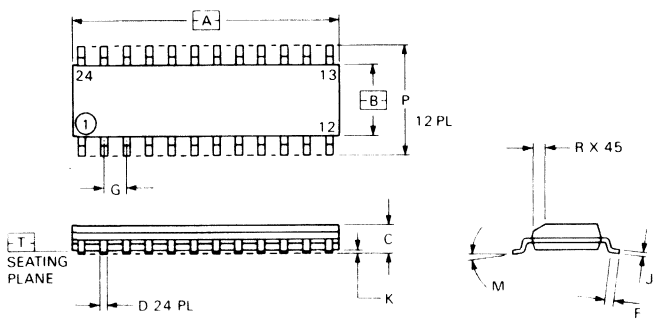
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.65	12.95	0.499	0.509
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. POSITIONAL TOLERANCE FOR D DIMENSION (20 PLACES):
   ⌖ | 0.25 (0.010) Ⓜ | T | B Ⓢ | A Ⓢ
3. POSITIONAL TOLERANCE FOR P DIMENSION (10 PLACES):
   ⌖ | 0.25 (0.010) Ⓜ | B Ⓜ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: MILLIMETER.
6. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
7. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

8

SO-24L (WIDE)

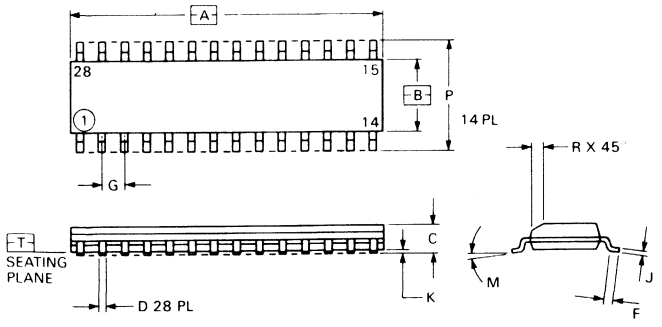
CASE 751E



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.25	15.50	0.601	0.610
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

SO-28L (WIDE)

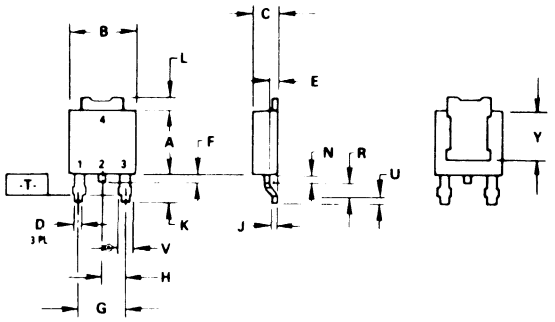
CASE 751F



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	17.80	18.05	0.701	0.710
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

DPAK

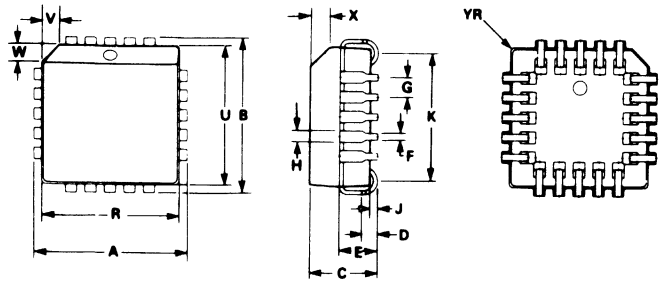
CASE 369A



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.19	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.18	2.38	0.086	0.094
D	0.69	0.88	0.027	0.035
E	0.89	1.14	0.035	0.045
F	0.64	0.88	0.025	0.035
G	4.57 BSC		0.180 BSC	
H	2.87 BSC		0.090 BSC	
J	0.46	0.58	0.018	0.023
K	2.59	2.89	0.102	0.114
L	0.89	1.27	0.035	0.050
N	0.81	1.11	0.032	0.044
R	1.07	1.37	0.042	0.054
S	5.21	5.46	0.205	0.215
U	0.51	—	0.020	—
V	0.76	1.14	0.030	0.045
W	0.48	0.55	0.019	0.022
Y	4.32	—	0.170	—

PLCC-20

CASE 775

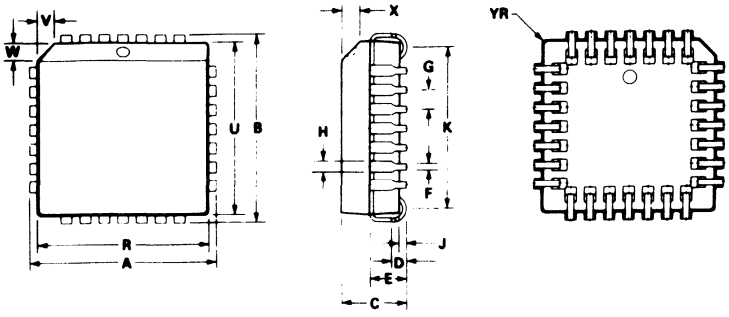


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.78	10.02	0.385	0.395
B	9.78	10.02	0.385	0.395
C	4.19	4.57	0.165	0.180
D	0.64	1.01	0.025	0.040
E	2.16	2.79	0.085	0.110
F	0.33	0.53	0.013	0.021
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.38	0.63	0.015	0.025
K	7.37	8.38	0.290	0.330
R	8.89	9.04	0.350	0.356
U	8.89	9.04	0.350	0.356
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	0.00	0.50	0.000	0.020

8

PLCC-28

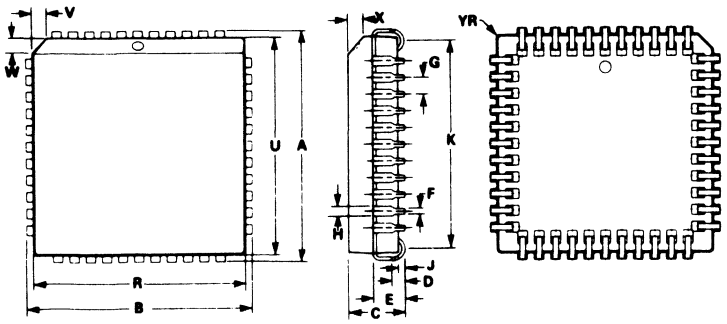
CASE 776



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.32	12.57	0.485	0.495
B	12.32	12.57	0.485	0.495
C	4.19	4.57	0.165	0.180
D	0.64	1.01	0.025	0.040
E	2.16	2.79	0.085	0.110
F	0.33	0.53	0.013	0.021
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.38	0.63	0.015	0.025
K	9.91	10.92	0.390	0.430
R	11.43	11.58	0.450	0.456
U	11.43	11.58	0.450	0.456
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	0.00	0.50	0.000	0.020

PLCC-44

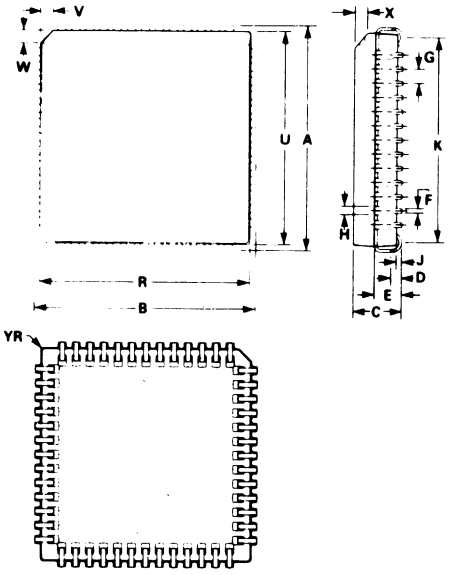
CASE 777



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	17.40	17.65	0.685	0.695
B	17.40	17.65	0.685	0.695
C	4.19	4.57	0.165	0.180
D	0.64	1.01	0.025	0.040
E	2.16	2.79	0.085	0.110
F	0.33	0.53	0.013	0.021
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.38	0.63	0.015	0.025
K	14.99	16.00	0.590	0.630
R	16.51	16.66	0.650	0.656
U	16.51	16.66	0.650	0.656
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	0.00	0.50	0.000	0.020

PLCC-52

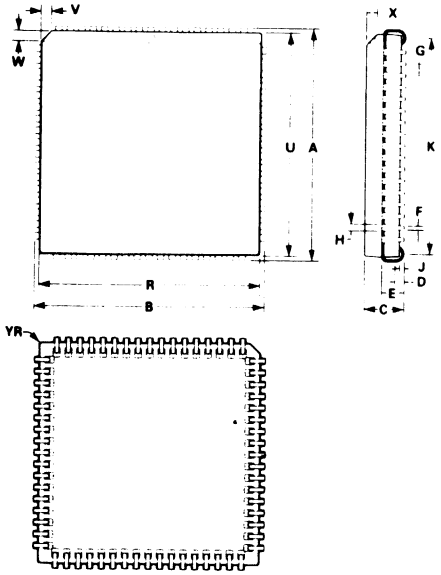
CASE 778



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	19.94	20.19	0.785	0.795
B	19.94	20.19	0.785	0.795
C	4.19	4.57	0.165	0.180
D	0.64	1.01	0.025	0.040
E	2.16	2.79	0.085	0.110
F	0.33	0.53	0.013	0.021
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.38	0.63	0.015	0.025
K	17.52	18.54	0.690	0.730
R	19.05	19.20	0.750	0.756
U	19.05	19.20	0.750	0.756
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	0.00	0.50	0.000	0.020

PLCC-68

CASE 779

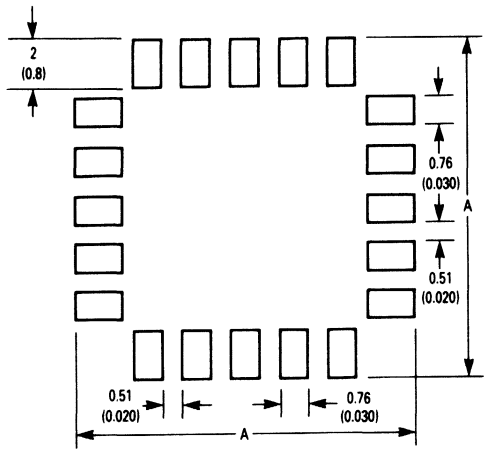


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	25.02	25.27	0.985	0.995
B	25.02	25.27	0.985	0.995
C	4.19	4.57	0.165	0.180
D	0.64	1.01	0.025	0.040
E	2.16	2.79	0.085	0.110
F	0.33	0.53	0.013	0.021
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.38	0.63	0.015	0.025
K	22.61	23.62	0.890	0.930
R	24.13	24.28	0.950	0.956
U	24.13	24.28	0.950	0.956
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	0.00	0.50	0.000	0.020

Geometries

Surface mount board layout is a critical portion of the total design. The "foot print" for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry the packages will self align when subjected to a solder reflow process.

Unit: mm (inch) Min Value

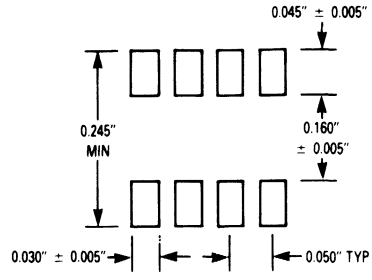


Unit: mm (inch)
Min. Value

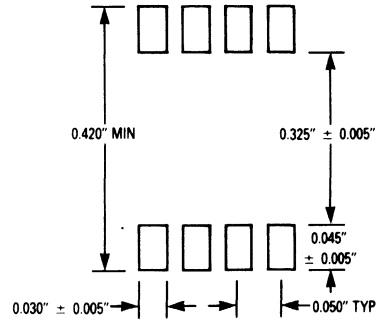
Dimension A	Inches	mm
PLCC20	0.430	10.9
PLCC28	0.530	13.5
PLCC44	0.630	16
PLCC52	0.830	21.1
PLCC68	1.030	25.1

PLCC

RECOMMENDED SOLDER PADS FOR SO PACKAGES

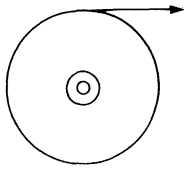


SO-8, SO-14, SO-16



SO-16L, SO-20L,
SO-18L

8

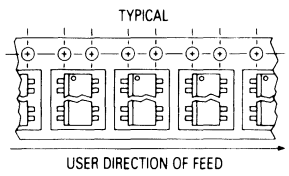


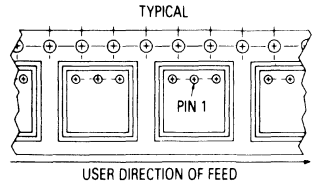
Tape and Reel

Standard Bipolar Logic, Bipolar Analog and MOS Integrated Circuits

Motorola has now added the convenience of Tape and Reel packaging for our growing family of standard Integrated Circuit products. Two reel sizes are available, for all but the largest types, to support the requirements of both first and second generation pick-and-place equipment. The packaging fully conforms to the latest EIA RS-481A specification. The antistatic embossed tape provides a secure cavity, sealed with a peel-back cover tape.

SOIC DEVICES **Mechanical Polarization** **PLCC DEVICES**





Package	Tape Width (mm)	Device per Reel	Reel Size* (inch)	Tape & Reel Lot Size(1) (Min)	Device Suffix
SO-8	12 12	500 2,500	7 13	5,000 5,000	R1 R2
SO-14	16 16	500 2,500	7 13	5,000 5,000	R1 R2
SO-16	16 16	500 2,500	7 13	5,000 5,000	R1 R2
SO-16 WIDE	16 16	250 1,000	7 13	5,000 5,000	R1 R2
SO-20 WIDE	24 24	250 1,000	7 13	5,000 5,000	R1 R2
SO-24 WIDE	24 24	250 1,000	7 13	5,000 5,000	R1 R2
SO-28 WIDE	24 24	200 1,000	7 13	3,000 3,000	R1 R2
PLCC-20	16 16	200 1,000	7 13	3,000 3,000	R1 R2
PLCC-28	24 24	200 500	7 13	2,400 2,500	R1 R2
PLCC-44	32 32	200 500	7 13	2,000 2,000	R1 R2
PLCC-52 PLCC-68 PLCC-84	32 44 44	500 250 250	13 13 13	2,000 2,000 2,000	R2 R2 R2
TO-92	38	2000	13	10,000	RA or RE only
TO-220	Contact local sales office for information				

Notes: 1. Minimum lot size information applies to OEM customers. Distributors may break lots or reels at their option, however broken reels may not be returned.

For ordering information please contact your local Motorola Semiconductor Sales Office.
Distribution minimum order quantity is 1 reel.
*Reel Size: 7"/178 mm, 13"/330 mm.

8